NEC

MOS INTEGRATED CIRCUIT
μPD4702

INCREMENTAL ENCODER 8-BIT UP/DOWN COUNTER
CMOS INTEGRATED CIRCUITS

DESCRIPTION

The μPD4702 is 8-bit up/down counters for an incremental encoder. Two-phase (A, B) incremental input signals are phase-differentiated, and on each signal edge, an up-count is executed if the A phase is leading, or a down-count if the B phase is leading. Eight-bit count data is output in real time. A carry output and borrow output are also provided for counter overflow and underflow.

The μPD4704 is also available; use of these enables the count width to be extended.

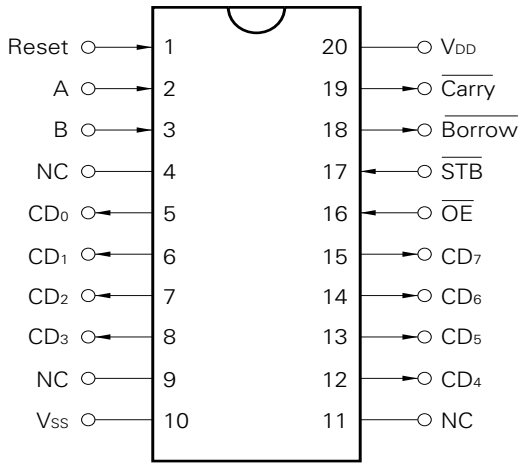
FEATURES

- Incremental inputs (A, B)
- On-chip phase discrimination circuit (up-count mode when the phase order is A → B, down-count mode when B → A) 4-multiplication count method
- On-chip edge detection circuit
- 8-bit up/down counter latch output o Carry output, borrow output
- Count data output controllable (3-state output)
- CMOS, single +5 V power supply

ORDERING INFORMATION

Part Number	Package	
μPD4702C	20-pin plastic DIP	(300 mil)
μPD4702G	20-pin plastic SOP	(300 mil)

PIN CONFIGURATION (Top View)



PIN NAMES

A, B } 2-phase incremental signal inputs
Reset : Counter reset input
$\overline{STB}$: Latch strobe signal input
$\overline{OE}$: Output control signal input
CD_{0-7} : Count data outputs
$\overline{Carry}$: Carry pulse output
$\overline{Borrow}$: Borrow pulse output

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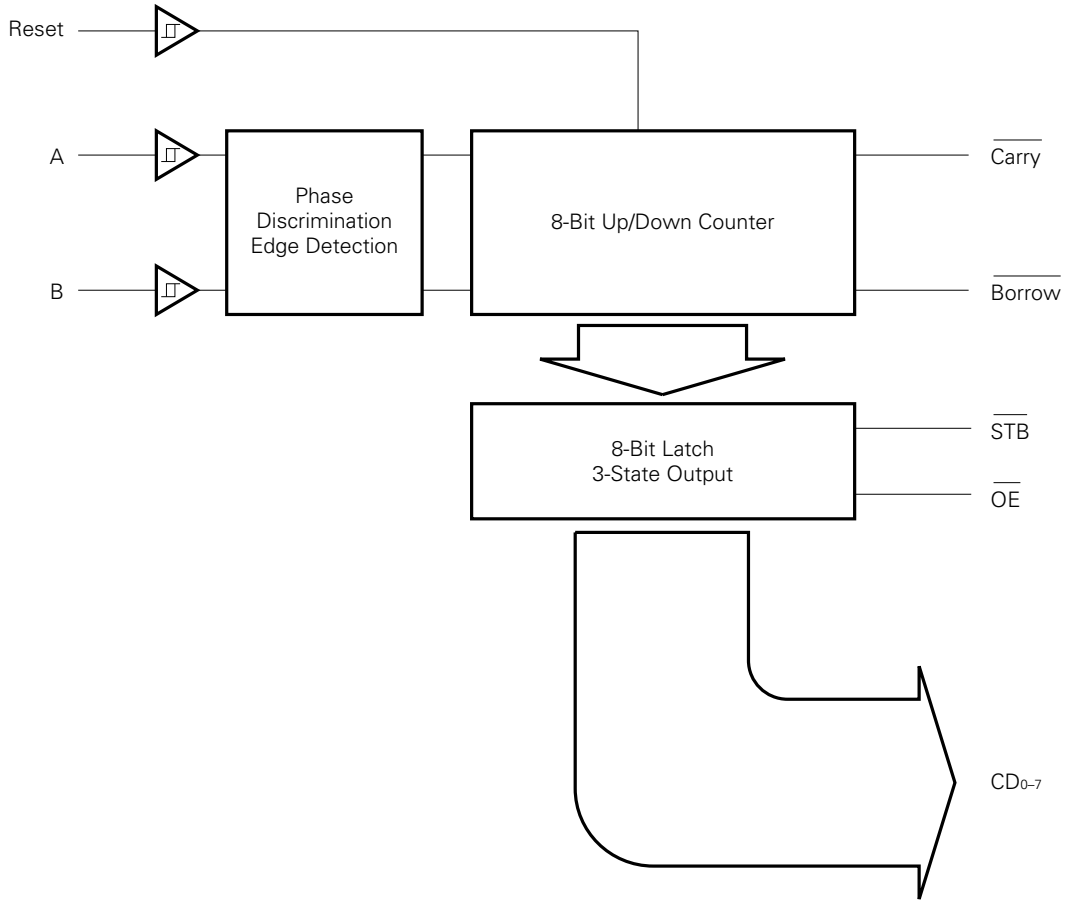
BLOCK DIAGRAM



PIN FUNCTIONS

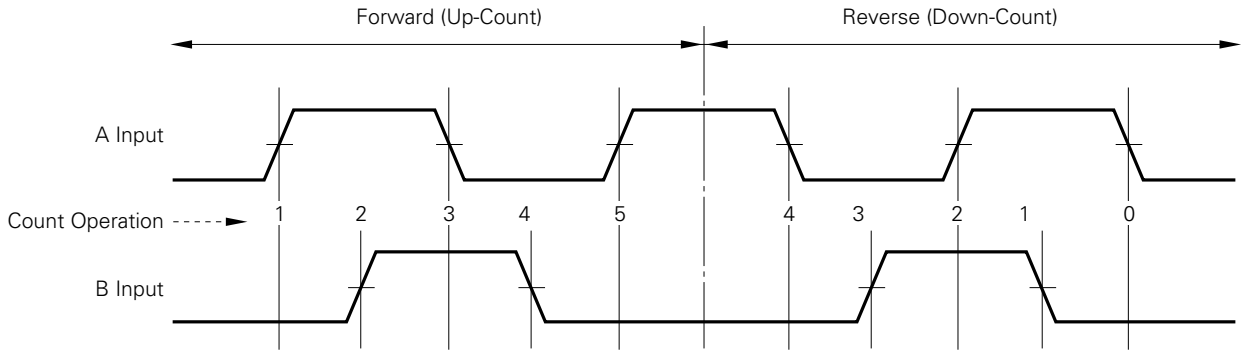
Pin Name	Input/Output	Function
A, B	Input (Schmitt)	Incremental signal A phase and B phase signal input pins (Schmitt input)
$D_{0\ to\ 7}$	Output (3-state)	Count data output pins. Activated when $\overline{OE}$ is "L", high impedance outputs when $\overline{OE}$ is "H".
$\overline{Carry}$	Output	8-bit counter carry signal output pin (active-low)
$\overline{Borrow}$	Output	8-bit counter borrow signal output pin (active-low)
RESET	Input (Schmitt)	8-bit counter reset signal output pin Counter is reset when this pin is "H".
$\overline{OE}$	Input	Count data output control signal input pin
$\overline{STB}$	Input	Counter data output latch signal. Data is latched on the fall of $\overline{STB}$, and is held while STB = "L".
V_{DD}		Power supply input pin
GND		Ground pin

1. DESCRIPTION OF OPERATIONS

(1) Count operation

The μPD4702 incorporates a phase discrimination circuit, and counts by 4-multiplication of the A and B input 2-phase pulses. Therefore, a count operation is performed by an A input edge and a B input edge.

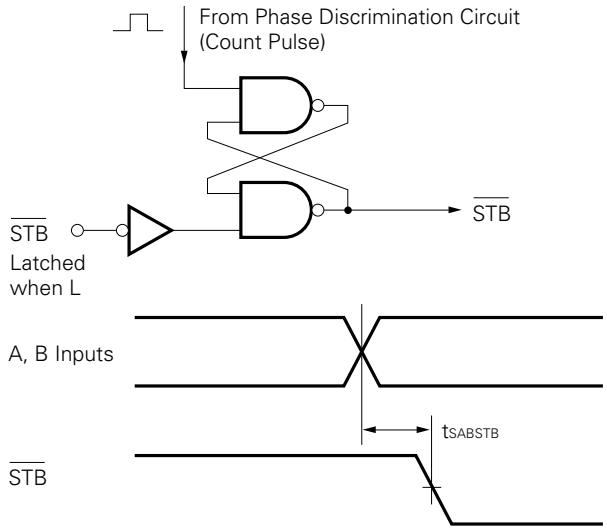
Fig. 1 Count Operation Timing Chart



(2) Latch operation

An R-S flip-flop is inserted in the strobe input of the latch circuit as shown in Fig. 2, and when $\overline{STB}$ changes from "H" to "L" during a count operation, the internal latch signal $\overline{STB}$ remains at "H" until the end of the count operation. Therefore, the count value is latched correctly even if $\overline{STB}$ input is performed asynchronously from the A and B input (if $\overline{STB}$ changes from "H" to "L" within t_{SABSTB} (40 ns) after the A input or B input edge, the latch contents will be either the pre-count or post-count value). However, when a μPD4704 is added, the correct value cannot be latched if all digits are latched simultaneously when a carry or borrow is generated (the high-order digit may be latched before carry/borrow transmission).

Fig. 2 $\overline{STB}$ Input Circuit



If t_{SABSTB} is 40 ns or longer, the post-count value is input to the latch.

(3) Carry & borrow outputs

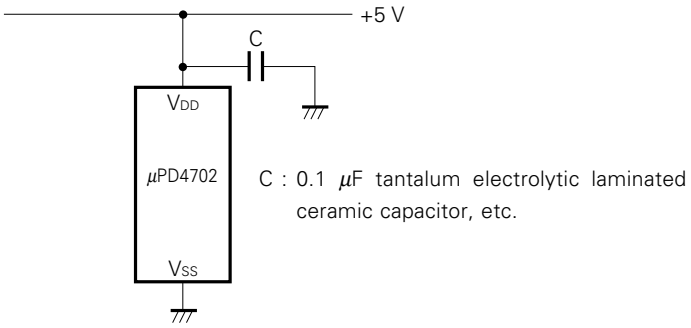
If the counter performs an up-count operation when the count value is 0FF$_H$, an active-low pulse is output to the $\overline{\text{Carry}}$ output (the pulse width is 25 ns MIN. 120 ns MAX. irrespective of the A/B phase input cycle. Similarly, if the counter performs a down-count operation when the count value is 00$_H$, an active-low pulse is output to the $\overline{\text{Borrow}}$ output.

A $\overline{\text{Borrow}}$ pulse is also output if a down-count operation is performed while RESET is "H" (during a reset), and therefore, when a μPD4704 is added, a reset must be executed at the same time.

2. OPERATING PRECAUTIONS

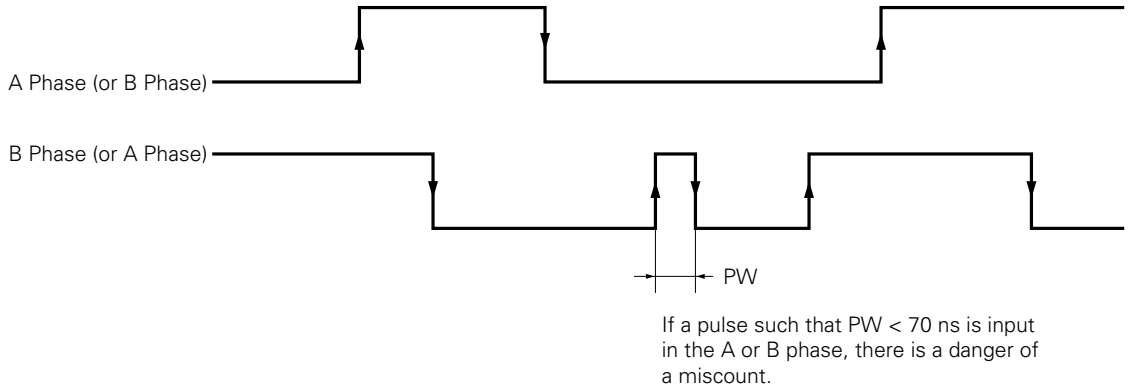
As the μPD4702 incorporates an 8-bit counter, a large transient current flows in the case of a count value which changes all the bits (such as $00_H \leftrightarrow 0FF_H$ or $7F_H \leftrightarrow 080_H$). This will cause misoperation unless the impedance of the power supply line is sufficiently low. It is therefore recommended that a decoupling capacitor (of around 0.1 μF) be connected between V_{DD} and V_{SS} right next to the IC as shown in Fig. 3.

Fig. 3 Decoupling Capacitor



Also, if a pulse shorter than the phase difference time t_{SAB} (70 ns) is input to the A/ B phase inputs, this will result in a miscount. Therefore, if this kind of pulse is to be input because of encoder bounds, etc., a filter should be inserted in the A & B phase inputs.

Fig. 4 A & B Phase Input Pulses



If PW is at 70 ns or more, the count value remains the same before and after pulse input. (UP count → DOWN count or DOWN count → UP count is implemented, and therefore the the result is no change in the count value.)

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, V_{SS} = 0 V)

PARAMETER	SYMBOL	RATING		UNIT
Supply voltage	V_{DD}	–0.5 to +7.0		V
Input voltage	V_I	–1.0 to V_{DD} +1.0		V
Output voltage	V_O	–0.5 to V_{DD} +0.5		V
Operating temperature	T_{opt}	–40 to +85		°C
Storage temperature	T_{stg}	–65 to +150		°C
Permissible loss	P_D	500 (DIP)	200 (SOP)	mW

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = +5 V ±10 %)

PARAMETER	SYMBOL	TEST CONDITIONS	RATING		UNIT
			MIN.	MAX.	
Input voltage high	V_{IL}			0.8	V
Input voltage low	V_{IH}	A, B, Reset	2.6		V
	V_{IH}	Other than the above	2.2		V
Output voltage low	V_{OL}	I_{OL} = 12 mA		0.45	V
Output voltage high	V_{OH}	I_{OH} = –4 mA	V_{DD} – 0.8		V
Static consumption current	I_{DD}	V_I = V_{DD}, V_{SS}		50	μA
Input current	I_I	V_I = V_{DD}, V_{SS}	–1.0	1.0	μA
3-state output leak current	I_{OFF}		–10	10	μA
Dynamic consumption current	$I_{DD\ dyn}$	f_{IN} = 3.6 MHz, C_L = 50 pF		12	mA
Hysteresis voltage	V_H	A, B, Reset	0.2		V

AC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = +5 V ±10 %)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
A, B	Cycle	t_{CYAB}	f_{in} = 3.6 MHz	280		ns
	High-level width	t_{PWABH}		140		ns
	Low-level width	t_{PWABL}		140		ns
	Phase difference time	t_{SAB}		70		ns
	Setting time	t_{SRSAB}		0		ns
$CD_{0\ to\ 7}$	Reset time	t_{DRSCD}			60	ns
	Output delay	t_{DABCD}			100	ns
	Output delay	t_{DOECD}			50	ns
	Output delay	t_{DSTBCD}			60	ns
	Float time	t_{FOECD}			40	ns
$\overline{Carry}$	Output delay	t_{DABCB}			120	ns
$\overline{Borrow}$	Output pulse width	t_{PWCB}		25	120	ns
RESET	Reset pulse width	t_{PWRS}		40		ns
$\overline{STB}$	Setting time	t_{SABSTB}		40		ns

AC Timings

Fig. 1 Two-Phase Signal Input Timing

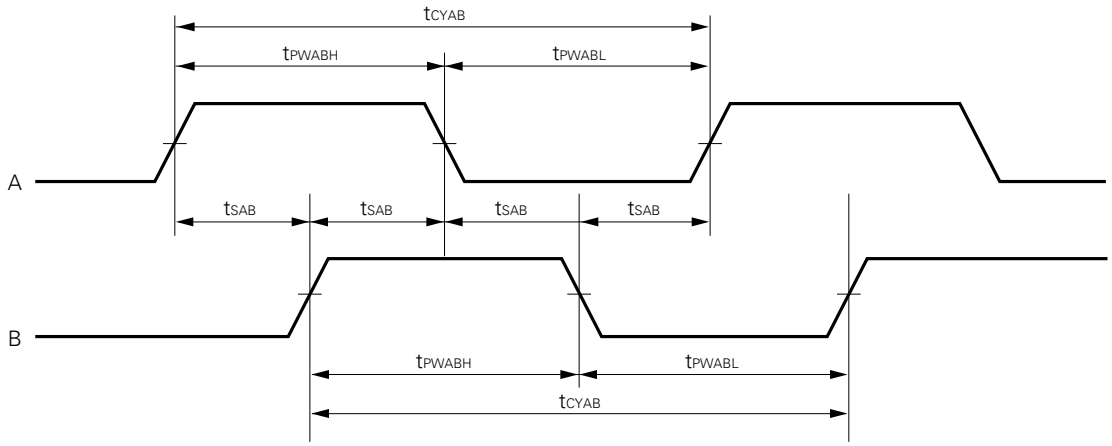


Fig. 2 Count Data Output Timing

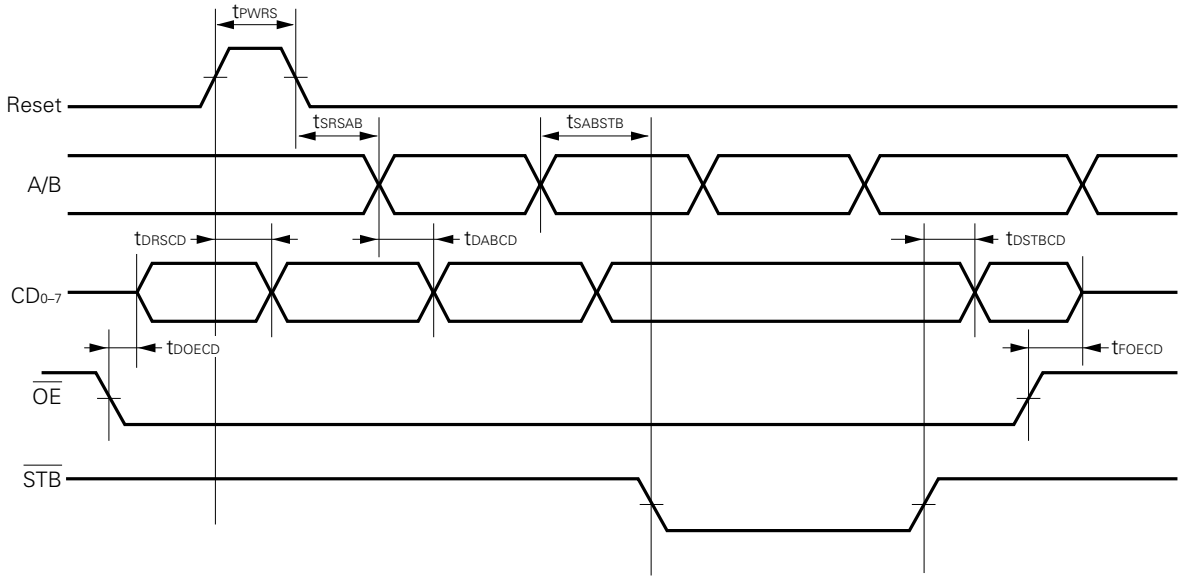
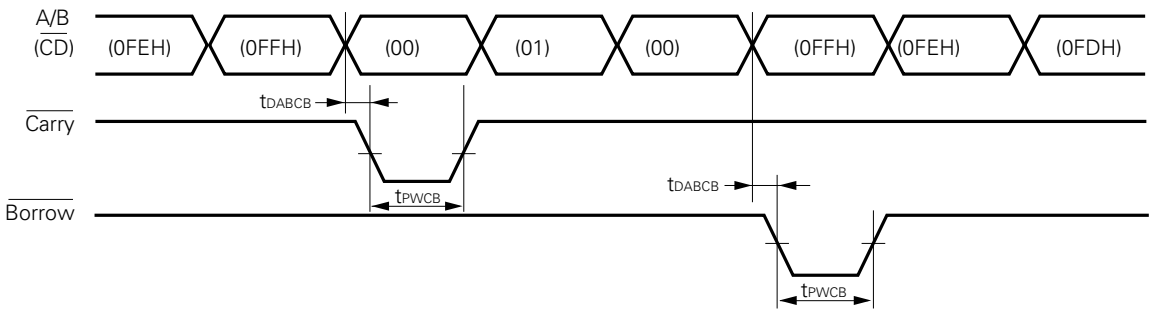
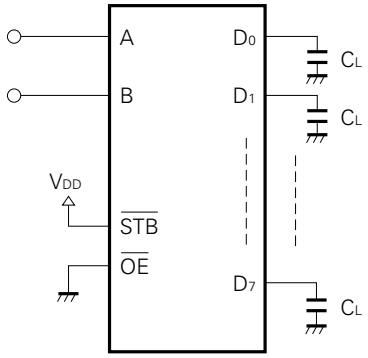


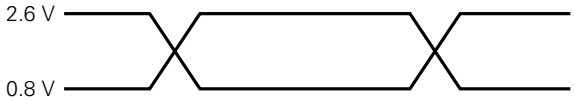
Fig. 3 Carry/Borrow Signal Output Timing



Consumption Current Measurement Circuit

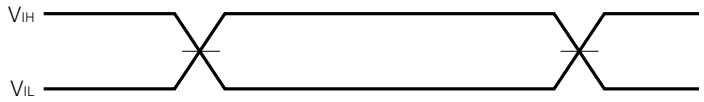


Measurement Conditions
A, B inputs
f_{IN} = 3.6 MHz



$\overline{STB}$ input connected to V_{DD} or
$\overline{OE}$ input connected to V_{SS}.
Load on all outputs, C_L = 50 pF.

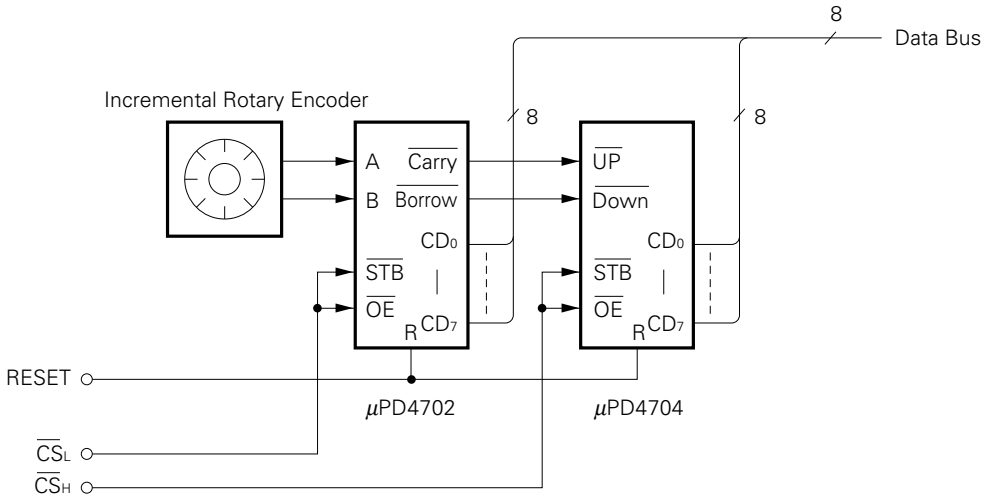
AC Test Input Waveform



V_{IH} = 2.6 V (A, B, RESET inputs)
V_{IH} = 2.2 V (inputs other than A, B, RESET)
V_{IL} = 0.8 V
Timing measurement is performed at 1.5 V.

Sample Application Circuits

16-bit counter



The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPES OF SURFACE MOUNT DEVICE

For more details, refer to our document **"Semiconductor Device Mounting Technology Manual" (IEI-1207)**.

μPD4702G

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 2, Exposure limit*: None	IR35-00-2
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 2, Exposure limit*: None	VP15-00-2
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below, Number of flow process: 1, Exposure limit*: None	WS60-00-1
Partial heating method	Terminal temperature: 300 °C or below, Flow time: 10 seconds or below, Exposure limit*: None	

* Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Note Do not apply more than a single process at once, except for "Partial heating method".

TYPES OF THROUGH HOLE MOUNT DEVICE

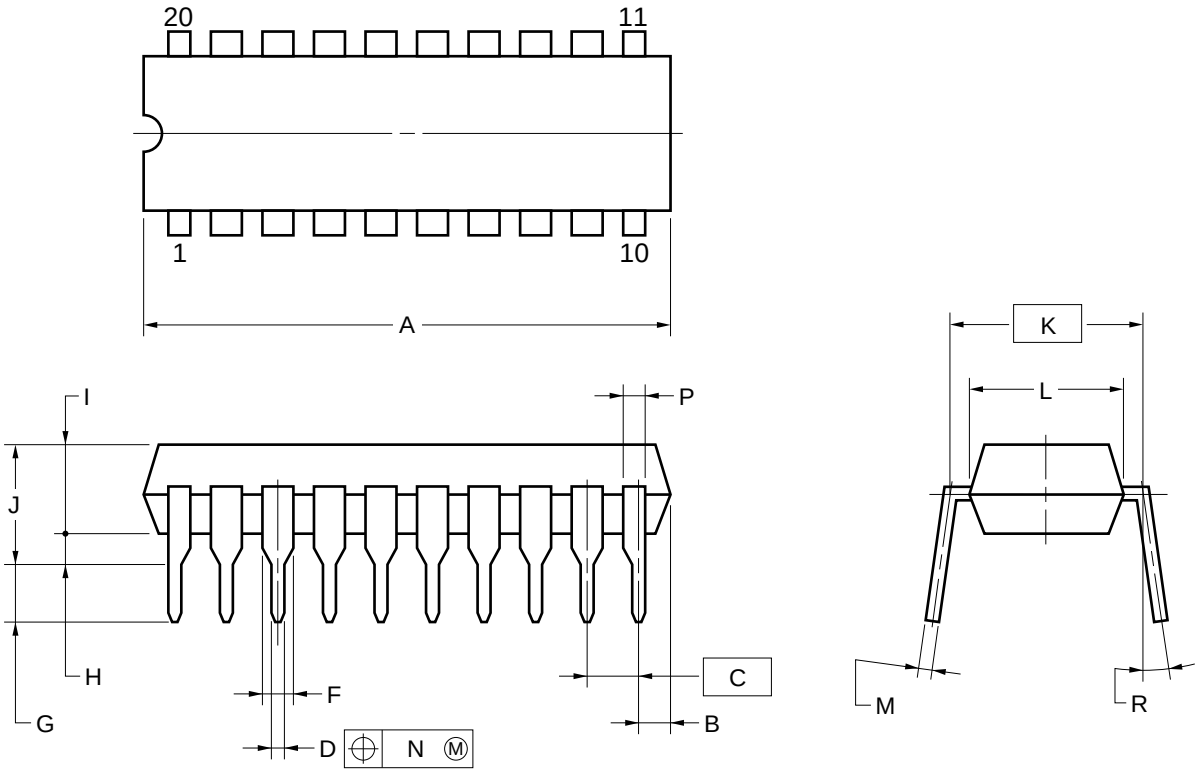
μPD4702C

Soldering process	Soldering conditions	Symbol
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below	

REFERENCE

Dcodument name	Document No.
NEC semiconductor device reliability/quality control system	IEI-1212
Quality grade on NEC semiconductor devices	IEI-1209
Semiconductor device mounting technology manual	IEI-1207
Semiconductor device package manual	IEI-1213
Guide to quality assurance for semiconductor devices	MEI-1202
Semiconductor selection guide	MF-1134

20PIN PLASTIC DIP (300 mil)



NOTES

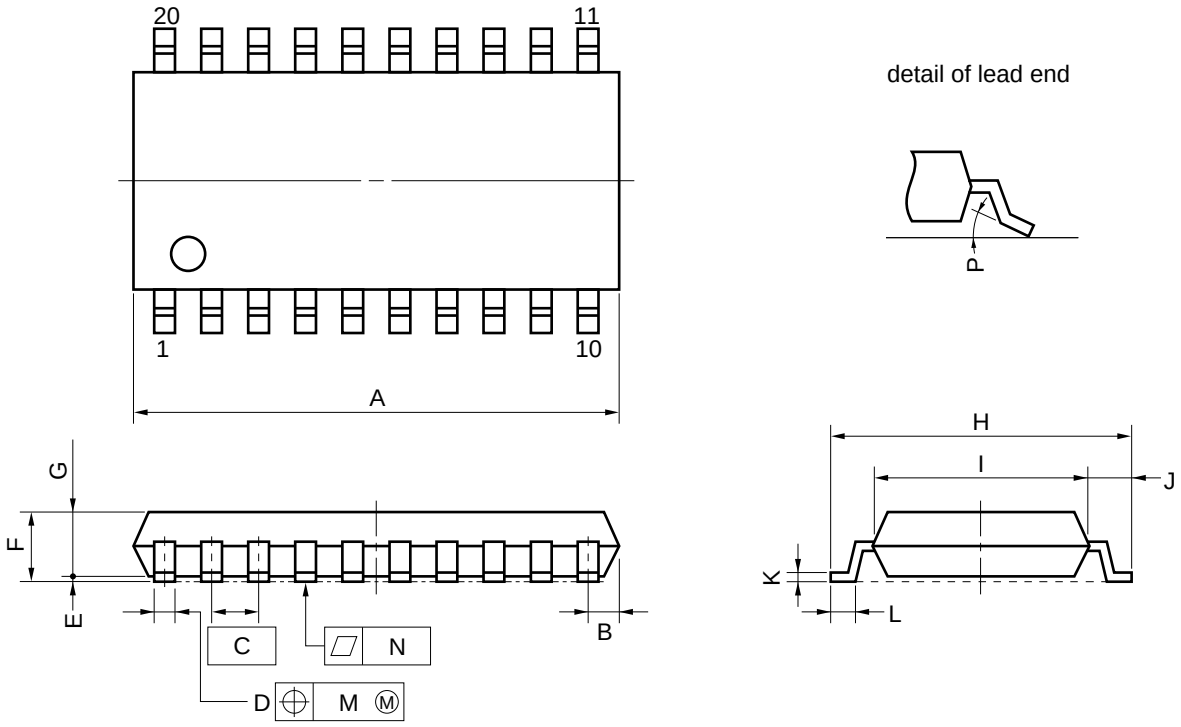
1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	25.40 MAX.	1.000 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	1.1 MIN.	0.043 MIN.
G	3.5±0.3	0.138±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.
R	0~15°	0~15°

P20C-100-300A,C-1

20 PIN PLASTIC SOP (300 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.00 MAX.	0.512 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1±0.1	0.004±0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7±0.3	0.303±0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6±0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005
N	0.10	0.004
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P20GM-50-300B, C-4

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