DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD70F3017A, 70F3017AY

V850/SA1™
32-/16-BIT SINGLE-CHIP MICROCONTROLLER

The μPD70F3017A, 70F3017AY are products with on-chip flash memory. Because the devices can be programmed by the user on-board, they are ideal for the evaluation stages of system development, small-scale production of a variety of products, and rapid development of new products.

The V850/SA1 provides a high-level cost performance ideal for applications ranging from low-power camcorders and other AV equipment to portable telephone equipment such as cellular phones and personal handyphone systems (PHS).

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

V850/SA1 User's Manual Hardware: U12768E
V850 Family™ User's Manual Architecture: U10243E

FEATURES

- Number of instructions: 74
- Minimum instruction execution time:
  59 ns (@ 17 MHz operation with main system clock (f_{XX}))
  50 ns (@ 20 MHz operation with main system clock (f_{XX}))
  30.5 μs (@ 32.768 kHz operation with subsystem clock (f_{XT}))
- General-purpose registers: 32 bits × 32 registers
- Instruction set:
  Signed multiplication, saturation operations, 32-bit shift instructions, bit manipulation instructions, load/store instructions
- Memory space:
  16 MB linear address space
  Memory block division function: 2 MB per block
- External bus interface: 16-bit data bus
  Address bus: Separate output enabled
- Internal memory
  Flash memory: 256 KB
  RAM: 8 KB
- Interrupts and exceptions
  External: 8, internal: 23, exceptions: 1
- I/O lines Total: 85
- Timer/counters
  16-bit timer: 2 channels
  8-bit timer: 4 channels
- Watch timer: 1 channel
- Watchdog timer: 1 channel
- Serial interface (SIO)
  Asynchronous serial interface (UART)
  Clocked serial interface (CSI)
  I^2C bus interface (μPD70F3017AY)
- A/D converter: 12 channels
- DMA controller: 3 channels
- RTP: 8 bits × 1 channel or 4 bits × 2 channels
- Power-saving functions: HALT/IDLE/STOP modes
- Packages: 100-pin plastic LQFP (14 × 14 mm)
  121-pin plastic FBGA (12 × 12 mm)

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The mark ★ shows major revised points.

APPLICATIONS

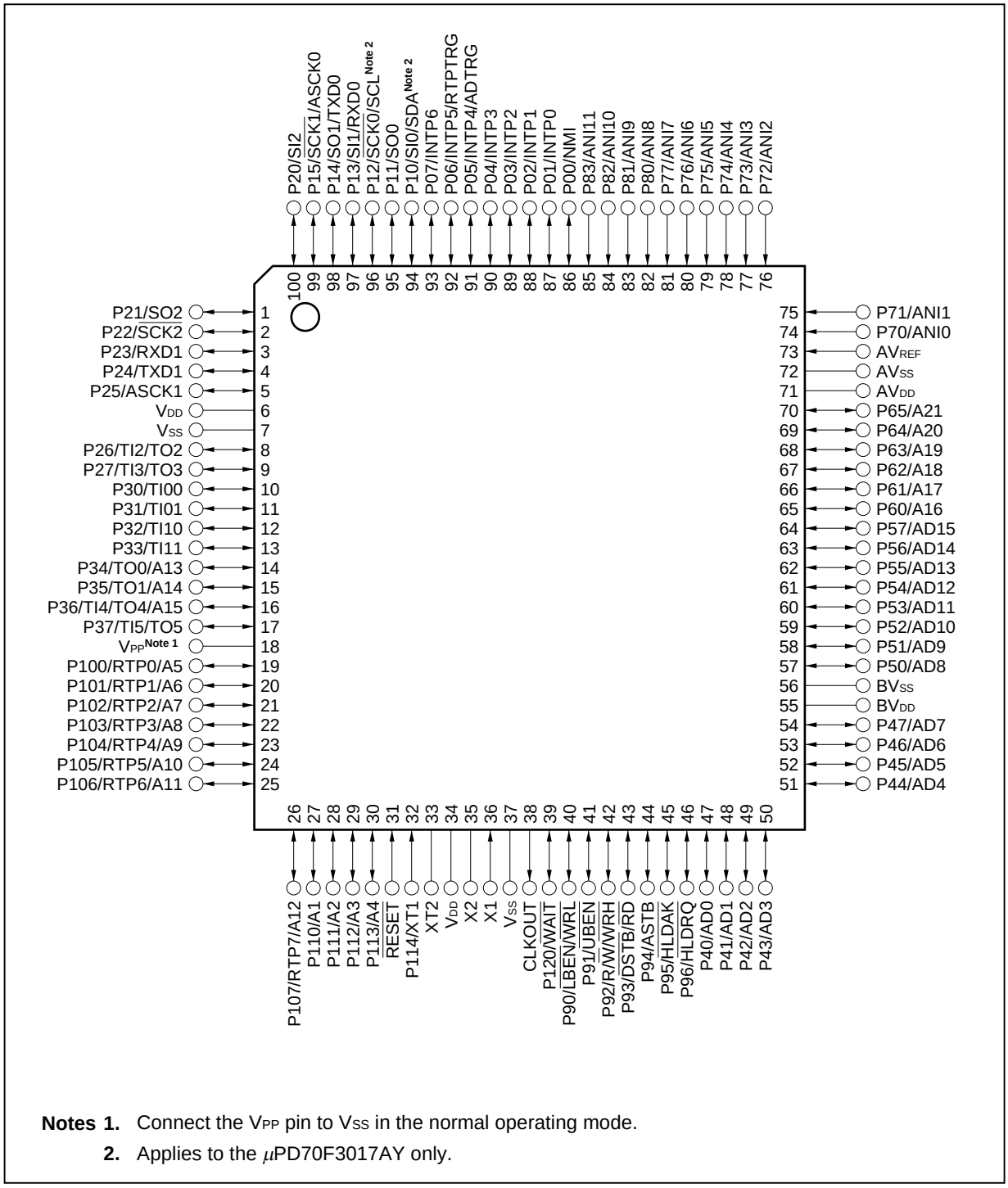
○ Low-power portable devices
Cellular phones, PHSs, and camcorders

★ ORDERING INFORMATION

Part Number	Package	Internal ROM
μPD70F3017AGC-8EU	100-pin plastic LQFP (fine-pitch) (14 × 14 mm)	256 KB (Flash memory)
μPD70F3017AF1-EA6	121-pin plastic FBGA (12 × 12 mm)	256 KB (Flash memory)
μPD70F3017AYGC-8EU	100-pin plastic LQFP (fine-pitch) (14 × 14 mm)	256 KB (Flash memory)
μPD70F3017AYF1-EA6	121-pin plastic FBGA (12 × 12 mm)	256 KB (Flash memory)

PIN CONFIGURATION

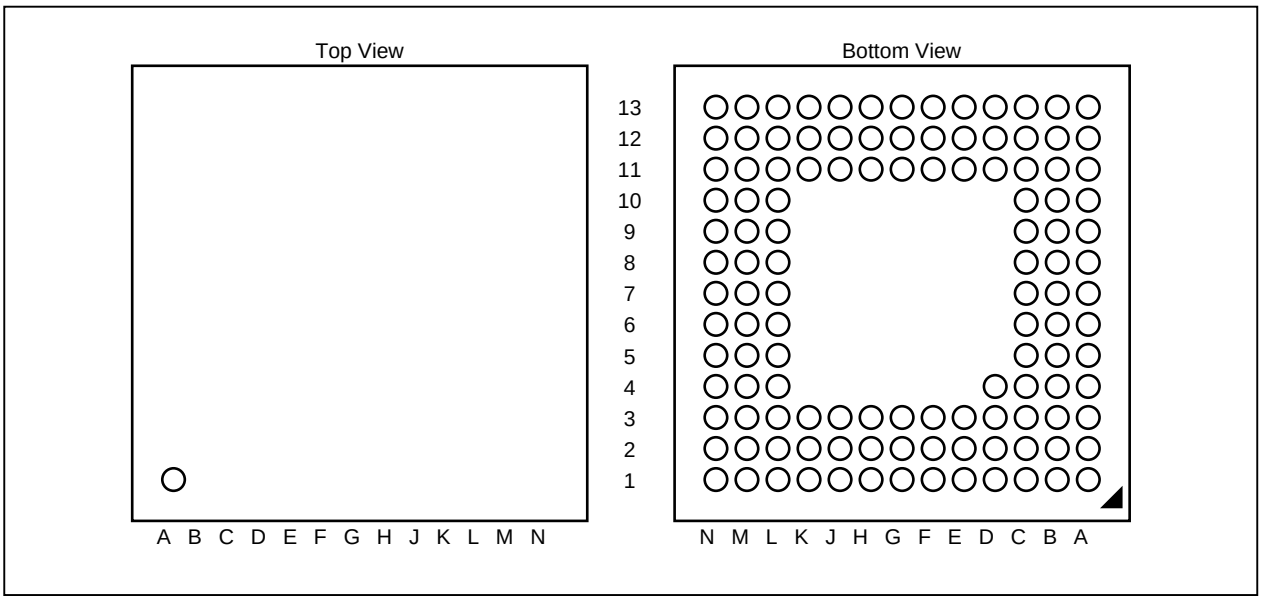
100-pin plastic LQFP (fine-pitch) (14 × 14 mm)
μPD70F3017AGC-8EU
μPD70F3017AYGC-8EU



Notes 1. Connect the V_{PP} pin to V_{SS} in the normal operating mode.

2. Applies to the μPD70F3017AY only.

★ 121-pin plastic FBGA (12 × 12 mm)
μPD70F3017AF1-EA6
μPD70F3017AYF1-EA6



Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
A1	P20	B8	P83	D2	V_{DD}	G11	P60	K13	BV_{DD}	M7	V_{SS}
A2	P15	B9	P80	D3	V_{SS}	G12	P56	L1	P104	M8	V_{SS}
A3	V_{SS}	B10	P75	D11	AV_{DD}	G13	P57	L2	P105	M9	P92
A4	P13	B11	AV_{SS}	D12	AV_{DD}	H1	P34	L3	$\overline{\text{RESET}}$	M10	P95
A5	P11	B12	AV_{SS}	D13	AV_{DD}	H2	P37	L4	V_{DD}	M11	P41
A6	P06	B13	P71	E1	P25	H3	P35	L5	V_{SS}	M12	P45
A7	P03	C1	P22	E2	V_{DD}	H11	P55	L6	X2	M13	P44
A8	P00	C2	P23	E3	P30	H12	P53	L7	P90	N1	P107
A9	P81	C3	V_{SS}	E11	AV_{DD}	H13	P54	L8	P120	N2	P110
A10	P76	C4	P24	E12	P64	J1	V_{PP}[Note]	L9	P93	N3	P112
A11	P73	C5	P07	E13	P65	J2	V_{PP}[Note]	L10	P96	N4	V_{DD}
A12	P72	C6	P04	F1	P26	J3	P100	L11	BV_{SS}	N5	XT1
A13	AV_{SS}	C7	P01	F2	P27	J11	P52	L12	BV_{SS}	N6	V_{SS}
B1	P21	C8	P82	F3	P33	J12	P50	L13	BV_{SS}	N7	V_{SS}
B2	P14	C9	P77	F11	P63	J13	P51	M1	P106	N8	CLKOUT
B3	V_{SS}	C10	P74	F12	P61	K1	P101	M2	P111	N9	P91
B4	P12	C11	AV_{SS}	F13	P62	K2	P102	M3	P113	N10	P94
B5	P10	C12	P70	G1	P31	K3	P103	M4	V_{DD}	N11	P40
B6	P05	C13	AV_{REF}	G2	P32	K11	P46	M5	XT2	N12	P42
B7	P02	D1	V_{DD}	G3	P36	K12	P47	M6	X1	N13	P43

Note Connect the V_{PP} pin to V_{SS} in the normal operating mode.

Remarks 1. Alternate function names are omitted. The alternate functions are identical to the 100-pin plastic LQFP.

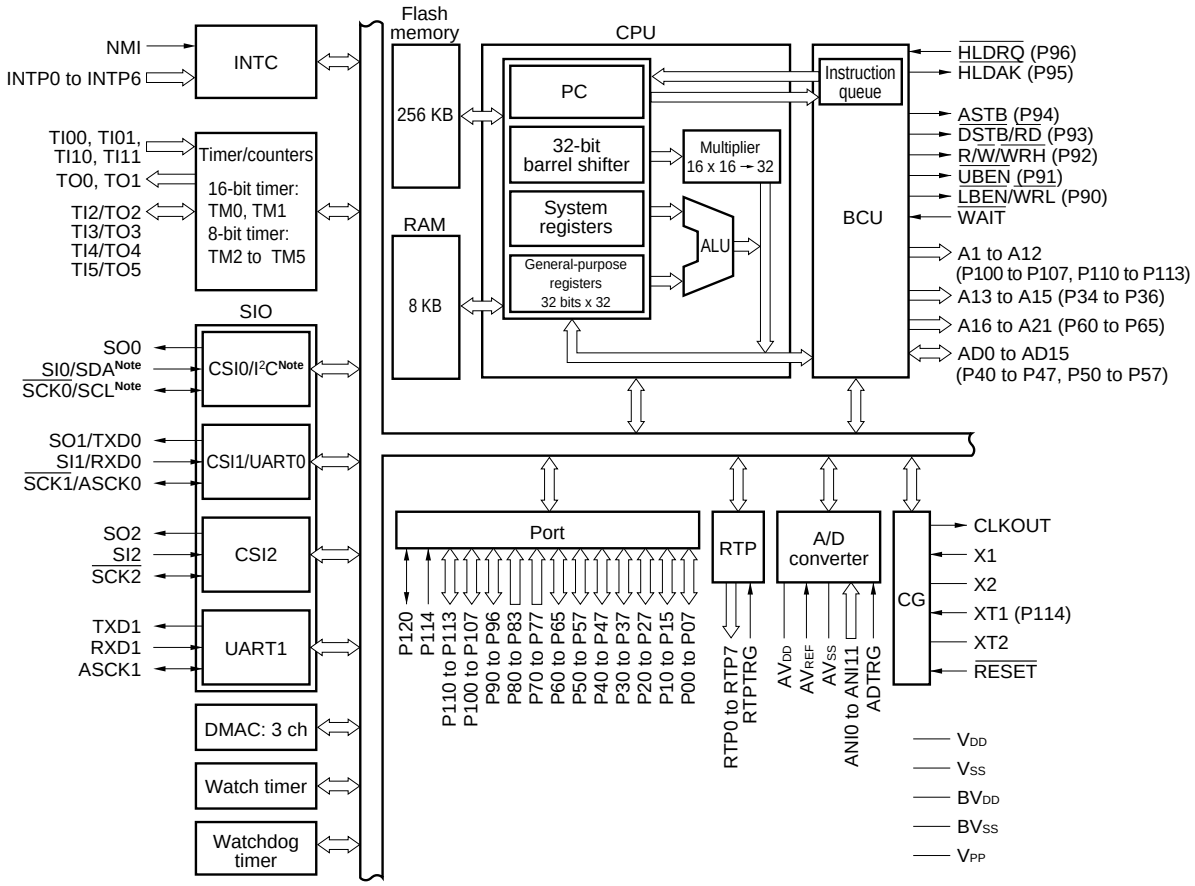
2. Connect the D4 pin directly to V_{SS}.

PIN IDENTIFICATION

A1 to A21:	Address Bus	P100 to P107:	Port 10
AD0 to AD15:	Address/Data Bus	P110 to P114:	Port 11
ADTRG:	AD Trigger Input	P120:	Port 12
ANI0 to ANI11:	Analog Input	$\overline{RD}$:	Read
ASCK0, ASCK1:	Asynchronous Serial Clock	$\overline{RESET}$:	Reset
ASTB:	Address Strobe	RTP0 to RTP7:	Real-Time Port
AV_{DD}:	Analog V_{DD}	RTPTRG:	RTP Trigger
AV_{REF}:	Analog Reference Voltage	R/$\overline{W}$:	Read/Write Status
AV_{SS}:	Analog V_{SS}	RXD0, RXD1:	Receive Data
BV_{DD}:	Power Supply for Bus Interface	$\overline{SCK0}$ to $\overline{SCK2}$:	Serial Clock
BV_{SS}:	Ground for Bus Interface	SCL[Note]:	Serial Clock
CLKOUT:	Clock Output	SDA[Note]:	Serial Data
$\overline{DSTB}$:	Data Strobe	SI0 to SI2:	Serial Input
$\overline{HLDAK}$:	Hold Acknowledge	SO0 to SO2:	Serial Output
$\overline{HLDRQ}$:	Hold Request	TI00, TI01, TI10, :	Timer Input
INTP0 to INTP6:	Interrupt Request From Peripherals	TI11, TI2 to TI5	
$\overline{LBEN}$:	Lower Byte Enable	TO0 to TO5:	Timer Output
NMI:	Non-maskable Interrupt Request	TXD0,TXD1:	Transmit Data
P00 to P07:	Port 0	$\overline{UBEN}$:	Upper Byte Enable
P10 to P15:	Port 1	V_{DD}:	Power Supply
P20 to P27:	Port 2	V_{PP}:	Programming Power Supply
P30 to P37:	Port 3	V_{SS}:	Ground
P40 to P47:	Port 4	$\overline{WAIT}$:	Wait
P50 to P57:	Port 5	$\overline{WRH}$:	Write Strobe High Level Data
P60 to P65:	Port 6	$\overline{WRL}$:	Write Strobe Low Level Data
P70 to P77:	Port 7	X1, X2:	Crystal for Main System Clock
P80 to P83:	Port 8	XT1, XT2:	Crystal for Subsystem Clock
P90 to P96:	Port 9		

Note Applies to the μPD70F3017AY only.

INTERNAL BLOCK DIAGRAM



Note Applies to the μPD70F3017AY only.

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1. PIN FUNCTIONS

1.1 Port Pins

(1/3)

Pin Name	I/O	PULL	Function	Alternate Function
P00	I/O	Yes	Port 0 8-bit I/O port Input/output can be specified in 1-bit units.	NMI
P01				INTP0
P02				INTP1
P03				INTP2
P04				INTP3
P05				INTP4/ADTRG
P06				INTP5/RTPTRG
P07				INTP6
P10	I/O	Yes	Port 1 6-bit I/O port Input/output can be specified in 1-bit units.	SI0/SDA[Note]
P11				SO0
P12				$\overline{\text{SCK0}}$/SCL[Note]
P13				SI1/RXD0
P14				SO1/TXD0
P15				$\overline{\text{SCK1}}$/ASCK0
P20	I/O	Yes	Port 2 8-bit I/O port Input/output can be specified in 1-bit units.	SI2
P21				SO2
P22				$\overline{\text{SCK2}}$
P23				RXD1
P24				TXD1
P25				ASCK1
P26				TI2/TO2
P27				TI3/TO3
P30	I/O	Yes	Port 3 8-bit I/O port Input/output can be specified in 1-bit units.	TI00
P31				TI01
P32				TI10
P33				TI11
P34				TO0/A13
P35				TO1/A14
P36				TI4/TO4/A15
P37				TI5/TO5

Note Applies to the μPD70F3017AY only.

Remark PULL: On-chip pull-up resistor

(2/3)

Pin Name	I/O	PULL	Function	Alternate Function
P40	I/O	No	Port 4 8-bit I/O port Input/output can be specified in 1-bit units.	AD0
P41				AD1
P42				AD2
P43				AD3
P44				AD4
P45				AD5
P46				AD6
P47				AD7
P50	I/O	No	Port 5 8-bit I/O port Input/output can be specified in 1-bit units.	AD8
P51				AD9
P52				AD10
P53				AD11
P54				AD12
P55				AD13
P56				AD14
P57				AD15
P60	I/O	No	Port 6 6-bit I/O port Input/output can be specified in 1-bit units.	A16
P61				A17
P62				A18
P63				A19
P64				A20
P65				A21
P70	Input	No	Port 7 8-bit input port	ANI0
P71				ANI1
P72				ANI2
P73				ANI3
P74				ANI4
P75				ANI5
P76				ANI6
P77				ANI7
P80	Input	No	Port 8 4-bit input port	ANI8
P81				ANI9
P82				ANI10
P83				ANI11

Remark PULL: On-chip pull-up resistor

(3/3)

Pin Name	I/O	PULL	Function	Alternate Function
P90	I/O	No	Port 9 7-bit I/O port Input/output can be specified in 1-bit units.	$\overline{\text{LBEN}}$/$\overline{\text{WRL}}$
P91				$\overline{\text{UBEN}}$
P92				R/$\overline{\text{W}}$/$\overline{\text{WRH}}$
P93				$\overline{\text{DSTB}}$/$\overline{\text{RD}}$
P94				ASTB
P95				$\overline{\text{HLDAK}}$
P96				$\overline{\text{HLDRQ}}$
P100	I/O	Yes	Port 10 8-bit I/O port Input/output can be specified in 1-bit units.	RTP0/A5
P101				RTP1/A6
P102				RTP2/A7
P103				RTP3/A8
P104				RTP4/A9
P105				RTP5/A10
P106				RTP6/A11
P107				RTP7/A12
P110	I/O	Yes	Port 11 5-bit I/O port Input/output can be specified in 1-bit units. P114 is fixed as input only.	A1
P111				A2
P112				A3
P113				A4
P114	Input	No		XT1
P120	I/O	No	Port 12 1-bit I/O port	$\overline{\text{WAIT}}$

Remark PULL: On-chip pull-up resistor

1.2 Non-Port Pins

(1/3)

Pin Name	I/O	PULL	Function	Alternate Function
A1 to A4	Output	Yes	Low-order address bus used for external memory expansion	P110 to P113
A5 to A12				P100/RTP0 to P107/RTP7
A13				P34/TO0
A14				P35/TI1
A15				P36/TI4/TO4
A16 to A21	Output	No	High-order address bus used for external memory expansion	P60 to P65
AD0 to AD7	I/O	No	16-bit multiplexed address/data bus used for external memory expansion	P40 to P47
AD8 to AD15				P50 to P57
ADTRG	Input	Yes	A/D converter external trigger input	P05/INTP4
ANI0 to ANI7	Input	No	Analog input to A/D converter	P70 to P77
ANI8 to ANI11	Input	No		P80 to P83
ASCK0	Input	Yes	Serial clock input for UART0 and UART1	P15/$\overline{\text{SCK1}}$
ASCK1				P25
ASTB	Output	No	External address strobe signal output	P94
AV_{DD}	–	–	Positive power supply for A/D converter	–
AV_{REF}	Input	–	Reference voltage input for A/D converter	–
AV_{SS}	–	–	Ground potential for A/D converter	–
BV_{DD}	–	–	Positive power supply for bus interface	–
BV_{SS}	–	–	Ground potential for bus interface	–
CLKOUT	Output	–	Internal system clock output	–
$\overline{\text{DSTB}}$	Output	No	External data strobe signal output	P93/$\overline{\text{RD}}$
$\overline{\text{HLDAK}}$	Output	No	Bus hold acknowledge output	P95
$\overline{\text{HLDRQ}}$	Input	No	Bus hold request input	P96
INTP0 to INTP3	Input	Yes	External interrupt request input (analog noise elimination)	P01 to P04
INTP4			External interrupt request input (digital noise elimination)	P05/ADTRG
INTP5				P06/RTPTRG
INTP6				P07
$\overline{\text{LBEN}}$	Output	No	External data bus's low-order byte enable signal output	P90/$\overline{\text{WRL}}$
NMI	Input	Yes	Non-maskable interrupt request input	P00
$\overline{\text{RD}}$	Output	No	Read strobe signal output	P93/$\overline{\text{DSTB}}$
$\overline{\text{RESET}}$	Input	–	System reset input	–
RTP0 to RTP7	Output	Yes	Real-time output port	P100/A5 to P107/A12

Remark PULL: On-chip pull-up resistor

(2/3)

Pin Name	I/O	PULL	Function	Alternate Function
RTPTRG	Input	Yes	RTP external trigger input	P06/INTP5
R/$\overline{W}$	Output	No	External read/write status output	P92/$\overline{WRH}$
RXD0	Input	Yes	Serial receive data input for UART0 and UART1	P13/SI1
RXD1				P23
$\overline{SCK0}$	I/O	Yes	Serial clock I/O (3-wire type) for CSI0 to CSI2	P12
$\overline{SCK1}$				P15/ASCK0
$\overline{SCK2}$				P22
SCL			I^2C serial clock I/O (μPD70F3017AY only)	P12/$\overline{SCK0}$
SDA			I^2C serial transmit/receive data I/O (μPD70F3017AY only)	P10/SI0
SI0	Input	Yes	Serial receive data input (3-wire type) for CSI0 to CSI2	P10
SI1				P13/RXD0
SI2				P20
SO0	Output	Yes	Serial transmit data output (3-wire type) for CSI0 to CSI2	P11
SO1				P14/TXD0
SO2				P21
TI00	Input	Yes	External capture trigger input and external count clock input for TM0	P30
TI01			External capture trigger input for TM0	P31
TI10			External capture trigger input and external count clock input for TM1	P32
TI11			External capture trigger input for TM1	P33
TI2			External count clock input for TM2	P26/TO2
TI3			External count clock input for TM3	P27/TO3
TI4			External count clock input for TM4	P36/TO4/A15
TI5			External count clock input for TM5	P37/TO5
TO0, TO1	Output	Yes	Pulse signal output for TM0, TM1	P34/A13, P35/A14
TO2			Pulse signal output for TM2	P26/TI2
TO3			Pulse signal output for TM3	P27/TI3
TO4			Pulse signal output for TM4	P36/TI4/A15
TO5			Pulse signal output for TM5	P37/TI5
TXD0	Output	Yes	Serial transmit data output for UART0 and UART1	P14/SO1
TXD1				P24
$\overline{UBEN}$	Output	No	High-order byte enable signal output for external data bus	P91
V_{DD}	–	–	Positive power supply pin	–
V_{SS}	–	–	GND potential	–

Remark PULL: On-chip pull-up resistor

(3/3)

Pin Name	I/O	PULL	Function	Alternate Function
$\overline{\text{WAIT}}$	Input	No	Control signal input for inserting wait in bus cycle	P120
$\overline{\text{WRH}}$	Output	No	High-order byte write strobe signal output for external data bus	P92/R/$\overline{\text{W}}$
$\overline{\text{WRL}}$			Low-order byte write strobe signal output for external data bus	P90/$\overline{\text{LBEN}}$
X1	Input	No	Resonator connection for main system clock	–
X2	–			–
XT1	Input	No	Resonator connection for subsystem clock	P114
XT2	–			–
V_{PP}	–	–	Pin to which high voltage is applied during program write/verify	–

Remark PULL: On-chip pull-up resistor

1.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 1-1. For the input/output schematic circuit diagram of each type, refer to Figure 1-1.

Table 1-1. Types of Pin I/O Circuits (1/2)

Pin	Alternate Function	I/O Circuit Type	Recommended Connection of Unused Pins
P00	NMI	8-A	Input: Connect to V_{SS} Output: Leave open
P01 to P04	INTP0 to INTP3		
P05	INTP4/ADTRG		
P06	INTP5/RTPTRG		
P07	INTP6		
P10	SI0/SDA[Note]	10-A	Input: Connect to V_{DD} or V_{SS} Output: Leave open
P11	SO0	26	
P12	$\overline{SCK0}$/SCL[Note]	10-A	
P13	SI1/RXD0	8-A	
P14	SO1/TXD0	26	
P15	$\overline{SCK1}$/ASCK0	10-A	
P20	SI2	8-A	
P21	SO2	26	
P22	$\overline{SCK2}$	10-A	
P23	RXD1	8-A	
P24	TXD1	5-A	
P25	ASCK1	8-A	
P26, P27	TI2/TO2, TI3/TO3		
P30, P31	TI00, TI01		
P32, P33	TI10, TI11		
P34, P35	TO0/A13, TO1/A14	5-A	
P36	TI4/TO4/A15	8-A	
P37	TI5/TO5		
P40 to P47	AD0 to AD7	5	Input: Connect to BV_{DD} or BV_{SS} Output: Leave open
P50 to P57	AD8 to AD15		
P60 to P65	A16 to A21		
P70 to P77	ANI0 to ANI7	9	Connect to AV_{SS} or AV_{DD}
P80 to P83	ANI8 to ANI11		

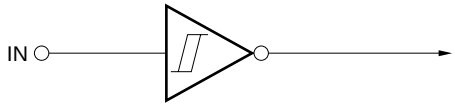
Note Applies to the μPD70F3017AY only.

Table 1-1. Types of Pin I/O Circuits (2/2)

Pin	Alternate Function	I/O Circuit Type	Recommended Connection of Unused Pins
P90	$\overline{LBEN}/\overline{WRL}$	5	Input: Connect to BV_{DD} or BV_{SS} Output: Leave open
P91	$\overline{UBEN}$		
P92	$R/\overline{W}/\overline{WRH}$		
P93	$\overline{DSTB}/\overline{RD}$		
P94	ASTB		
P95	$\overline{HLDAK}$		
P96	$\overline{HLDRQ}$		
P100 to P107	RTP0/A5 to RTP7/A12	26	Input: Connect to V_{DD} or V_{SS} Output: Leave open
P110 to P113	A1 to A4	5-A	
P114	XT1	16	
P120	$\overline{WAIT}$	5	Input: Connect to BV_{DD} or BV_{SS} Output: Leave open
AV_{REF}	–	–	Connect to AV_{SS}
CLKOUT	–	4	Leave open
$\overline{RESET}$	–	2	–
X2	–	–	Leave open (when external clock is input to X1 pin)
XT2	–	16	Leave open
V_{PP}	–	–	Connect to V_{SS}

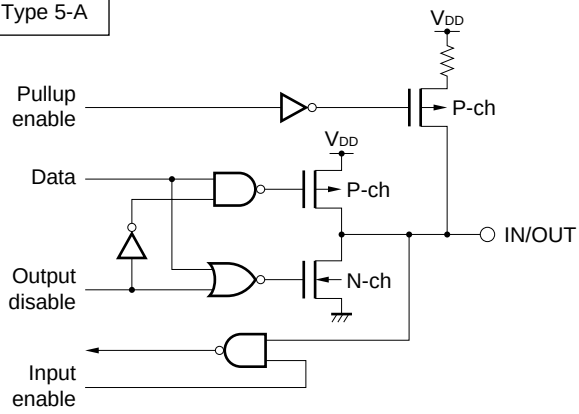
Figure 1-1. Pin Input/Output Circuits (1/2)

Type 2

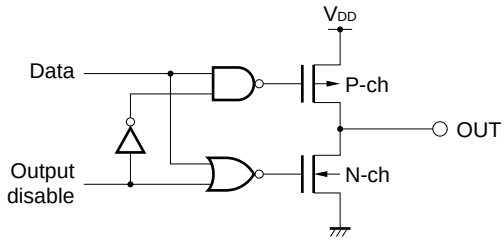


Schmitt-triggered input with hysteresis characteristics

Type 5-A

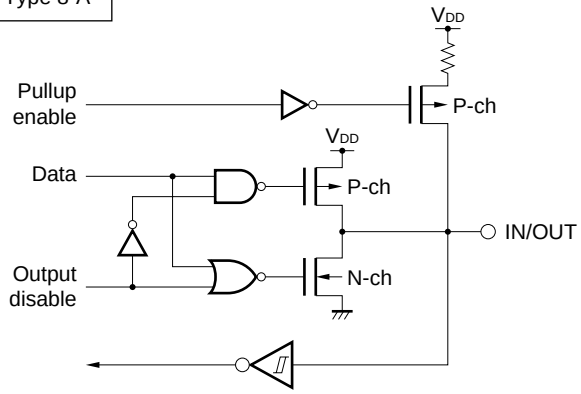


Type 4

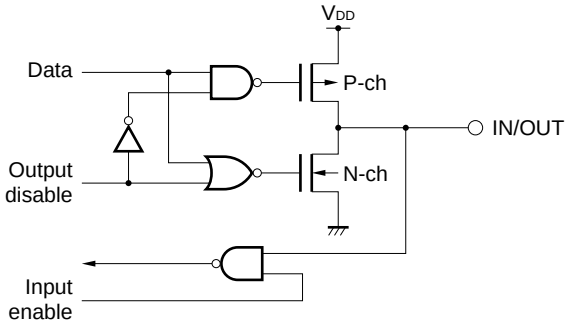


Push-pull output that can be set for high-impedance output (both P-ch and N-ch off)

Type 8-A



Type 5



Type 9

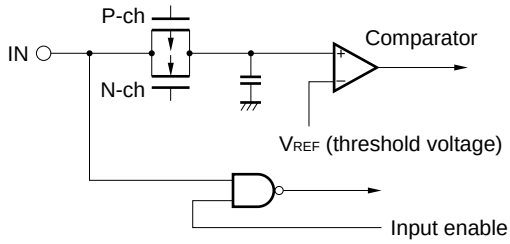
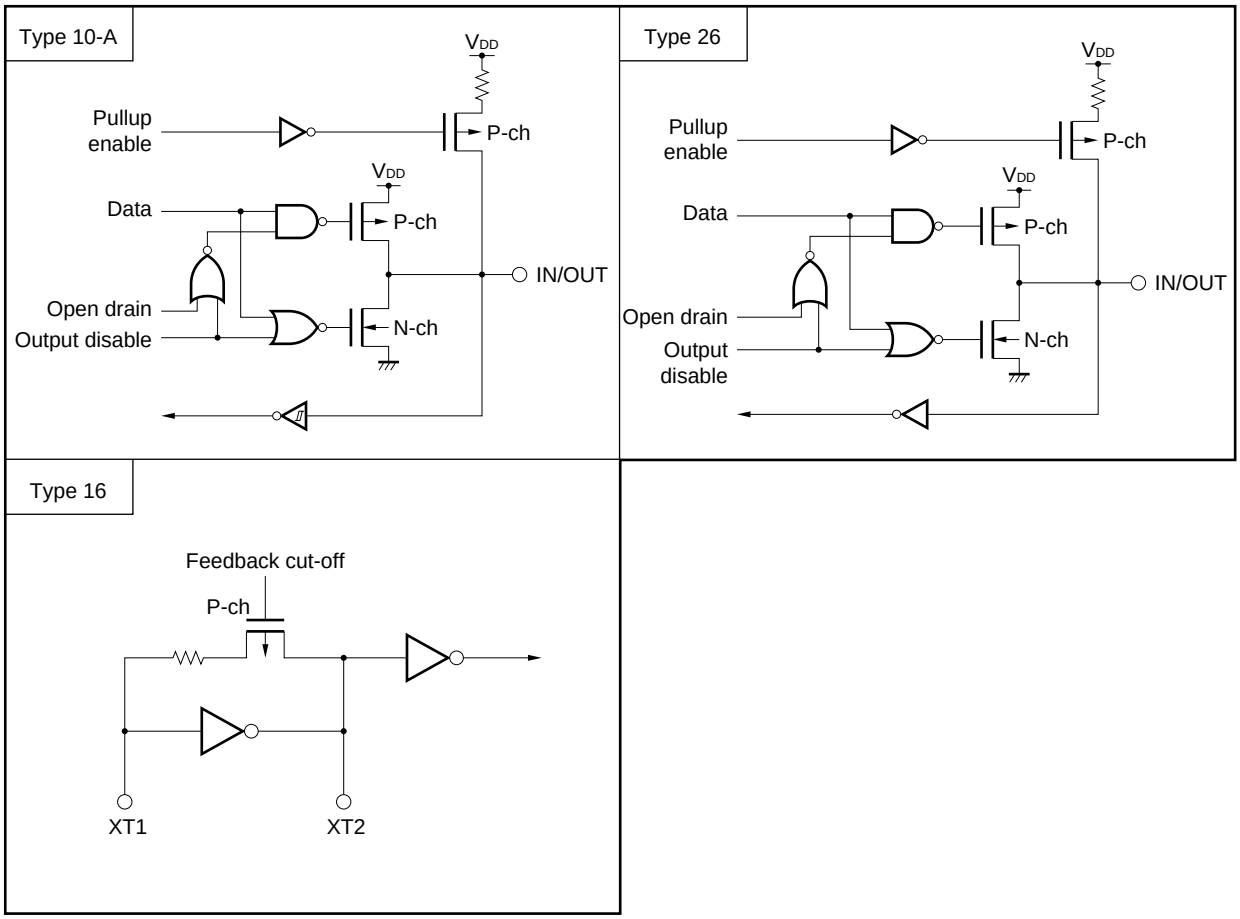


Figure 1-1. Pin Input/Output Circuits (2/2)



2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.5 to +4.6	V
	AV_{DD}		–0.5 to +4.6	V
	BV_{DD}		–0.5 to +4.6	V
	AV_{SS}		–0.5 to +0.5	V
	BV_{SS}		–0.5 to +0.5	V
Input voltage	V_{I1}	**Note 1**	–0.5 to V_{DD} + 0.5 Note 4	V
	V_{I2}	**Note 2**	–0.5 to BV_{DD} + 0.5 Note 4	V
	V_{I3}	V_{PP}	–0.5 to +8.5	V
Clock input voltage	V_K	X1, XT1, V_{DD} = 2.7 to 3.6 V	–0.5 to V_{DD} + 1.0 Note 4	V
Analog input voltage	V_{IAN}	**Note 3** (AV_{DD})	–0.5 to AV_{DD} + 0.5 Note 4	V
Analog reference input voltage	AV_{REF}	AV_{REF}	–0.5 to AV_{DD} + 0.5 Note 4	V
Output current, low	I_{OL}	Per pin	4.0	mA
		Total for P00 to P07, P10 to P15, P20 to P25	25	mA
		Total for P26, P27, P30 to P37, P100 to P107, P110 to P113	25	mA
		Total for P40 to P47, P90 to P96, P120, CLKOUT	25	mA
		Total for P50 to P57, P60 to P65	25	mA
Output current, high	I_{OH}	Per pin	–4.0	mA
		Total for P00 to P07, P10 to P15, P20 to P25	–25	mA
		Total for P26, P27, P30 to P37, P100 to P107, P110 to P113	–25	mA
		Total for P40 to P47, P90 to P96, P120, CLKOUT	–25	mA
		Total for P50 to P57, P60 to P65	–25	mA
Output voltage	V_{O1}	**Note 1**, V_{DD} = 2.7 to 3.6 V	–0.5 to V_{DD} + 0.5 Note 4	V
	V_{O2}	**Note 2**, BV_{DD} = 2.7 to 3.6 V	–0.5 to BV_{DD} + 0.5 Note 4	V
Operating ambient temperature	T_A	Normal operating mode	–40 to +85	°C
		Flash memory programming mode	10 to 40	°C
Storage temperature	T_{stg}		–40 to +125	°C

Notes 1. Ports 0, 1, 2, 3, 10, 11, 12, $\overline{\text{RESET}}$, and their alternate-function pins.

2. Ports 4, 5, 6, 9, CLKOUT, and their alternate-function pins.

3. Ports 7, 8, and their alternate-function pins.

4. Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

Cautions 1. Do not directly connect the output (or I/O) pins of IC products to each other, or to V_{DD}, V_{CC}, and GND. Open-drain pins or open-connector pins, however, can be directly connected to each other. Direct connection of the output pins between an IC product and an external circuit is possible, if the output pins can be set to the high-impedance state and the output timing of the external circuit is designed to avoid output conflict.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Capacitance (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz Unmeasured pins returned to 0 V			15	pF
I/O capacitance	C_{IO}				15	pF
Output capacitance	C_O				15	pF

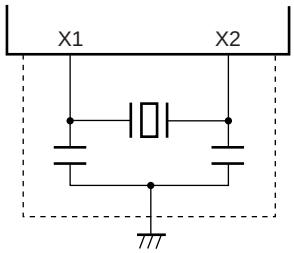
Operating Conditions

Internal Operation Clock Frequency (ϕ)	Supply Voltage (V_{DD})	Operating Ambient Temperature (T_A)
2 MHz ≤ f_{XX} ≤ 17 MHz	2.7 to 3.6 V	–40 to +85 °C
2 MHz ≤ f_{XX} ≤ 20 MHz	3.0 to 3.6 V	–40 to +85 °C
f_{XT} = 32.768 kHz	2.7 to 3.6 V	–40 to +85 °C

Recommended Oscillator

(1) Main system clock oscillator (T_A = –40 to +85 °C)

(a) Connection of ceramic resonator or crystal resonator



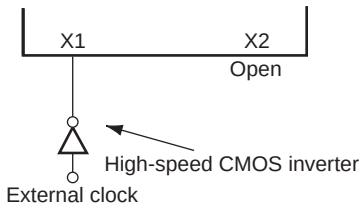
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★ Oscillation frequency	f_{XX}	V_{DD} = 2.7 to 3.6 V	2		17	MHz
		V_{DD} = 3.0 to 3.6 V	2		20	MHz
Oscillation stabilization time		Upon reset release		$2^{19}/f_{XX}$		s
		Upon STOP mode release		**Note**		s

Note The TYP value differs depending on the setting of the oscillation stabilization time select register (OSTS).

Caution Ensure that the duty of oscillation waveform is between 45% and 55%.

Remarks 1. Connect the oscillator as close as possible to the X1 and X2 pins.
2. Do not route the wiring near broken lines.
3. Sufficiently evaluate the matching between the oscillator and resonator.

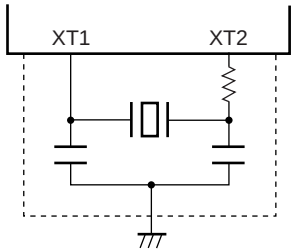
(b) External clock input



Cautions 1. Connect the high-speed CMOS inverter as close as possible to the X1 pin.
2. Sufficiently evaluate the matching between the μPD70F3017A, 70F3017AY and the high-speed CMOS inverter.

(2) Subsystem clock oscillator (T_A = –40 to +85 °C)

(a) Connection of crystal resonator



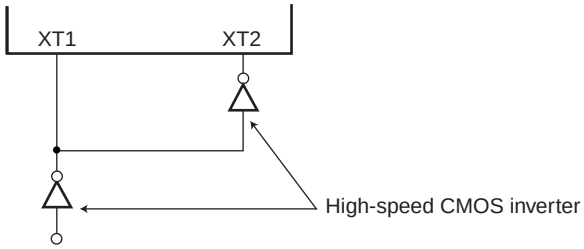
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation frequency	f_{XT}		32	32.768	35	kHz
Oscillation stabilization time				10		s

Remarks 1. Connect the oscillator as close as possible to the XT1 and XT2 pins.

2. Do not route the wiring near broken lines.

3. Sufficiently evaluate the matching between the oscillator and resonator.

(b) External clock input



Cautions 1. Connect the high-speed CMOS inverter as close as possible to the XT2 pin.

2. Sufficiently evaluate the matching between the μPD70F3017A, 70F3017AY and the high-speed CMOS inverter.

DC Characteristics

(1) Operating Conditions (T_A = –40 to +85 °C, V_{DD} = AV_{DD} = BV_{DD} = 2.7 to 3.6 V, V_{SS} = AV_{SS} = BV_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	Pins other than below		0.7V_{DD}		V_{DD}	V
	V_{IH2}	**Note 1**		0.7AV_{DD}		AV_{DD}	V
	V_{IH3}	**Note 2**		0.75V_{DD}		V_{DD}	V
	V_{IH4}	X1, XT1 (P114), XT2		0.8V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	Pins other than below		V_{SS}		0.3V_{DD}	V
	V_{IL2}	**Note 1**		AV_{SS}		0.3AV_{DD}	V
	V_{IL3}	**Note 2**		V_{SS}		0.2V_{DD}	V
	V_{IL4}	X1, XT1 (P114), XT2		V_{SS}		0.2V_{DD}	V
Output voltage, high	V_{OH1}	**Note 3**	I_{OH} = –3 mA	0.8V_{DD}			V
	V_{OH2}	**Note 4**	I_{OH} = –1 mA	0.8V_{DD}			V
Output voltage, low	V_{OL1}	**Note 3**	I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	**Note 4** (Except pins P10 and P12)	I_{OL} = 1.6 mA			0.4	V
	V_{OL3}	P10, P12	I_{OL} = 3 mA			0.4	V
Input leakage current, high	I_{LIH}	V_I = V_{DD} = AV_{DD} = BV_{DD}				5	μA
			X1, XT1, XT2			20	μA
Input leakage current, low	I_{LIL}	V_I = 0 V				–5	μA
			X1, XT1, XT2			–20	μA
Output leakage current, high	I_{LOH}	V_O = V_{DD} = AV_{DD} = BV_{DD}				5	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–5	μA
Supply current[Note 5]	I_{DD1}	Normal operation	f_{XX} = 17 MHz All peripheral functions operating		30	60	mA
	I_{DD2}	HALT mode	f_{XX} = 17 MHz All peripheral functions operating		10	25	mA
	I_{DD3}	IDLE mode	f_{XX} = 17 MHz Watch timer operating		4	8	mA
	I_{DD4}	STOP mode (subsystem oscillator, watch timer operating)			10	100	μA
		STOP mode (subsystem oscillator stopped (XT1 = V_{SS}))			2	100	μA

(1) Operating Conditions (T_A = –40 to +85 °C, V_{DD} = AV_{DD} = BV_{DD} = 2.7 to 3.6 V, V_{SS} = AV_{SS} = BV_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current[Note 5]	I_{DD5}	Subsystem clock normal operation mode f_{XT} = 32.768 kHz (main system clock stopped)		250	600	μA
	I_{DD6}	Subsystem clock IDLE mode f_{XT} = 32.768 kHz (main system clock stopped, watch timer operating)		130	360	μA
Pull-up resistance	R_L	V_{IN} = 0 V	10	30	100	kΩ

Notes 1. P70 to P77, P80 to P83, and their alternate-function pins.

2. P00 to P07, P10, P12, P13, P15, P20, P22, P23, P25 to P27, P30 to P33, P36, P37, $\overline{\text{RESET}}$, and their alternate-function pins.

3. CLKOUT, P40 to P47, P50 to P57, P60 to P65, P90 to P96, P120, and their alternate-function pins.

4. P00 to P07, P10 to P15, P20 to P27, P30 to P37, P100 to P107, P110 to P113, and their alternate-function pins.

5. The TYP value of V_{DD} is 3.3 V. The current consumed by the output buffer is not included.

(2) Operating Conditions (T_A = –40 to +85 °C, V_{DD} = AV_{DD} = BV_{DD} = 3.0 to 3.6 V, V_{SS} = AV_{SS} = BV_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	Pins other than below		0.7V_{DD}		V_{DD}	V
	V_{IH2}	**Note 1**		0.7AV_{DD}		AV_{DD}	V
	V_{IH3}	**Note 2**		0.75V_{DD}		V_{DD}	V
	V_{IH4}	X1, XT1 (P114), XT2		0.8V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	Pins other than below		V_{SS}		0.3V_{DD}	V
	V_{IL2}	**Note 1**		AV_{SS}		0.3AV_{DD}	V
	V_{IL3}	**Note 2**		V_{SS}		0.2V_{DD}	V
	V_{IL4}	X1, X2, XT1 (P114), XT2		V_{SS}		0.2V_{DD}	V
Output voltage, high	V_{OH1}	**Note 3**	I_{OH} = –3 mA	0.8V_{DD}			V
	V_{OH2}	**Note 4**	I_{OH} = –1 mA	0.8V_{DD}			V
Output voltage, low	V_{OL1}	**Note 3**	I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	**Note 4** (Except pins P10 and P12)	I_{OL} = 1.6 mA			0.4	V
	V_{OL3}	P10, P12	I_{OL} = 3 mA			0.4	V
Input leakage current, high	I_{LIH}	V_I = V_{DD} = AV_{DD} = BV_{DD}				5	μA
			X1, XT1, XT2			20	μA
Input leakage current, low	I_{LIL}	V_I = 0 V				–5	μA
			X1, XT1, XT2			–20	μA
Output leakage current, high	I_{LOH}	V_O = V_{DD}				5	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–5	μA
Supply current[Note 5]	I_{DD1}	Normal operation	f_{XX} = 20 MHz All peripheral functions operating		32	64	mA
	I_{DD2}	HALT mode	f_{XX} = 20 MHz All peripheral functions operating		11	26	mA
	I_{DD3}	IDLE mode	f_{XX} = 20 MHz Watch timer operating		4.5	9	mA
	I_{DD4}	STOP mode (subsystem oscillator, watch timer operating)			10	100	μA
		STOP mode (subsystem oscillator stopped (XT1 = V_{SS}))			2	100	μA

(2) Operating Conditions (T_A = –40 to +85 °C, V_{DD} = AV_{DD} = BV_{DD} = 3.0 to 3.6 V, V_{SS} = AV_{SS} = BV_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current[Note 5]	I_{DD5}	Subsystem clock normal operation mode f_{XT} = 32.768 kHz (main system clock stopped)		250	600	μA
	I_{DD6}	Subsystem clock IDLE mode f_{XT} = 32.768 kHz (main system clock stopped, watch timer operating)		130	360	μA
Pull-up resistance	R_L	V_{IN} = 0 V	10	30	100	kΩ

Notes 1. P70 to P77, P80 to P83, and their alternate-function pins.

2. P00 to P07, P10, P12, P13, P15, P20, P22, P23, P25 to P27, P30 to P33, P36, P37, $\overline{\text{RESET}}$ and their alternate-function pins.

3. CLKOUT, P40 to P47, P50 to P57, P60 to P65, P90 to P96, P120, and their alternate-function pins.

4. P00 to P07, P10 to P15, P20 to P27, P30 to P37, P100 to P107, P110 to P113, and their alternate-function pins.

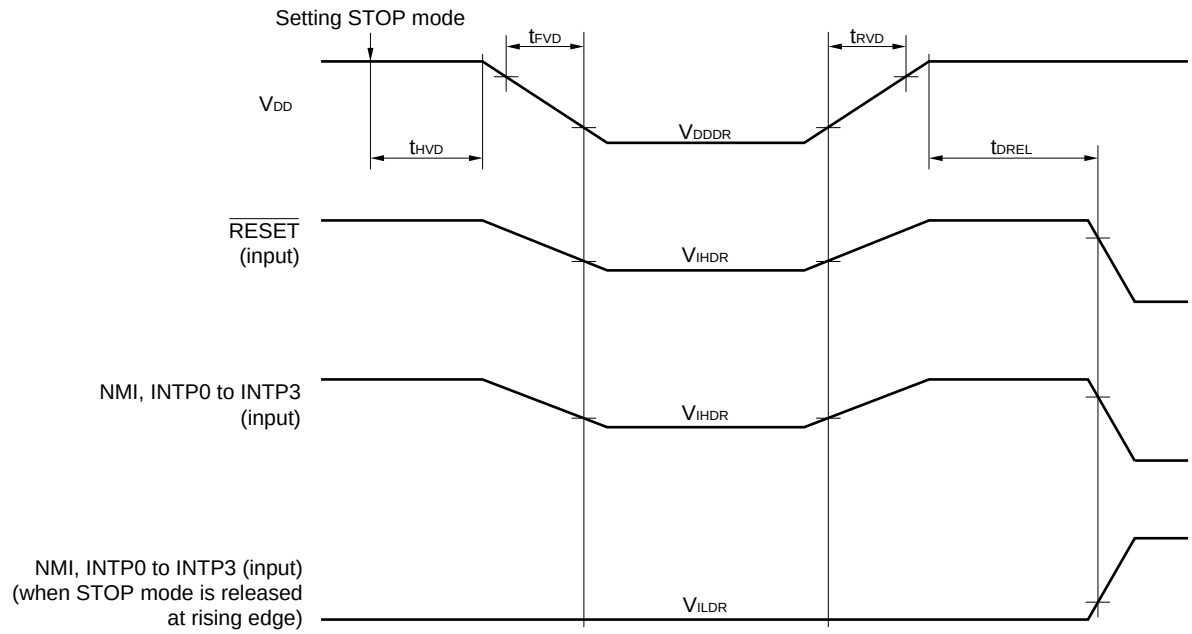
5. The TYP value of V_{DD} is 3.3 V. The current consumed by the output buffer is not included.

Data Retention Characteristics (T_A = –40 to +85 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	STOP mode	1.8		3.6	V
Data retention current	I_{DDDR}	V_{DDDR} [V]		2	100	μA
Supply voltage rise time	t_{RVD}		200			μs
Supply voltage fall time	t_{FVD}		200			μs
Supply voltage hold time (from STOP mode setting)	t_{HVD}		0			ms
STOP release signal input time	t_{DREL}		0			ms
Data retention high-level input voltage	V_{IHDR}	All input ports	V_{IHn}		V_{DDDR}	V
Data retention low-level input voltage	V_{ILDR}	All input ports	0		V_{ILn}	V

Remarks 1. TYP. values are reference values for when T_A = 25 °C.

2. n = 1 to 4

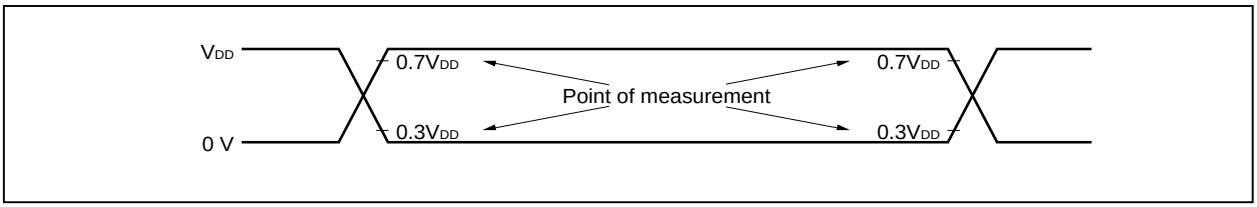


Caution Shifting to STOP mode and restoring from STOP mode must be performed at V_{DD} = 2.7 V min. (f_{XX} = 17 MHz) and V_{DD} = 3.0 V min. (f_{XX} = 20 MHz), respectively.

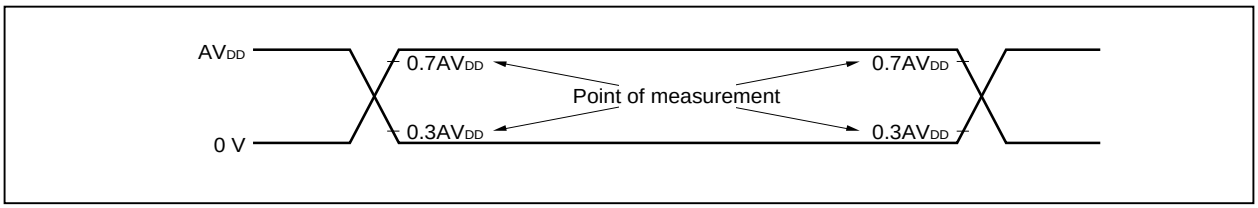
AC Characteristics

AC Test Input Waveforms

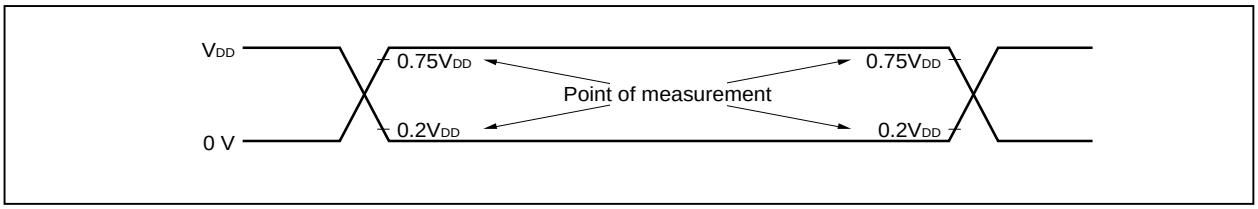
(1) P11, P14, P21, P24, P34, P35, P100 to P107, P110 to P113, and their alternate-function pins



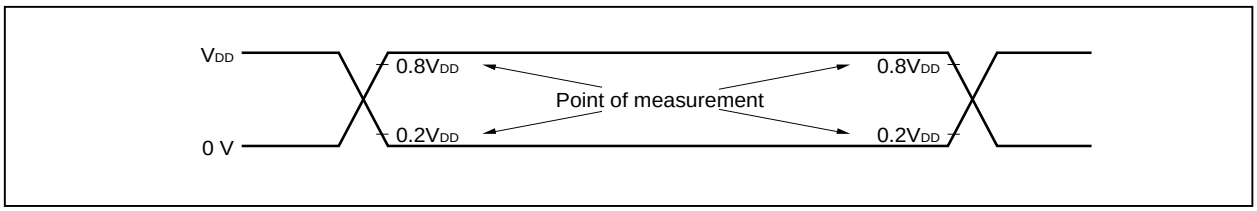
(2) P70 to P77, P80 to P83, and their alternate-function pins



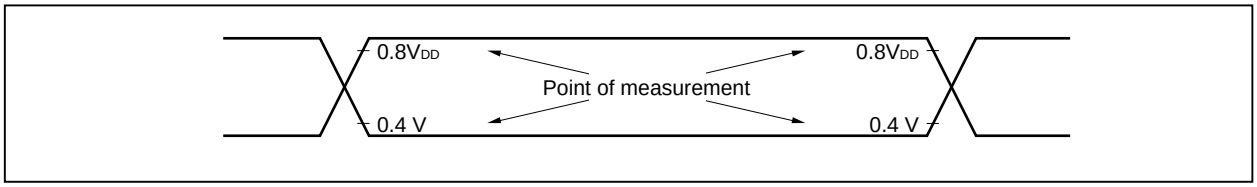
(3) P00 to P07, P10, P12, P13, P15, P20, P22, P23, P25 to P27, P30 to P33, P36, P37, $\overline{\text{RESET}}$, and their alternate-function pins



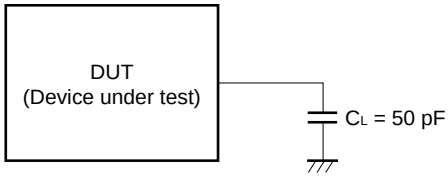
(4) X1, XT1 (P114), XT2



AC Test Output Measurement Points



Load conditions



Caution If the load capacitance exceeds 50 pF due to the circuit configuration, bring the load capacitance of the device to 50 pF or less by inserting a buffer or by some other means.

Clock Timing

(1) Operating Conditions (T_A = –40 to +85 °C, V_{DD} = BV_{DD} = 2.7 to 3.6 V, V_{SS} = BV_{SS} = 0 V, Output pin load capacitance: C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
X1 input cycle	t_{CYX}	<1>		58.8		ns
XT1 input cycle				28.5		μs
X1 input high-level width	t_{WXH}	<2>		26.4		ns
XT1 input high-level width				12.8		μs
X1 input low-level width	t_{WXL}	<3>		26.4		ns
XT1 input low-level width				12.8		μs
X1 input rise time	t_{XR}	<4>			0.5 (t_{CYX} – t_{WXH} – t_{WXL})	ns
X1 input fall time	t_{XF}	<5>			0.5 (t_{CYX} – t_{WXH} – t_{WXL})	ns
CLKOUT output cycle	t_{CYK}	<6>		58.8 ns	31.2 μs	
CLKOUT high-level width	t_{WKH}	<7>		0.4t_{CYK} – 10		ns
CLKOUT low-level width	t_{WKL}	<8>		0.4t_{CYK} – 10		ns
CLKOUT rise time	t_{KR}	<9>			10	ns
CLKOUT fall time	t_{KF}	<10>			10	ns

Remarks 1. T = t_{CYK}

2. Ensure that the duty is between 45% and 55%.

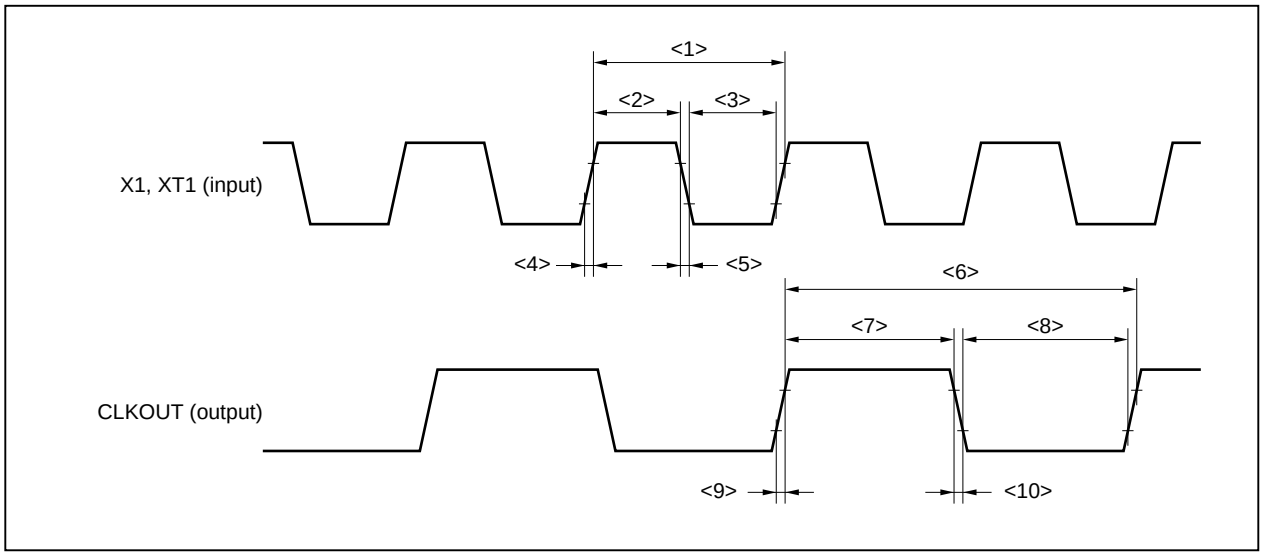
(2) Operating Conditions (T_A = –40 to +85 °C, V_{DD} = BV_{DD} = 3.0 to 3.6 V, V_{SS} = BV_{SS} = 0 V, Output pin load capacitance: C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
X1 input cycle	t_{CYX}	<1>		50.0		ns
XT1 input cycle				28.5		μs
X1 input high-level width	t_{WXH}	<2>		22.5		ns
XT1 input high-level width				12.8		μs
X1 input low-level width	t_{WXL}	<3>		22.5		ns
XT1 input low-level width				12.8		μs
X1 input rise time	t_{XR}	<4>			0.5 (t_{CYX} – t_{WXH} – t_{WXL})	ns
X1 input fall time	t_{XF}	<5>			0.5 (t_{CYX} – t_{WXH} – t_{WXL})	ns
CLKOUT output cycle	t_{CYK}	<6>		50.0 ns	31.2 μs	
CLKOUT high-level width	t_{WKH}	<7>		0.4t_{CYK} – 10		ns
CLKOUT low-level width	t_{WKL}	<8>		0.4t_{CYK} – 10		ns
CLKOUT rise time	t_{KR}	<9>			10	ns
CLKOUT fall time	t_{KF}	<10>			10	ns

Remarks 1. T = t_{CYK}

2. Ensure that the duty is between 45% and 55%.

Clock Timing



(1) Timing of pins other than CLKOUT, ports 4, 5, 6, and 9

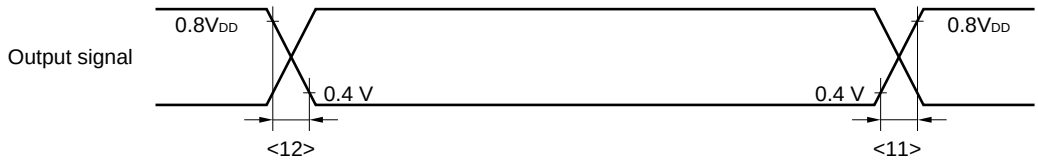
(T_A = –40 to +85 °C, V_{DD} = BV_{DD} = 2.7 to 3.6 V, V_{SS} = BV_{SS} = 0 V, Output pin load capacitance: C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Output rise time	t_{OR}	<11>			20	ns
Output fall time	t_{OF}	<12>			20	ns

(2) Timing of pins other than CLKOUT, ports 4, 5, 6, and 9

(T_A = –40 to +85 °C, V_{DD} = BV_{DD} = 3.0 to 3.6 V, V_{SS} = BV_{SS} = 0 V, Output pin load capacitance: C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Output rise time	t_{OR}	<11>			20	ns
Output fall time	t_{OF}	<12>			20	ns



Bus Timing (CLKOUT Asynchronous)

(T_A = –40 to +85 °C, V_{DD} = BV_{DD} = 2.7 to 3.6 V, V_{SS} = BV_{SS} = 0 V, Output pin load capacitance: C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address setup time (to ASTB↓)	t_{SAST}	<13>		0.5T – 15		ns
Address hold time (from ASTB↓)	t_{HSTA}	<14>		0.5T – 15		ns
Address float from $\overline{DSTB}$↓	t_{FDA}	<15>			2	ns
Data input setup time from address	t_{SAID}	<16>			(2 + n)T – 25	ns
Data input setup time from $\overline{DSTB}$↓	t_{SDID}	<17>			(1 + n)T – 25	ns
Delay time from ASTB↓ to $\overline{DSTB}$↓	t_{DSTD}	<18>		0.5T – 15		ns
Data input hold time (from $\overline{DSTB}$↑)	t_{HDID}	<19>		0		ns
Address output time from $\overline{DSTB}$↑	t_{DDA}	<20>		(1 + i)T – 15		ns
Delay time from $\overline{DSTB}$↑ to ASTB↑	t_{DDST1}	<21>		0.5T – 15		ns
Delay time from $\overline{DSTB}$↑ to ASTB↓	t_{DDST2}	<22>		(1.5 + i)T – 15		ns
$\overline{DSTB}$ low-level width	t_{WDL}	<23>		(1 + n)T – 15		ns
ASTB high-level width	t_{WSTH}	<24>		T – 15		ns
Data output time from $\overline{DSTB}$↓	t_{DDOD}	<25>			15	ns
Data output setup time (to $\overline{DSTB}$↑)	t_{SODD}	<26>		(1 + n)T – 20		ns
Data output hold time (from $\overline{DSTB}$↑)	t_{HDOD}	<27>		T – 15		ns
$\overline{WAIT}$ setup time (to address)	t_{SAWT1}	<28>	n ≥ 1		1.5T – 25	ns
	t_{SAWT2}	<29>	n ≥ 1		(1.5 + n)T – 25	ns
$\overline{WAIT}$ hold time (from address)	t_{HAWT1}	<30>	n ≥ 1	(0.5 + n)T		ns
	t_{HAWT2}	<31>	n ≥ 1	(1.5 + n)T		ns
$\overline{WAIT}$ setup time (to ASTB↓)	t_{SSTWT1}	<32>	n ≥ 1		T – 25	ns
	t_{SSTWT2}	<33>	n ≥ 1		(1 + n)T – 25	ns
$\overline{WAIT}$ hold time (from ASTB↓)	t_{HSTWT1}	<34>	n ≥ 1	nT		ns
	t_{HSTWT2}	<35>	n ≥ 1	(1 + n)T		ns
$\overline{HLDRQ}$ high-level width	t_{WHQH}	<36>		T + 10		ns
$\overline{HLDAK}$ low-level width	t_{WHAL}	<37>		T – 15		ns
Bus output delay time from $\overline{HLDAK}$↑	t_{DHAC}	<38>		0		ns
Delay time from $\overline{HLDRQ}$↓ to $\overline{HLDAK}$↓	t_{DHQHA1}	<39>			(2n + 7.5)T + 25	ns
Delay time from $\overline{HLDRQ}$↑ to $\overline{HLDAK}$↑	t_{DHQHA2}	<40>		0.5T	1.5T + 25	ns

Remarks 1. T = 1/f_{CPU} (f_{CPU}: CPU operation clock frequency)

2. n: Number of wait clocks inserted in the bus cycle.
The sampling timing changes when a programmable wait is inserted.

3. i: Number of idle states inserted after the read cycle (0 or 1).

4. The values in the above specifications are values for when clocks with a 5:5 duty ratio are input from X1.

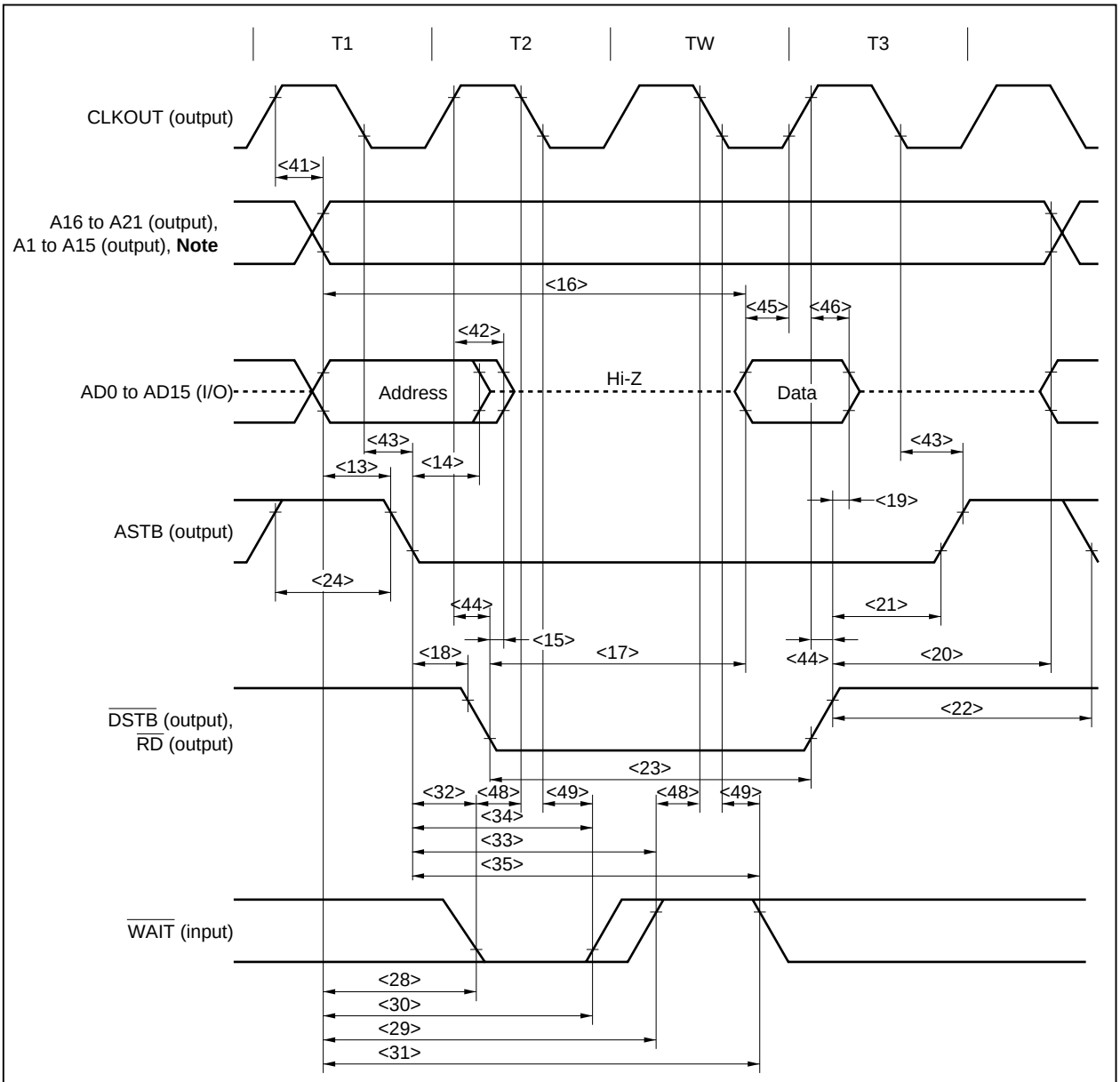
Bus Timing (CLKOUT Synchronous)

(T_A = –40 to +85 °C, V_{DD} = BV_{DD} = 2.7 to 3.6 V, V_{SS} = BV_{SS} = 0 V, Output pin load capacitance: C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address	t_{DKA}	<41>		0	19	ns
Delay time from CLKOUT↑ to address float	t_{FKA}	<42>		–12	7	ns
Delay time from CLKOUT↓ to ASTB	t_{DKST}	<43>		–12	7	ns
Delay time from CLKOUT↑ to $\overline{DSTB}$	t_{DKD}	<44>		–5	14	ns
Data input setup time (to CLKOUT↑)	t_{SIDK}	<45>		15		ns
Data input hold time (from CLKOUT↑)	t_{HKID}	<46>		5		ns
Data output delay time from CLKOUT↑	t_{DKOD}	<47>			19	ns
$\overline{WAIT}$ setup time (to CLKOUT↓)	t_{SWTK}	<48>		15		ns
$\overline{WAIT}$ hold time (from CLKOUT↓)	t_{HKWT}	<49>		5		ns
$\overline{HLDRQ}$ setup time (to CLKOUT↓)	t_{SHQK}	<50>		15		ns
$\overline{HLDRQ}$ hold time (from CLKOUT↓)	t_{HKHQ}	<51>		5		ns
Delay time from CLKOUT↑ to bus float	t_{DKF}	<52>			19	ns
Delay time from CLKOUT↑ to $\overline{HLDAK}$	t_{DKHA}	<53>			19	ns

Remark The values in the above specifications are values for when clocks with a 5:5 duty ratio are input from X1.

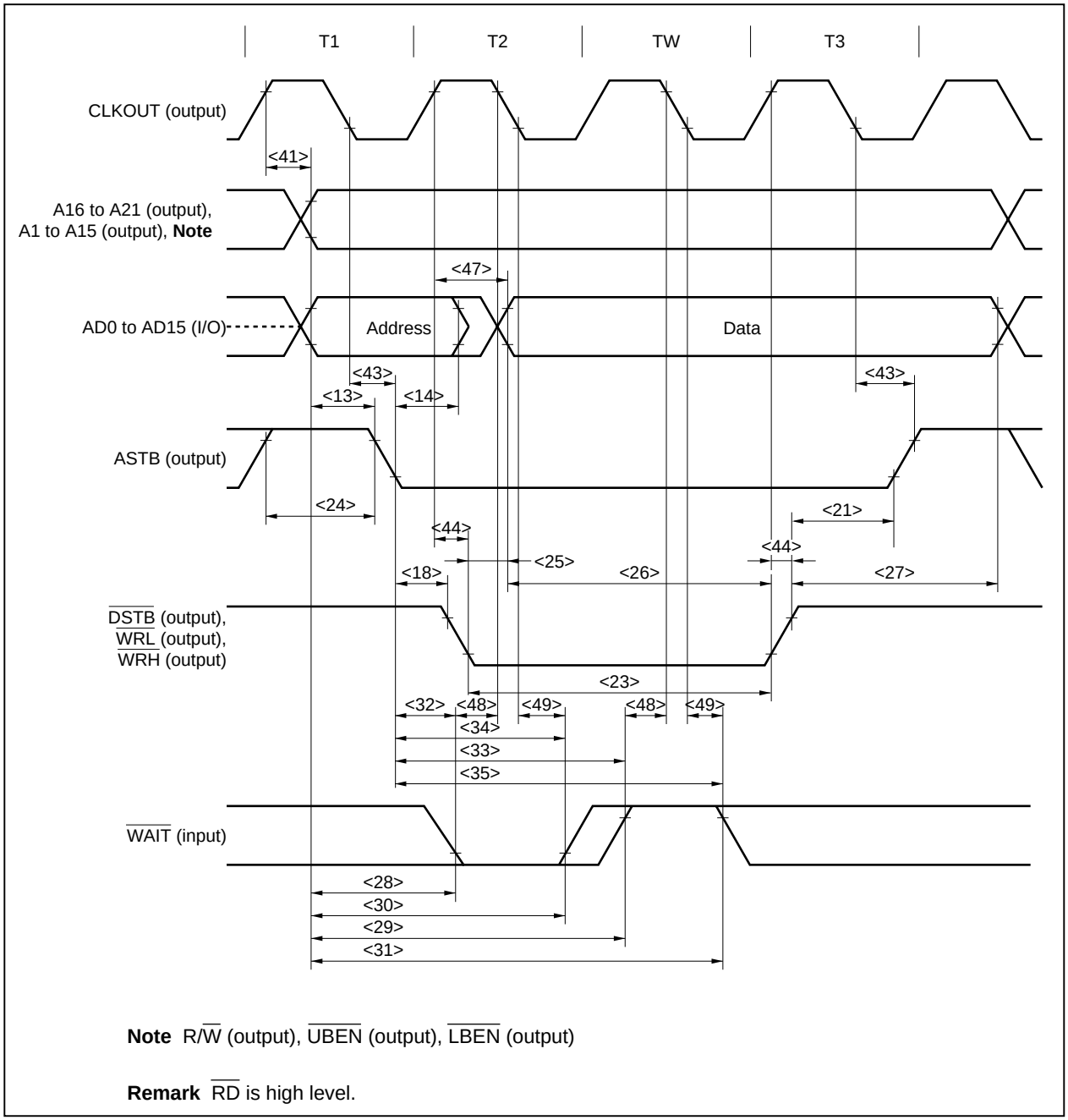
Read Cycle (CLKOUT Synchronous/Asynchronous, 1 Wait)



Note R/$\overline{W}$ (output), $\overline{UBEN}$ (output), $\overline{LBEN}$ (output)

Remark $\overline{WRL}$ and $\overline{WRH}$ are high level.

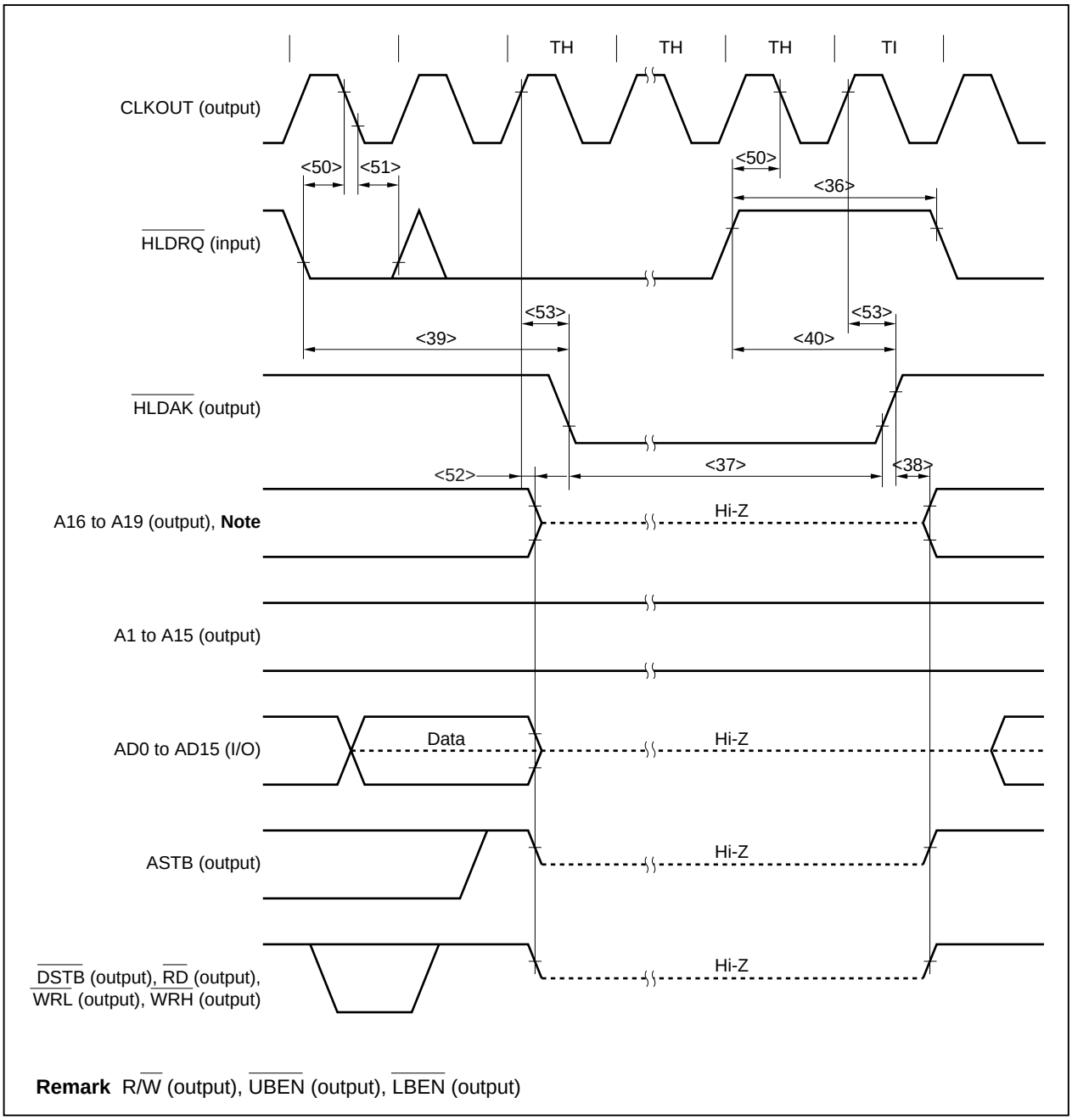
Write Cycle (CLKOUT Synchronous/Asynchronous, 1 Wait)



Note R/$\overline{W}$ (output), $\overline{UBEN}$ (output), $\overline{LBEN}$ (output)

Remark $\overline{RD}$ is high level.

Bus Hold



Remark R/W (output), UBEN (output), LBEN (output)

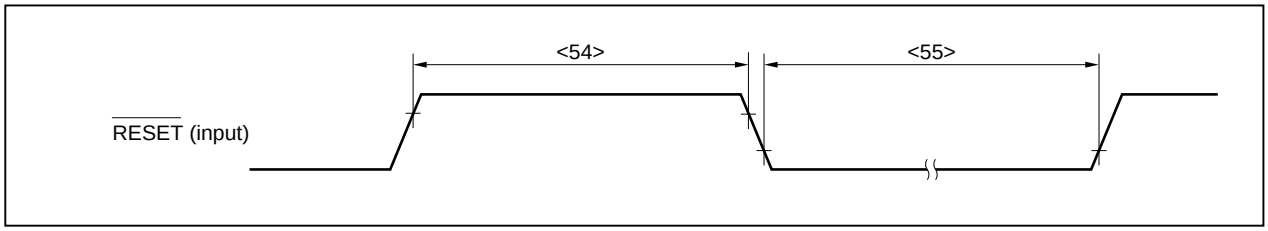
Reset/Interrupt Timing

(T_A = –40 to +85 °C, V_{DD} = BV_{DD} = 2.7 to 3.6 V, V_{SS} = BV_{SS} = 0 V, Output pin load capacitance: C_L = 50 pF)

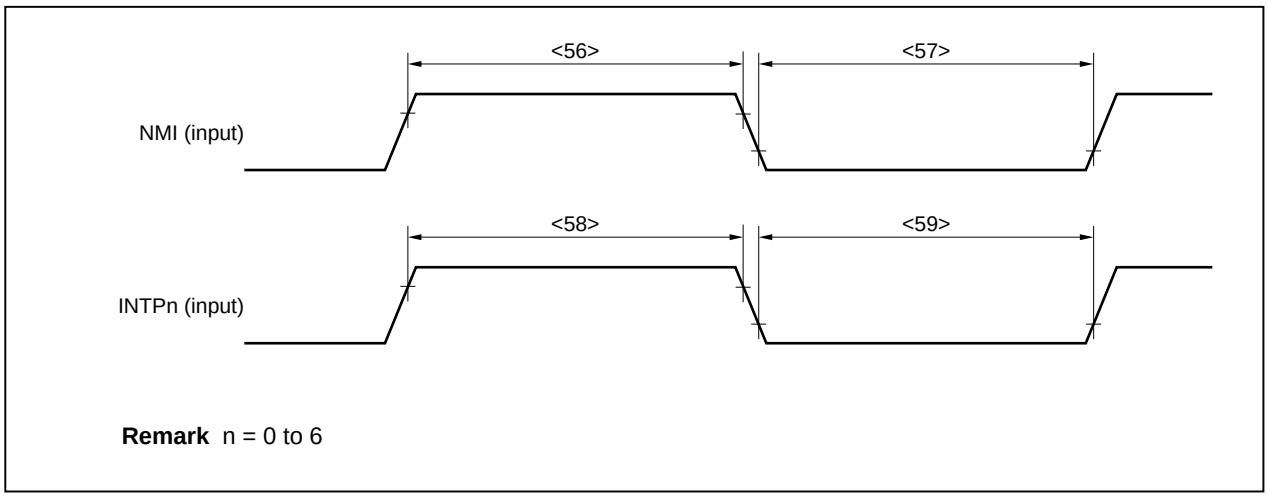
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ high-level width	t_{WRSH}	<54>		500		ns
$\overline{\text{RESET}}$ low-level width	t_{WRSL}	<55>		500		ns
NMI high-level width	t_{WNIH}	<56>		500		ns
NMI low-level width	t_{WNIL}	<57>		500		ns
INTPn high-level width	t_{WITH}	<58>	n = 0 to 3 (analog noise elimination)	500		ns
			n = 4 to 6 (digital noise elimination)	3T + 20		ns
INTPn low-level width	t_{WITL}	<59>	n = 0 to 3 (analog noise elimination)	500		ns
			n = 4 to 6 (digital noise elimination)	3T + 20		ns

Remark T = 1/f_{XX}

Reset



Interrupt



Remark n = 0 to 6

TIn Input Timing

(T_A = –40 to +85 °C, V_{DD} = BV_{DD} = 2.7 to 3.6 V, V_{SS} = BV_{SS} = 0 V, Output pin load capacitance: C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
TIn0, TIn1 high-level width	t_{TIHn}	<60>	n = 0, 1	$2T_{sam}$ + 20[Note]		ns
TIn high-level width			n = 2 to 5	3T + 20		ns
TIn0, TIn1 low-level width	t_{TILn}	<61>	n = 0, 1	$2T_{sam}$ + 20[Note]		ns
TIn low-level width			n = 2 to 5	3T + 20		ns

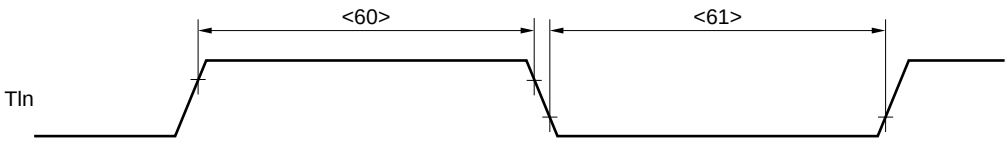
Note T_{sam} (count clock cycle) can be selected as follows by setting the PRMn2 to PRMn0 bits of prescaler mode register n, n1 (PRMn, PRMn1).

When n = 0 (TM0): T_{sam} = 2T, 4T, 16T, 64T, 256T or 1/INTWTI cycle

When n = 1 (TM1): T_{sam} = 2T, 4T, 16T, 32T, 128T, or 256T cycle

★ However, when the TIn0 valid edge is selected as the count clock cycle, T_{sam} = 2T.

Remark T= 1/f_{XX}



Remark n = 00, 01, 10, 11, 2 to 5

CSI Timing

(1) Master mode (T_A = –40 to +85 °C, V_{DD} = BV_{DD} = 2.7 to 3.6 V, V_{SS} = BV_{SS} = 0 V, Output pin load capacitance: C_L = 50 pF)

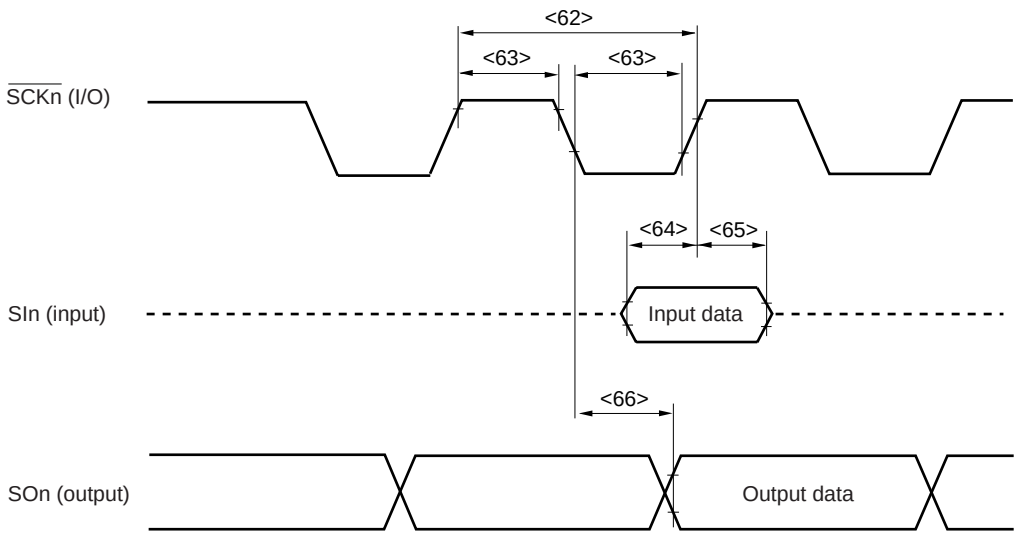
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle time	t_{KCY1}	<62>		400		ns
$\overline{SCKn}$ high-/low-level width	t_{KH1}, t_{KL1}	<63>		140		ns
SIn setup time (to $\overline{SCKn}$↑)	t_{SIK1}	<64>		50		ns
SIn hold time (from $\overline{SCKn}$↑)	t_{KSI1}	<65>		50		ns
Delay time from $\overline{SCKn}$↓ to SOn output	t_{KSO1}	<66>			60	ns

Remark n = 0 to 2

(2) Slave mode (T_A = –40 to +85 °C, V_{DD} = BV_{DD} = 2.7 to 3.6 V, V_{SS} = BV_{SS} = 0 V, Output pin load capacitance: C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle time	t_{KCY2}	<62>		400		ns
$\overline{SCKn}$ high-/low-level width	t_{KH2}, t_{KL2}	<63>		140		ns
SIn setup time (to $\overline{SCKn}$↑)	t_{SIK2}	<64>		50		ns
SIn hold time (from $\overline{SCKn}$↑)	t_{KSI2}	<65>		50		ns
Delay time from $\overline{SCKn}$↓ to SOn output	t_{KSO2}	<66>			60	ns

Remark n = 0 to 2

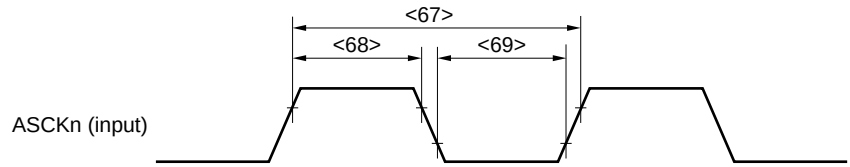


Remark n = 0 to 2

UART Timing (T_A = –40 to +85 °C, V_{DD} = BV_{DD} = 2.7 to 3.6 V, V_{SS} = BV_{SS} = 0 V, Output pin load capacitance: C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
ASCKn cycle time	t_{KCY13}	<67>		200		ns
ASCKn high-level width	t_{KH13}	<68>		80		ns
ASCKn low-level width	t_{KL13}	<69>		80		ns

Remark n = 0 or 1



Remark n = 0 or 1

I²C Bus Mode (μPD70F3017AY only)

(T_A = –40 to +85 °C, V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V)

Parameter		Symbol		Normal Mode		High-Speed Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCL clock frequency		f_{CLK}		0	100	0	400	kHz
Bus-free time (between stop/start conditions)		t_{BUF}	<70>	4.7	–	1.3	–	μs
Hold time[Note 1]		$t_{HD:STA}$	<71>	4.0	–	0.6	–	μs
SCL clock low-level width		t_{LOW}	<72>	4.7	–	1.3	–	μs
SCL clock high-level width		t_{HIGH}	<73>	4.0	–	0.6	–	μs
Setup time for start/restart condition		$t_{SU:STA}$	<74>	4.7	–	0.6	–	μs
Data hold time	CBUS compatible master	$t_{HD:DAT}$	<75>	5.0	–	–	–	μs
	I²C mode			0[Note 2]	–	0[Note 2]	0.9[Note 3]	μs
Data setup time		$t_{SU:DAT}$	<76>	250	–	100[Note 4]	–	ns
SDA and SCL signal rise time		t_R	<77>	–	1,000	20 + 0.1Cb[Note 5]	300	ns
SDA and SCL signal fall time		t_F	<78>	–	300	20 + 0.1Cb[Note 5]	300	ns
Stop condition setup time		$t_{SU:STO}$	<79>	4.0	–	0.6	–	μs
Capacitance load of each bus line		Cb		–	400	–	400	pF

Notes 1. At the start condition, the first clock pulse is generated after the hold time.

2. The system requires a minimum of 300 ns hold time internally for the SDA signal in order to occupy the undefined area at the falling edge of SCL.

3. If the system does not extend the SCL signal low hold time (t_{LOW}), only the maximum data hold time ($t_{HD:DAT}$) needs to be satisfied.

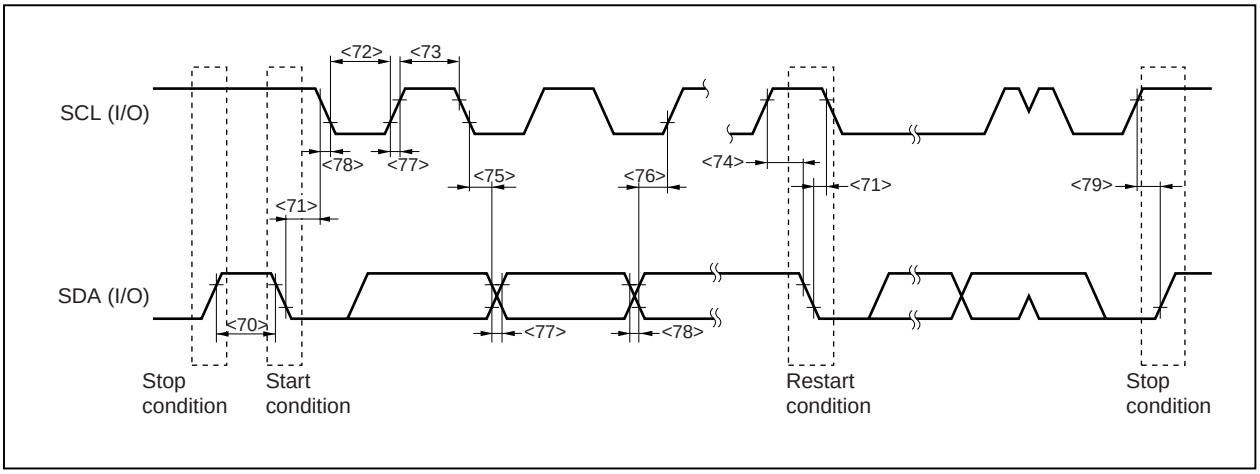
4. The high-speed mode I²C bus can be used in the normal-mode I²C bus system. In this case, set the high-speed mode I²C bus so that it meets the following conditions.

- If the system does not extend the SCL signal's low state hold time:
  $t_{SU:DAT} \geq 250$ ns
- If the system extends the SCL signal's low state hold time:
  Transmit the following data bit to the SDA line prior to the SCL line release ($t_{Rmax.} + t_{SU:DAT}$ = 1,000 + 250 = 1,250 ns: Normal mode I²C bus specification).

5. Cb: Total capacitance of one bus line (unit: pF)

Remark The maximum operating frequency of the μPD70F3017AY is 17 MHz.

I²C Bus Mode (μPD70F3017AY only)



A/D Converter

(T_A = –40 to +85 °C, V_{DD} = AV_{DD} = AV_{REF} = 2.7 to 3.6 V, V_{SS} = AV_{SS} = 0 V, Output pin load capacitance: C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error Note 1					±0.8	%FSR
Conversion time	t_{CONV}		5		100	μs
Zero-scale error Note 1					±0.4	%FSR
Full-scale error Note 1					±0.4	%FSR
Integral linearity error Note 2					±4	LSB
Differential linearity error Note 2					±4	LSB
Analog reference voltage	AV_{REF}	AV_{REF} = AV_{DD}	2.7		3.6	V
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
AV_{REF} current	AI_{REF}			360	500	μA
Power supply current	AI_{DD}			1	3	mA

Notes 1. Excluding quantization error (±0.05% FSR).

2. Excluding quantization error (±0.5 LSB)

Remark LSB: Least Significant Bit

FSR: Full Scale Range

Flash Memory Programming Mode

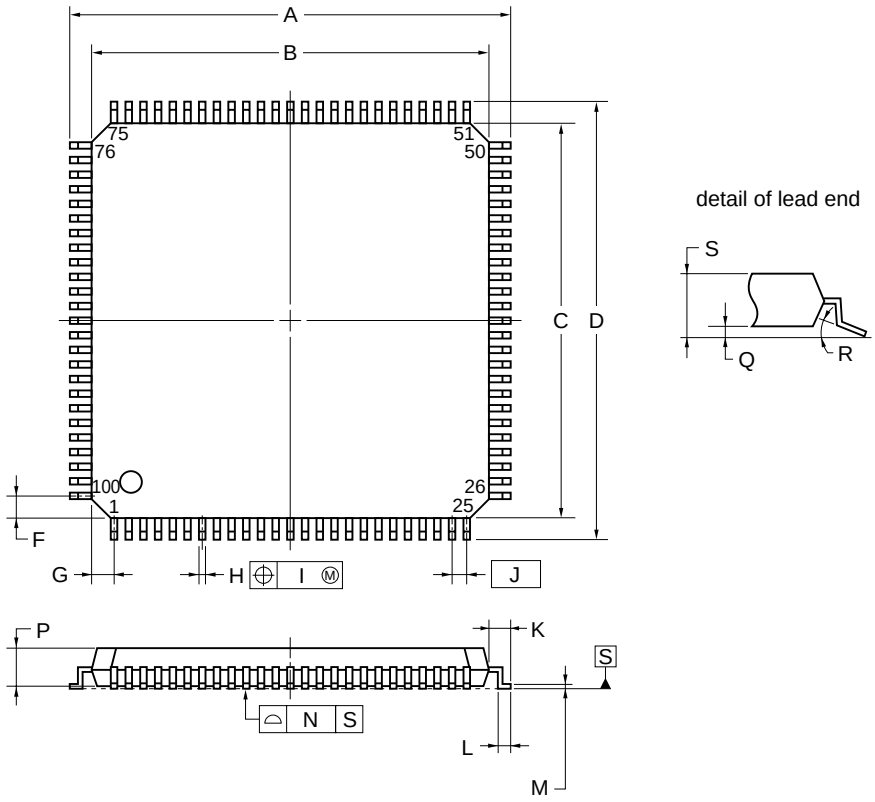
Write/erase characteristics (T_A = 10 to 40 °C, V_{DD} = 3.0 to 3.6 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Write current	I_{DDW}	When $V_{PP} = V_{PP1}$	V_{DD} pin			67	mA
	I_{PPW}		V_{PP} pin			100	mA
Erase current	I_{DDE}	When $V_{PP} = V_{PP1}$	V_{DD} pin			67	mA
	I_{PPE}		V_{PP} pin			200	mA
Unit erase time	t_{ER}			0.2	0.2	0.2	s
Total erase time	t_{ERT}					20	s
Number of rewrites[Note]				20			Times
V_{PP} supply voltage	V_{PP0}	During normal operation		0		$0.2V_{DD}$	V
	V_{PP1}	In flash memory programming mode		7.5	7.8	8.1	V
Operating frequency				2		20	MHz

Note Write/erase is regarded as one cycle.
Operations of the μPD70F3017A and 70F3017AY are unpredictable if flash memory is rewritten more than 20 times.

★ 3. PACKAGE DRAWINGS

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



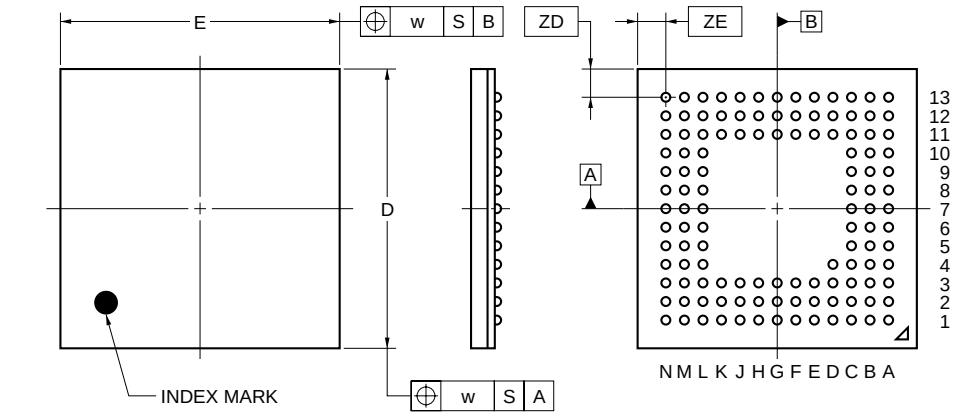
NOTE

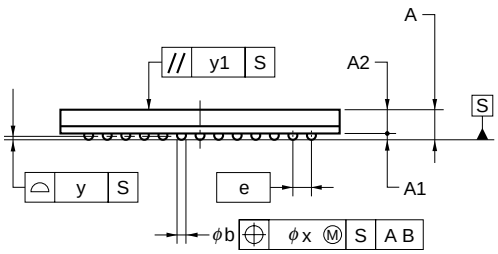
Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	16.00±0.20
B	14.00±0.20
C	14.00±0.20
D	16.00±0.20
F	1.00
G	1.00
H	$0.22^{+0.05}_{-0.04}$
I	0.08
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.40±0.05
Q	0.10±0.05
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.60 MAX.

S100GC-50-8EU, 8EA-2

121-PIN PLASTIC FBGA (12x12)





ITEM	MILLIMETERS
D	12.00±0.10
E	12.00±0.10
w	0.20
A	1.48±0.10
A1	0.35±0.06
A2	1.13
e	0.80
b	$0.50^{+0.05}_{-0.10}$
x	0.08
y	0.10
y1	0.20
ZD	1.20
ZE	1.20

P121F1-80-EA6

4. RECOMMENDED SOLDERING CONDITIONS

The μPD70F3017A and 70F3017AY should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E).**

For soldering methods and conditions other than those recommended below, contact your sales representative.

Table 4-1. Surface Mounting Type Soldering Conditions

(1) μPD70F3017AGC-8EU: 100-pin plastic LQFP (fine-pitch) (14 × 14 mm)
μPD70F3017AYGC-8EU: 100-pin plastic LQFP (fine-pitch) (14 × 14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C, Time: 30 seconds max. (at 210 °C or higher), Count: Two times or less Exposure limit: 7 days[Note] (after that, prebake at 125 °C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215 °C, Time: 40 seconds max. (at 200 °C or higher), Count: Two times or less Exposure limit: 7 days[Note] (after that, prebake at 125 °C for 10 hours)	VP15-107-2
Partial heating	Pin temperature: 300 °C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25 °C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

★ **(2) μPD70F3017AF1-EA6: 121-pin plastic FBGA (12 × 12 mm)**
μPD70F3017AYF1-EA6: 121-pin plastic FBGA (12 × 12 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C, Time: 30 seconds max. (at 210 °C or higher), Count: Two times or less Exposure limit: 7 days[Note] (after that, prebake at 125 °C for 10 hours)	IR35-107-2
Partial heating	Pin temperature: 300 °C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25 °C or less and 65% RH or less for the allowable storage period.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Caution The μPD70F3017AY contains an I^2C bus interface circuit.
Purchase of NEC I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, pIease contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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Reference document Electrical Characteristics for Microcomputer (IEI-601)[Note]

Note This document number is that of the Japanese version.

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