DATA SHEET

NEC

MOS INTEGRATED CIRCUIT
μPD75064, 75066, 75068, 75064(A), 75066(A), 75068(A)

4-BIT SINGLE-CHIP MICROCOMPUTER

The μPD75068 is a member of the 75X series of 4-bit single-chip microcomputers.

The minimum instruction execution time of the μPD75068's CPU is 0.95 μs. In addition to this high-speed capability, the chip contains an A/D converter and furnishes high-performance functions such as the serial bus interface (SBI) function compliant with the NEC standard format, providing powerful features and high cost performance. The μPD75068(A) is a high-reliability version of the μPD75068.

NEC also provides PROM versions suitable for small-scale production or evaluation samples in system development. The μPD75P068 is the PROM version for the μPD75064, 75066, 75068, and the μPD75P068(A) is that for the μPD75064(A), 75066(A), 75068(A).

The detailed function descriptions are described in the document below. Please make sure to read this document before starting design.

μPD75068 User's Manual: IEU-1366

FEATURES

- Variable instruction execution time advantageous to high-speed operation and power-saving:
  - 0.95 μs, 1.91 μs, or 15.3 μs (at 4.19 MHz with the main system clock selected)
  - 122 μs (at 32.768 kHz with the subsystem clock selected)
- A/D converter (8-bit resolution, successive approximation): 8 channels
  - Capable of low-voltage operation: V_{DD} = 2.7 to 6.0 V
- Timer function: 3 channels
- On-chip NEC standard serial bus interface (SBI)
- Very low-power watch operation enabled (5 μA TYP. at 3 V)
- Pull-up resistor option allowed for 27 I/O lines
- The μPD75P068 and 75P068(A) (PROM versions) available: Capable of low-voltage operation (V_{DD} = 2.7 to 6.0 V)

APPLICATIONS

- μPD75064, 75066, 75068
  Home electronic appliances, air conditioners, cameras, and electronic measuring instruments
- μPD75064(A), 75066(A), 75068(A)
  Automotive electronics ★

The information in this document is subject to change without notice.

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The mark ★ shows revised points.

The μPD75064, 75066, 75068 and μPD75064(A), 75066(A), 75068(A) differ only in their quality grade.
Unless otherwise specified, this data sheet describes the μPD75068 as the representative product.
For products with the suffix (A) attached, please make the following substitutions when reading:
μPD75064 —> μPD75064(A)
μPD75066 —> μPD75066(A)
μPD75068 —> μPD75068(A)

ORDERING INFORMATION

Part number	Package	Quality Grade
μPD75064CU-xxx	42-pin plastic shrink DIP (600 mil)	Standard
μPD75064GB-xxx-3B4	44-pin plastic QFP (10x10 mm)	Standard
μPD75066CU-xxx	42-pin plastic shrink DIP (600 mil)	Standard
μPD75066GB-xxx-3B4	44-pin plastic QFP (10x10 mm)	Standard
μPD75068CU-xxx	42-pin plastic shrink DIP (600 mil)	Standard
μPD75068GB-xxx-3B4	44-pin plastic QFP (10x10 mm)	Standard
★ μPD75064CU(A)-xxx	42-pin plastic shrink DIP (600 mil)	Special
★ μPD75064GB(A)-xxx-3B4	44-pin plastic QFP (10x10 mm)	Special
★ μPD75066CU(A)-xxx	42-pin plastic shrink DIP (600 mil)	Special
★ μPD75066GB(A)-xxx-3B4	44-pin plastic QFP (10x10 mm)	Special
★ μPD75068CU(A)-xxx	42-pin plastic shrink DIP (600 mil)	Special
★ μPD75068GB(A)-xxx-3B4	44-pin plastic QFP (10x10 mm)	Special

Remark xxx : ROM code suffix

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

★ DIFFERENCE BETWEEN μPD7506x SUBSERIES AND μPD7506x(A) SUBSERIES

Part number / Parameter	μPD75064 μPD75066 μPD75068	μPD75064(A) μPD75066(A) μPD75068(A)
Quality grade	Standard	Special

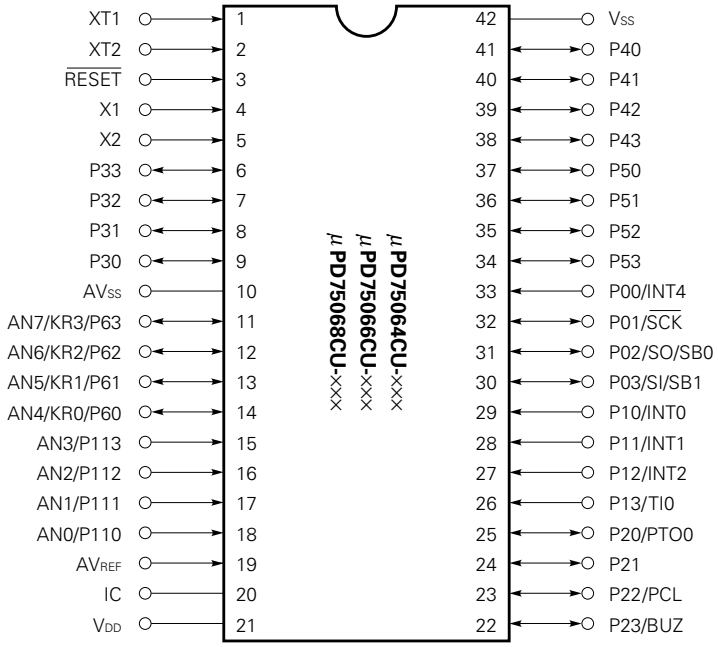
FUNCTION OVERVIEW

Item		Function			
Instruction execution time		• Main system clock : 0.95 μs, 1.91 μs, 15.3 μs (at 4.19 MHz) • Subsystem clock : 122 μs (at 32.768 kHz)			
Internal memory	ROM	• μPD75064: 4096 × 8 bits • μPD75066 : 6016 × 8 bits • μPD75068 : 8064 × 8 bits			
	RAM	512 × 4 bits			
General register		• When operating in 4 bits: 8 • When operating in 8 bits: 4			
I/O port		32	12	CMOS input	Of these, seven with software-specifiable on-chip pull-up resistors
			12	CMOS I/O	Software-specifiable on-chip pull-up resistors Four pins can directly drive LEDs.
			8	N-ch open-drain I/O	Breakdown voltage: 10 V Mask-option-specifiable on-chip pull-up resistors Can directly drive LEDs.
Timer		3 chs.		• Timer/event counter • Basic interval timer : Applicable to watchdog timer • Watch timer : Capable of buzzer output	
Serial interface		• 3-wire serial I/O mode • 2-wire serial I/O mode • SBI mode			
Bit sequencial buffer		16 bits			
Clock output function		Φ , $f_X/2^3$, $f_X/2^4$, $f_X/2^6$ (Main system clock: at 4.19 MHz operation)			
A/D converter		• 8-bit resolution x 8 channels • Low-power operation possible : V_{DD} = 2.7 to 6.0 V			
Vectored interrupt		External : 3 , Internal : 3			
Test input		External : 1, Internal : 1			
System clock oscillator		• Ceramic/crystal oscillator for main system clock • Crystal oscillator for subsystem clock			
Standby function		STOP / HALT mode			
Operating ambient temperature		–40 to +85 °C			
Operating supply voltage		2.7 to 6.0 V			
Package		• 42-pin plastic shrink DIP (600 mil) • 44-pin plastic QFP (10 x 10 mm)			

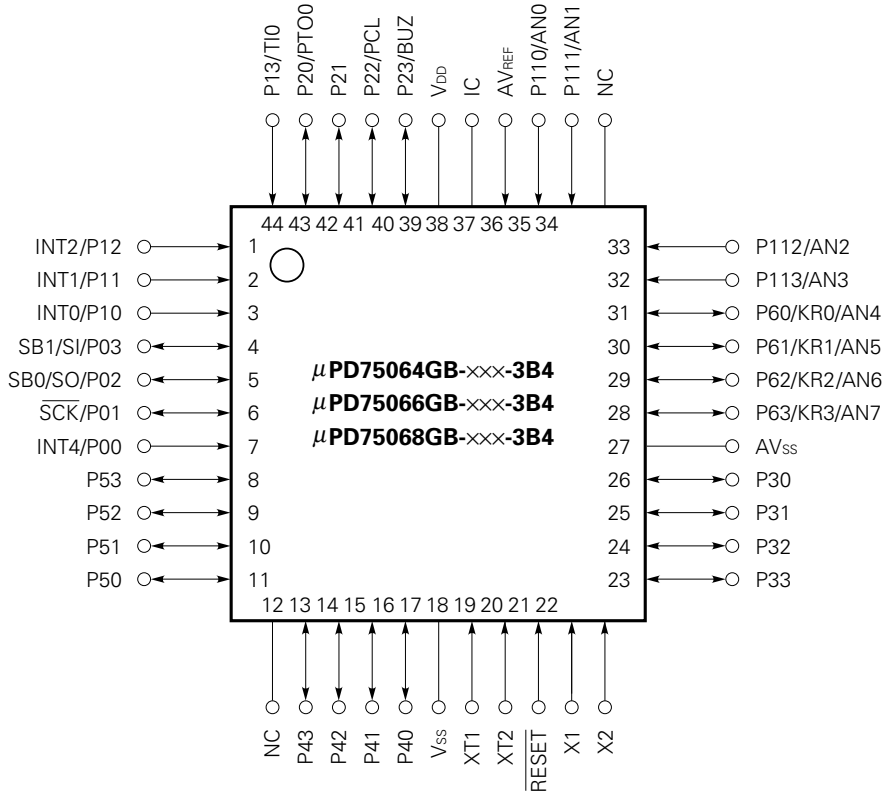
CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

- **42-pin plastic shrink DIP**



- **44-pin plastic QFP**

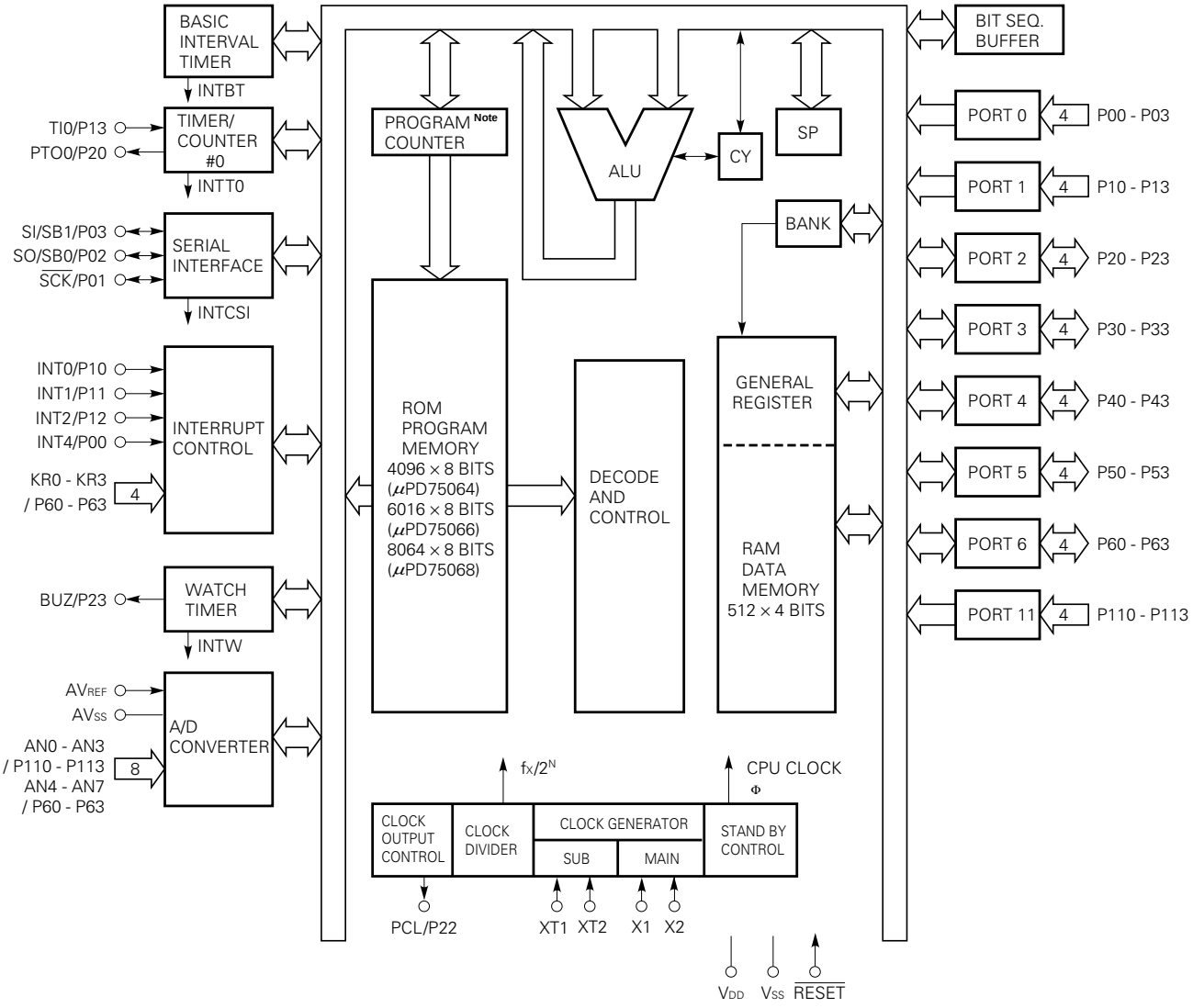


IC : Internally Connected (This pin should be directly connected to V_{DD})

PIN IDENTIFICATIONS

P00 - 03 : Port 0
P10 - 13 : Port 1
P20 - 23 : Port 2
P30 - 33 : Port 3
P40 - 43 : Port 4
P50 - 53 : Port 5
P60 - 63 : Port 6
P110 - 113 : Port 11
KR0 - 3 : Key Return
$\overline{SCK}$: Serial Clock
SI : Serial Input
SO : Serial Output
SB0, 1 : Serial Bus 0, 1
$\overline{RESET}$: Reset Input
TI0 : Timer Input 0
PTO0 : Programmable Timer Output 0
BUZ : Buzzer Clock
PCL : Programmable Clock
INT0, 1, 4 : External Vectored Interrupt 0, 1, 4
INT2 : External Test Input 2
X1, 2 : Main System Clock Oscillation 1, 2
XT1, 2 : Subsystem Clock Oscillation 1, 2
AN0 - 7 : Analog Input 0 - 7
AV_{REF} : Analog Reference
AV_{SS} : Analog V_{SS}
V_{DD} : Positive Power Supply
V_{SS} : Ground

2. BLOCK DIAGRAM



Note The μPD75064 uses the program counter of a 12-bit configuration, the μPD75066 and μPD75068 use that of a 13-bit configuration.

3. PIN FUNCTIONS

3.1 Port Pins

Pin name	Input/ output	Shared with	Function	8-bit I/O	When reset	I/O circuit type[Note 1]
P00	Input	INT4	4-bit input port (PORT0). For P01 to P03, pull-up resistors can be provided by software in units of 3 bits.	×	Input	Ⓑ
P01	I/O	$\overline{SCK}$				Ⓕ-A
P02	I/O	SO/SB0				Ⓕ-B
P03	I/O	SI/SB1				Ⓜ-C
P10	Input	INT0	With noise elimination function	×	Input	Ⓑ-C
P11		INT1	4-bit input port (PORT1). Pull-up resistors can be provided by software in units of 4 bits.			
P12		INT2				
P13		TI0				
P20	I/O	PTO0	4-bit I/O port (PORT2). Pull-up resistors can be provided by software in units of 4 bits.	×	Input	E-B
P21		–				
P22		PCL				
P23		BUZ				
P30[Note 2]	I/O	–	Programmable 4-bit I/O port (PORT3). I/O can be specified bit by bit. Pull-up resistors can be provided by software in units of 4 bits.	×	Input	E-B
P31[Note 2]		–				
P32[Note 2]		–				
P33[Note 2]		–				
P40 - P43[Note 2]	I/O	–	N-ch open-drain 4-bit I/O port (PORT4). A pull-up resistor can be provided for each bit (mask option). Breakdown voltage is 10 V in open-drain mode.	○	High level (when pull-up resistors are provided) or high impedance	M
P50 - P53[Note 2]	I/O	–	N-ch open-drain 4-bit I/O port (PORT5). A pull-up resistor can be provided for each bit (mask option). Breakdown voltage is 10 V in open-drain mode.		High level (when pull-up resistors are provided) or high impedance	M
P60	I/O	KR0/AN4	Programmable 4-bit I/O port (PORT6). I/O can be specified bit by bit. Pull-up resistors can be provided by software in units of 4 bits.	×	Input	Ⓨ-D
P61		KR1/AN5				
P62		KR2/AN6				
P63		KR3/AN7				
P110	Input	AN0	4-bit input port (PORT11).	×	Input	Y-A
P111		AN1				
P112		AN2				
P113		AN3				

Notes 1. The circle (○) indicates the Schmitt trigger input.

2. Can directly drive LEDs.

3.2 Non-Port Pins

Pin name	Input/ output	Shared with	Function		When reset	I/O circuit type[Note 1]
TI0	Input	P13	Input for receiving external event pulse signal for timer/event counter		–	Ⓑ-C
PTO0	I/O	P20	Timer/event counter output		Input	E-B
PCL	I/O	P22	Clock output		Input	E-B
BUZ	I/O	P23	Output frequency selectable (for buzzer output or system clock trimming)		Input	E-B
$\overline{SCK}$	I/O	P01	Serial clock I/O		Input	Ⓕ-A
SO/SB0	I/O	P02	Serial data output Serial bus I/O		Input	Ⓕ-B
SI/SB1	I/O	P03	Serial data input Serial bus I/O		Input	Ⓜ-C
INT4	Input	P00	Edge-detective vectored interrupt input (both rising and falling edges enabled)		–	Ⓑ
INT0	Input	P10	Edge-detective vectored interrupt input (detection edge selectable)	Note 2	–	Ⓑ-C
INT1		P11		Note 3		
INT2	Input	P12	Edge-detective testable input (rising edge detection)	Note 3	–	Ⓑ-C
KR0 - KR3	I/O	P60 - P63/ AN4 - AN7	Parallel falling edge detection testable input		Input	Ⓨ-D
AN0 - AN3	Input	P110 - P113	For A/D converter only	8-bit analog input	Input	Y-A
AN4 - AN7	I/O	P60 - P63/ KR0 - KR3				Ⓨ-D
AV_{REF}	Input	–		Reference voltage input	–	Z
AV_{SS}	–	–		GND potential	–	Z
X1, X2	Input	–	Crystal/ceramic connection for main system clock generation. When external clock signal is used, the signal should be applied to X1, and its reverse phase signal to X2.		–	–
XT1, XT2	Input	–	Crystal connection for subsystem clock generation. When external clock signal is used, the signal should be applied to XT1, and its reverse phase signal to XT2. XT1 can be used as a 1-bit input (test).		–	–
$\overline{RESET}$	Input	–	System reset input		–	Ⓑ
IC	–	–	Internally connected. (Connect this pin directly to V_{DD})		–	–
V_{DD}	–	–	Positive power supply		–	–
V_{SS}	–	–	GND potential		–	–

Notes 1. The circle (◯) indicates the Schmitt trigger input.

2. Clock synchronous

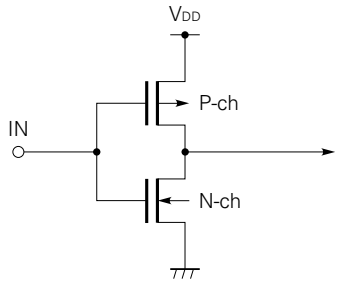
3. Asynchronous

3.3 Pin Input/Output Circuits

The input/output circuit of each μPD75068 pin is shown below in a simplified manner.

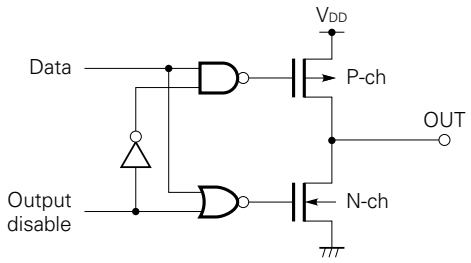
(1/3)

Type A (For type E-B)



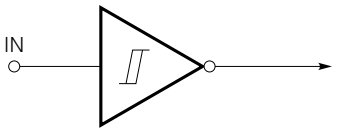
CMOS input buffer

Type D (For type E-B, F-A)



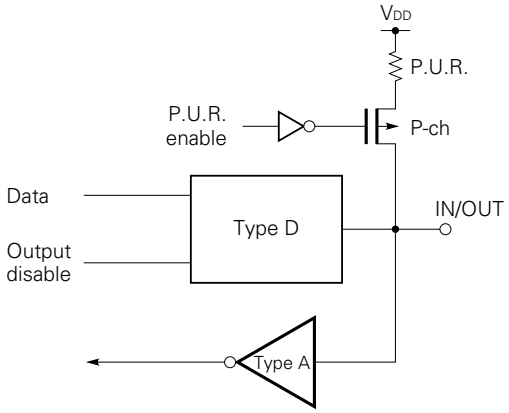
Push-pull output which can be set to high impedance output (off for both P-ch and N-ch)

Type B



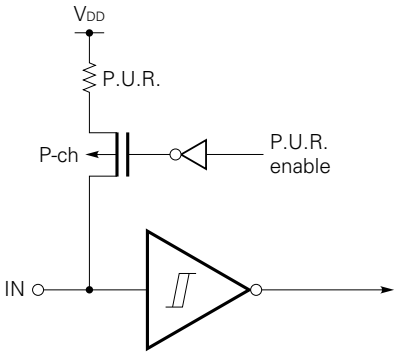
Schmitt trigger input with hysteresis

Type E-B



P.U.R.: Pull-Up Resistor

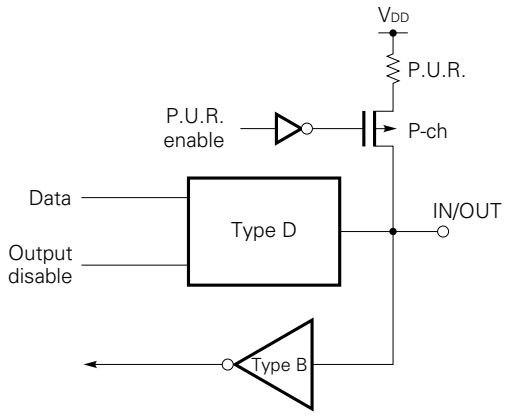
Type B-C



P.U.R.: Pull-Up Resistor

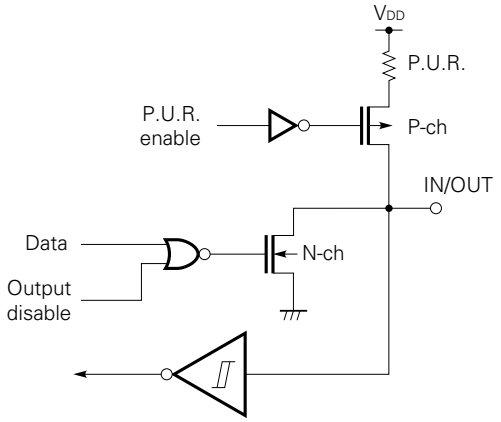
(2/3)

Type F-A



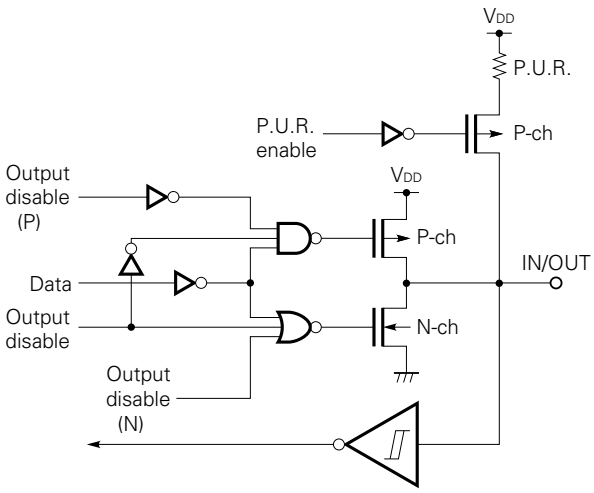
P.U.R.: Pull-Up Resistor

Type M-C



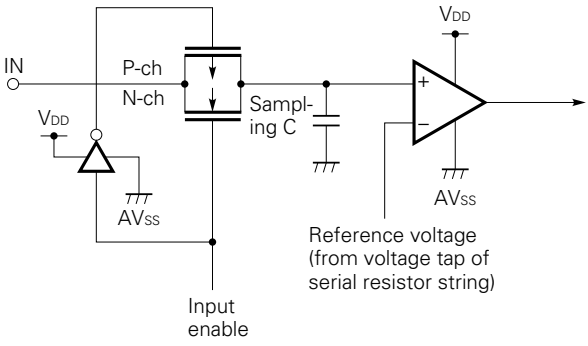
P.U.R.: Pull-Up Resistor

Type F-B

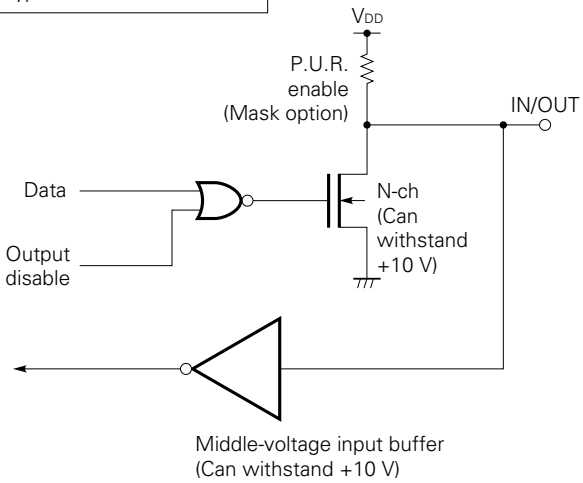


P.U.R.: Pull-Up Resistor

Type Y (For type Y-A , Y-D)

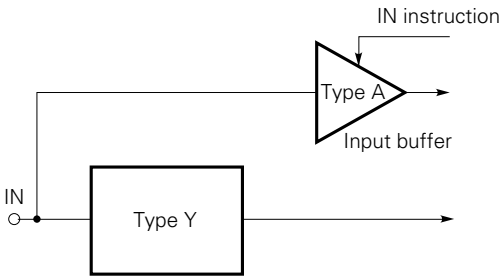


Type M

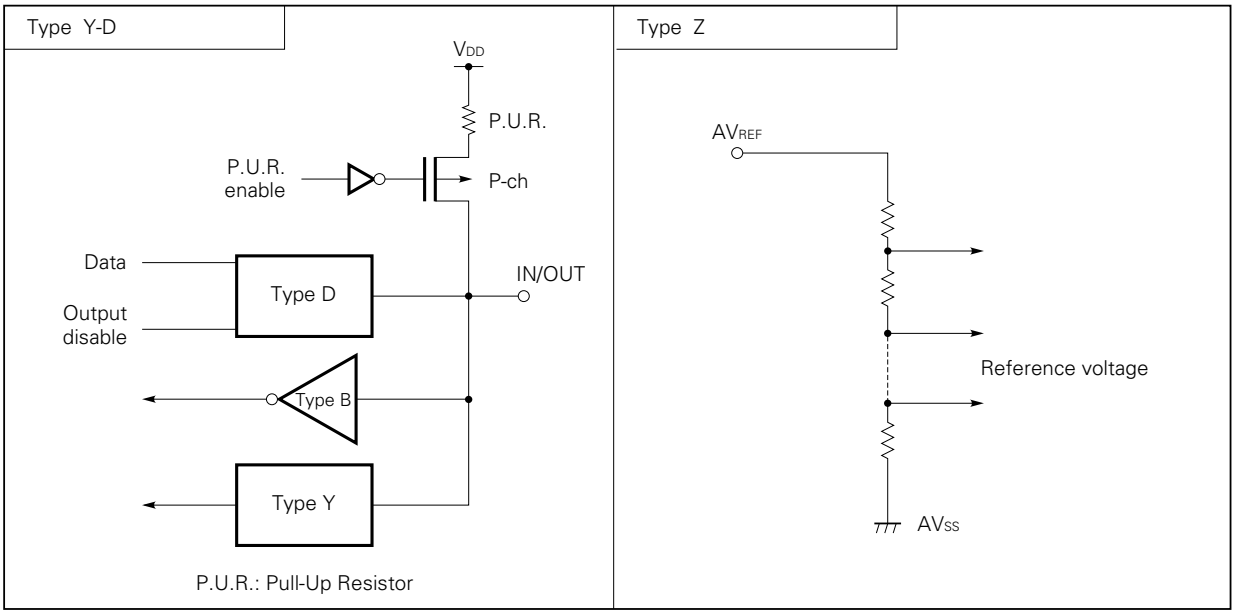


P.U.R.: Pull-Up Resistor

Type Y-A



(3/3)



3.4 Mask Option Selection

The following mask options are available for selection for each pin.

Pin name	Mask option	
P40 - P43, P50 - P53	① Pull-up resistor enabled (specifiable bit by bit)	② Pull-up resistor disabled (specifiable bit by bit)
XT1, XT2	① Feedback resistor enabled (if a subsystem clock is used)	② Feedback resistor disabled (if a subsystem clock is not used)

3.5 Handling Unused Pins

Table 3-1. Handling Unused Pins

Pin	Recommended connection
P00/INT4	Connect to V_{SS}.
P01/$\overline{SCK}$	Connect to V_{SS} or V_{DD}.
P02/SO/SB0	
P03/SI/SB1	
P10/INT0-P12/INT2	Connect to V_{SS}.
P13/TI0	
P20/PTO0	Input state: Connect to V_{SS} or V_{DD}.
P21	Output state: Open
P22/PCL	
P23/BUZ	
P30-P33	
P40-P43	
P50-53	
P60/KR0/AN4-P63/KR3/AN7	
P110/AN0-P113/AN3	Connect to V_{SS} or V_{DD}.
AV_{REF}	Connect to V_{SS}.
AV_{SS}	
XT1	Connect to V_{SS} or V_{DD}.
XT2	Open
IC	Directly connect to V_{DD}.

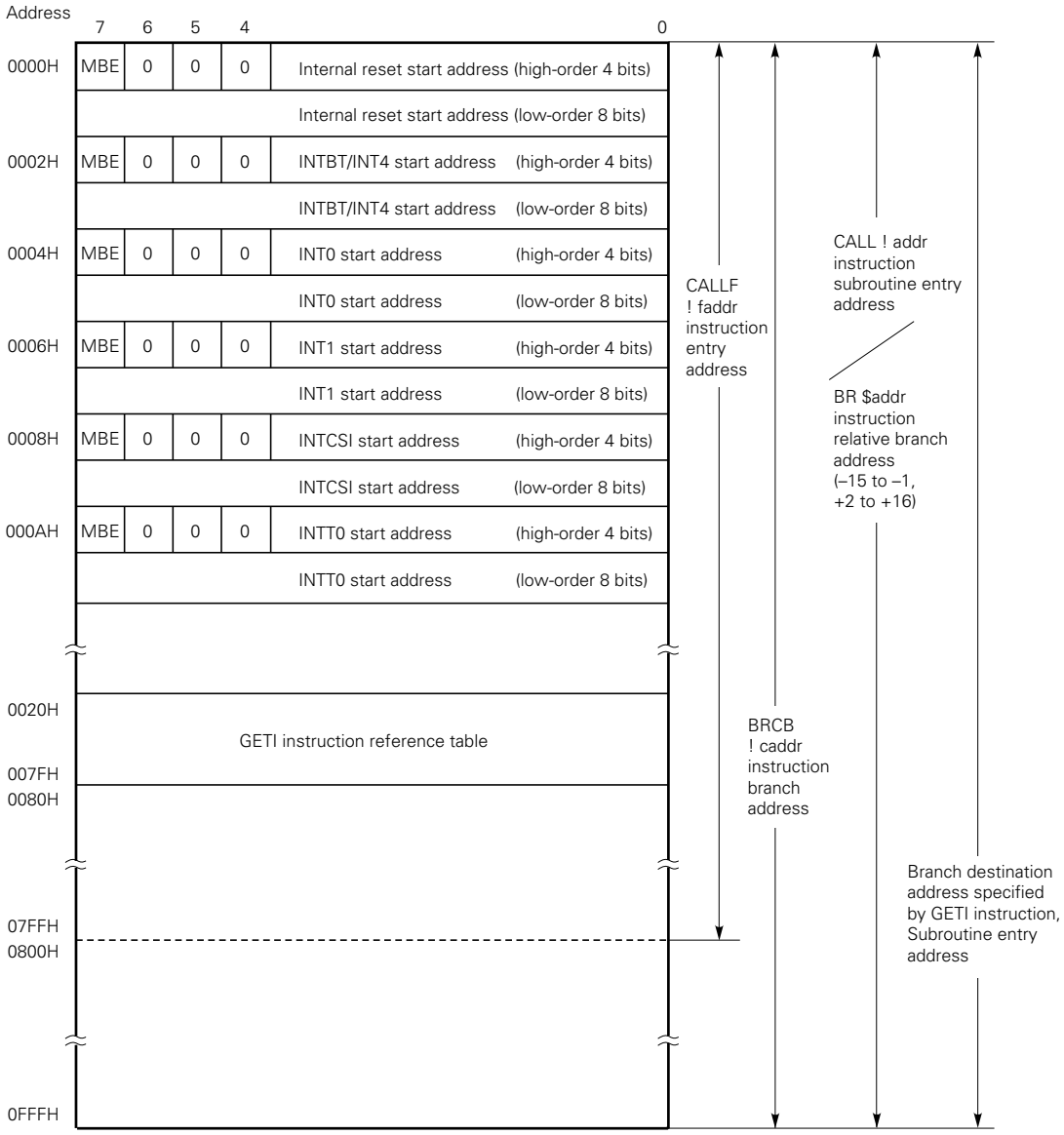
4. MEMORY CONFIGURATION

- Program memory (ROM) ..... 4096 × 8 bits (0000H to 0FFFH) : μPD75064
  ..... 6016 × 8 bits (0000H to 177FH) : μPD75066
  ..... 8064 × 8 bits (0000H to 1F7FH) : μPD75068
  - 0000H to 0001H : Vector table in which the program start address by reset is stored
  - 0002H to 000BH : Vector table in which the program start address by interrupt is stored
  - 0020H to 007FH : Table area to be referenced by GETI instruction

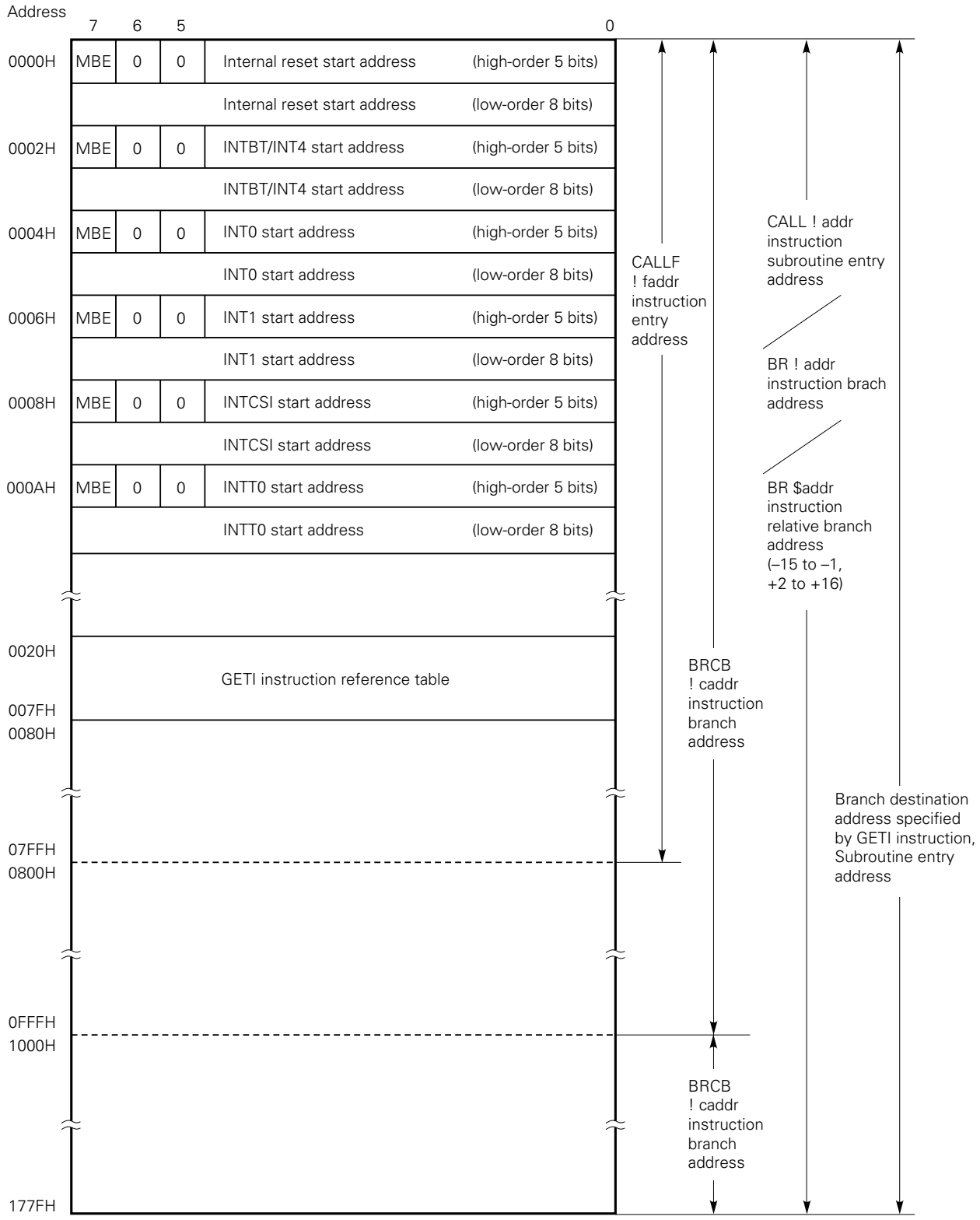
- Data memory
  - Data area ..... 512 × 4 bits (000H to 1FFH)
  - Peripheral hardware area ..... 128 × 4 bits (F80H to FFFH)

Figure 4-1. Program Memory Map

(a) μPD75064



(b) μPD75066


Address
7
6
5
0
0000H
MBE
0
0
Internal reset start address (high-order 5 bits)
Internal reset start address (low-order 8 bits)
0002H
MBE
0
0
INTBT/INT4 start address (high-order 5 bits)
INTBT/INT4 start address (low-order 8 bits)
0004H
MBE
0
0
INT0 start address (high-order 5 bits)
INT0 start address (low-order 8 bits)
0006H
MBE
0
0
INT1 start address (high-order 5 bits)
INT1 start address (low-order 8 bits)
0008H
MBE
0
0
INTCSI start address (high-order 5 bits)
INTCSI start address (low-order 8 bits)
000AH
MBE
0
0
INTT0 start address (high-order 5 bits)
INTT0 start address (low-order 8 bits)
0020H
GETI instruction reference table
007FH
0080H
07FFH
0800H
0FFFH
1000H
177FH
CALLF ! faddr instruction entry address
BRCB ! caddr instruction branch address
BRCB ! caddr instruction branch address
CALL ! addr instruction subroutine entry address
BR ! addr instruction brach address
BR $addr instruction relative branch address (–15 to –1, +2 to +16)
Branch destination address specified by GETI instruction, Subroutine entry address

(c) μPD75068

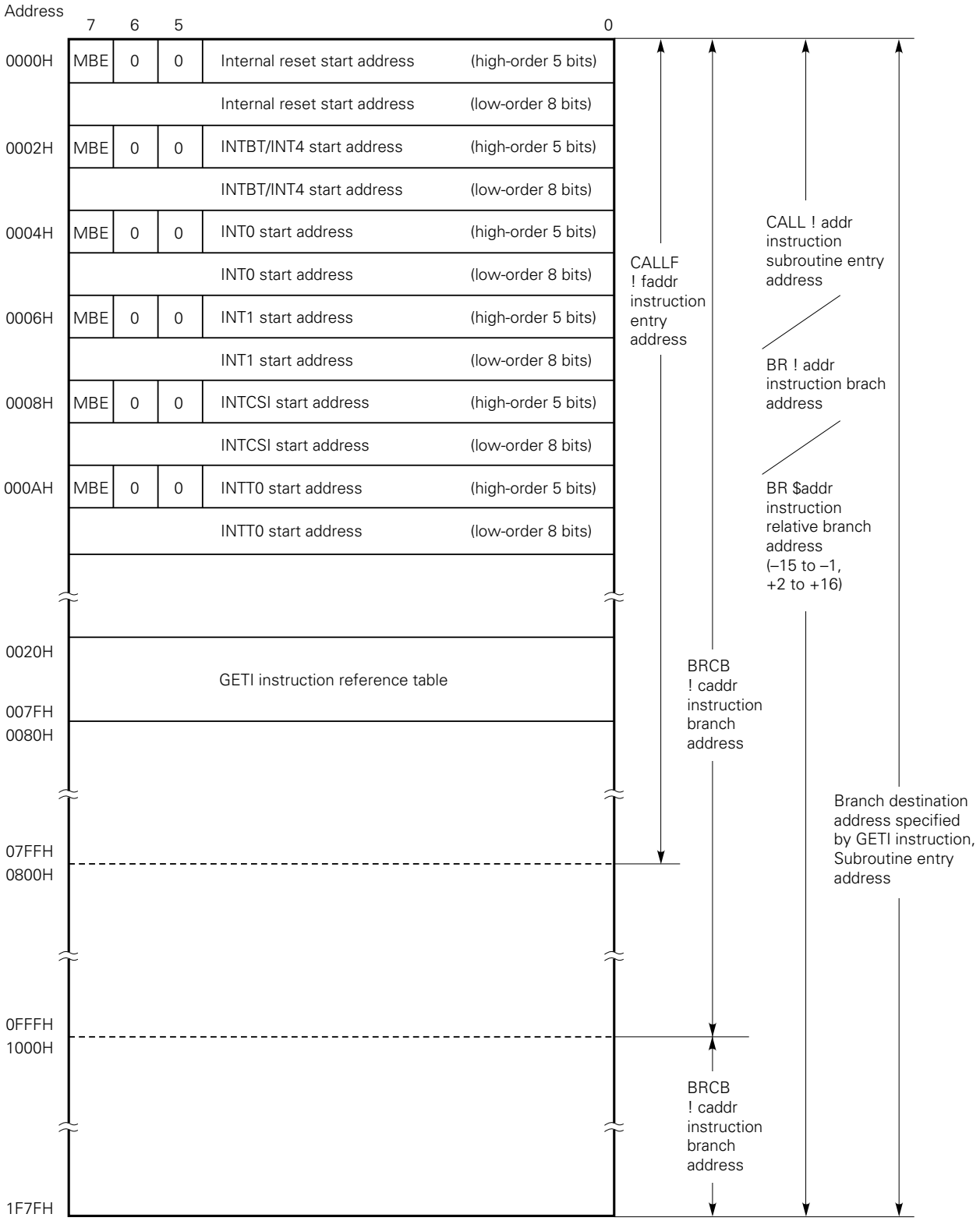
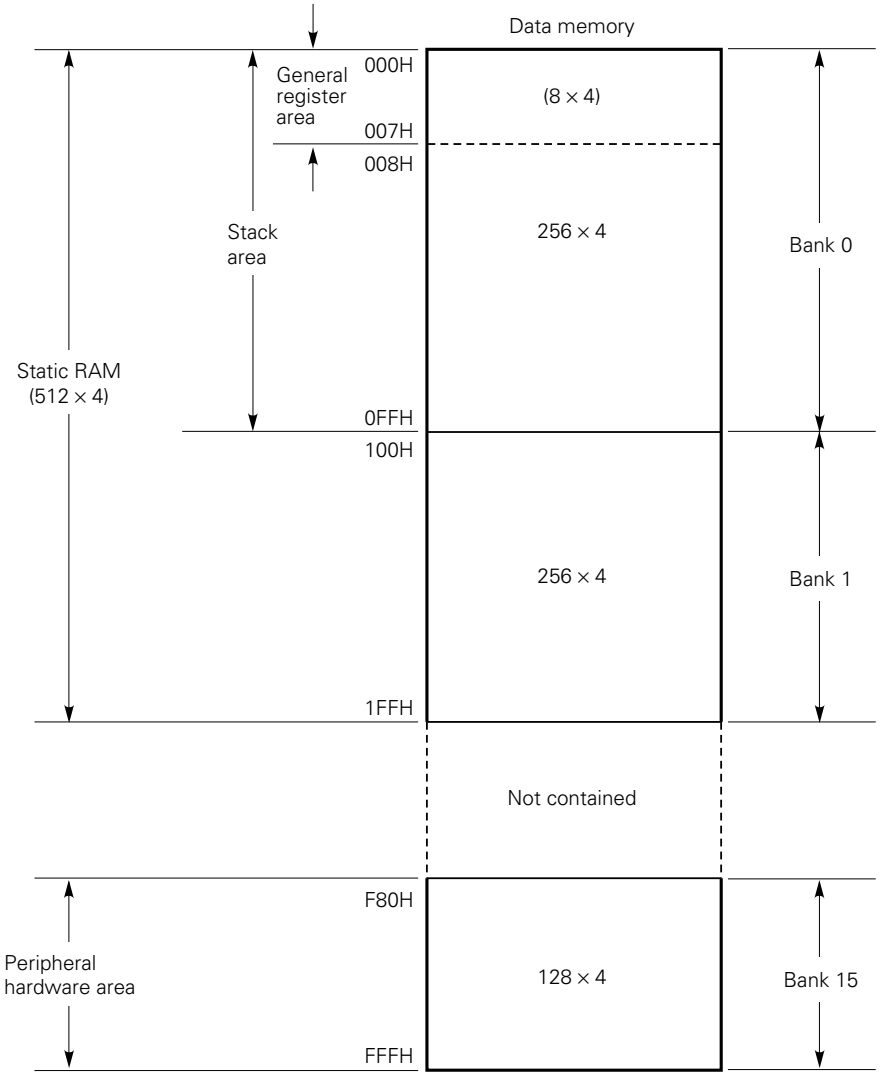

Address
7
6
5
0
0000H
MBE
0
0
Internal reset start address (high-order 5 bits)
Internal reset start address (low-order 8 bits)
0002H
INTBT/INT4 start address (high-order 5 bits)
INTBT/INT4 start address (low-order 8 bits)
0004H
INT0 start address (high-order 5 bits)
INT0 start address (low-order 8 bits)
0006H
INT1 start address (high-order 5 bits)
INT1 start address (low-order 8 bits)
0008H
INTCSI start address (high-order 5 bits)
INTCSI start address (low-order 8 bits)
000AH
INTT0 start address (high-order 5 bits)
INTT0 start address (low-order 8 bits)
0020H
GETI instruction reference table
007FH
0080H
07FFH
0800H
0FFFH
1000H
1F7FH
CALLF ! faddr instruction entry address
CALL ! addr instruction subroutine entry address
BR ! addr instruction brach address
BR $addr instruction relative branch address (–15 to –1, +2 to +16)
BRCB ! caddr instruction branch address
BRCB ! caddr instruction branch address
Branch destination address specified by GETI instruction, Subroutine entry address

Figure 4-2. Data Memory Map



5. PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

The following three types of I/O port are provided:

- CMOS input ports (PORT0, 1, 11) : 12
- CMOS input/output ports (PORT2, 3, 6) : 12
- N-ch open-drain input/output ports (PORT4, 5) : 8

Total 32

Table 5-1. Functions of Port

Port (Symbol)	Function	Operation/features	Remarks
PORT0 PORT1	4-bit input	Can be read or tested regardless of the operation mode of the dual function pin.	Shared with the SO/SB0, SI/SB1, $\overline{SCK}$, INT0-2, 4, and TI0 pins.
PORT3[Note] PORT6	4-bit I/O	Can be specified for input/output in bit units.	Port 6 is shared with pins KR0 to KR3 and pins AN4 to AN7.
PORT2		Can be specified for input/output in 4-bit units.	Port 2 is shared with PTO0, PCL, and BUZ pins.
PORT4[Note] PORT5[Note]	4-bit I/O (N-ch open-drain, can withstand 10 V)	Can be specified for input/output in 4-bit units. Ports 4 and 5 can be paired to input/output data in 8-bit units.	Whether or not the internal pull-up resistor is provided can be specified for each bit by mask option.
PORT11	4-bit input	4-bit port dedicated to input	Port 11 is shared with pins AN0 to AN3.

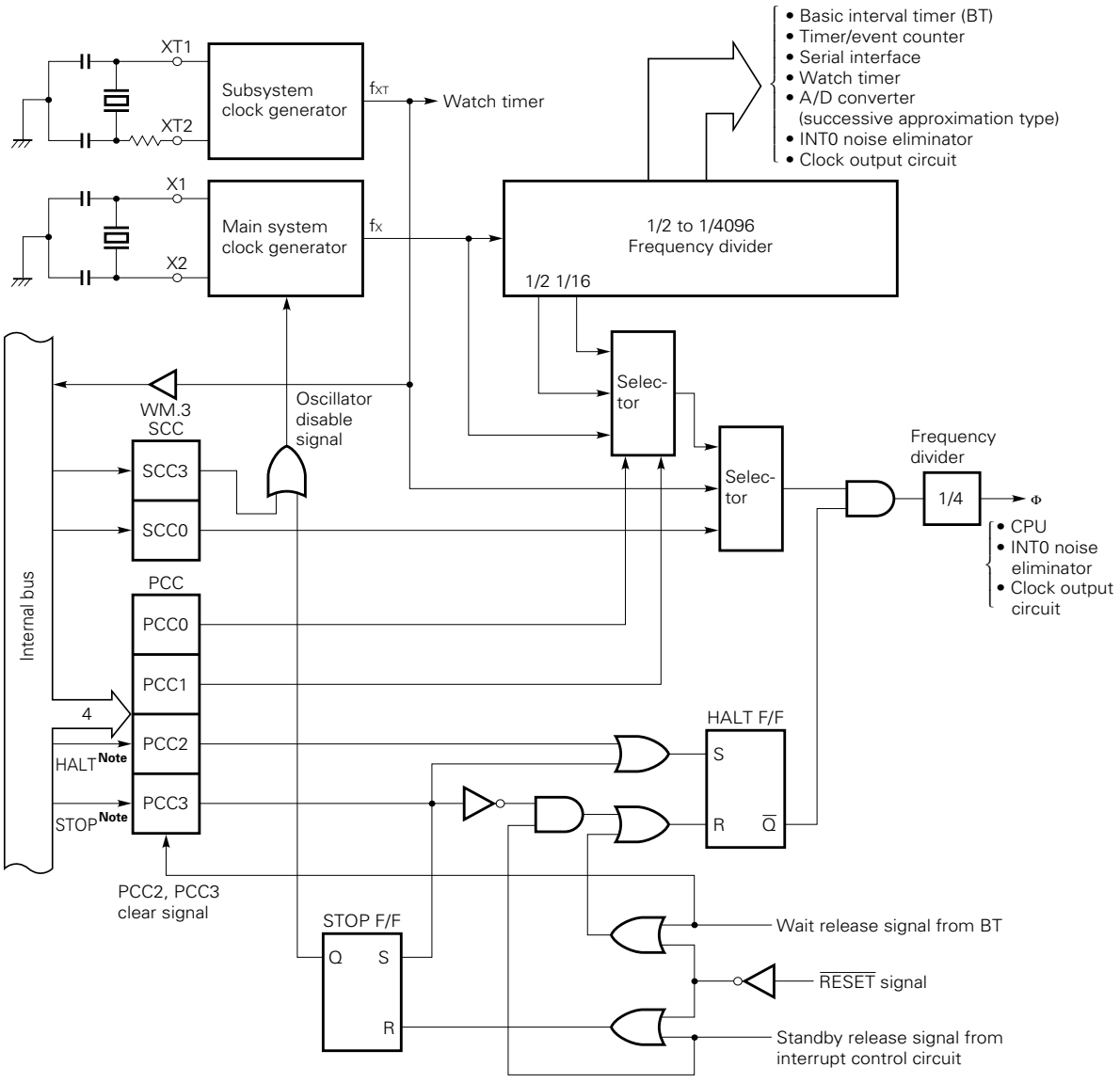
Note Can directly drive LEDs.

5.2 Clock Generator

The clock generator operates according to the statuses of the processor clock control register (PCC) and the system clock control register (SCC). Two types of clock are provided: main system clock and subsystem clock, and the instruction execution time can be changed.

- 0.95 μs / 1.91 μs / 15.3 μs (operated with main system clock at 4.19 MHz)
- 122 μs (operated with subsystem clock at 32.768 kHz)

Figure 5-1. Clock Generator Block Diagram



Note Instruction execution

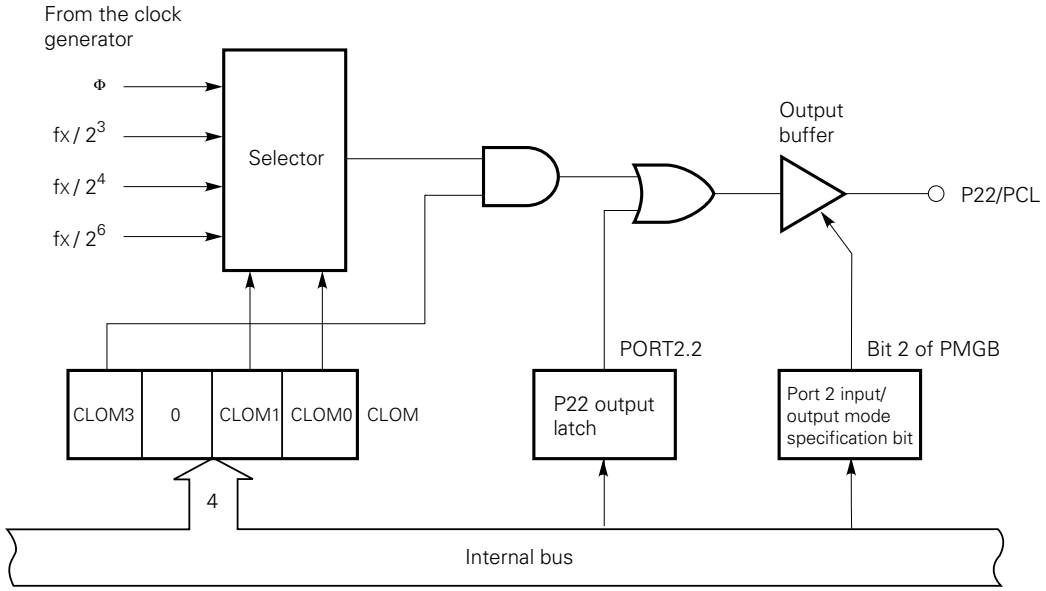
Remarks
1. fX = Main system clock frequency
2. fXT = Subsystem clock frequency
3. Φ = CPU clock
4. PCC: Processor clock control register
5. SCC: System clock control register
6. One clock cycle (tCY) at Φ is equal to one machine cycle of an instruction.
   For tCY, refer to **AC Characteristics in 10. ELECTRICAL SPECIFICATIONS**.

5.3 Clock Output Circuit

The clock output circuit outputs clock pulses from the P22/PCL pin, and is used to supply clock pulses to remote unit controller and peripheral LSIs.

- Clock output (PCL): Φ, 524 kHz, 262 kHz, 65.5 kHz (fx = at 4.19 MHz)

Figure 5-2. Clock Output Circuit Configuration



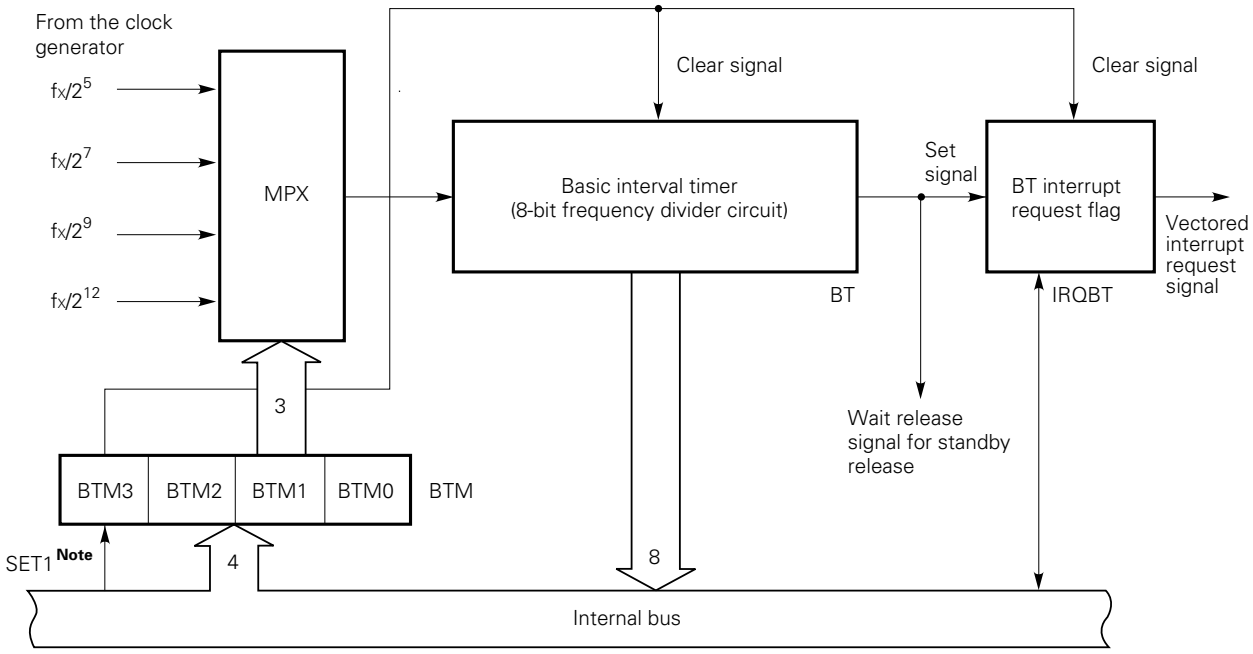
Remark Measures are taken to prevent outputting a narrow pulse when selecting clock output enable/disable.

5.4 Basic Interval Timer

The basic interval timer has these functions:

- Interval timer operation which generates a reference timer interrupt
- Watchdog timer application which detects a program runaway
- Selection of wait time for releasing the standby mode and counting the wait time
- Reading out the count value

Figure 5-3. Basic Interval Timer Configuration



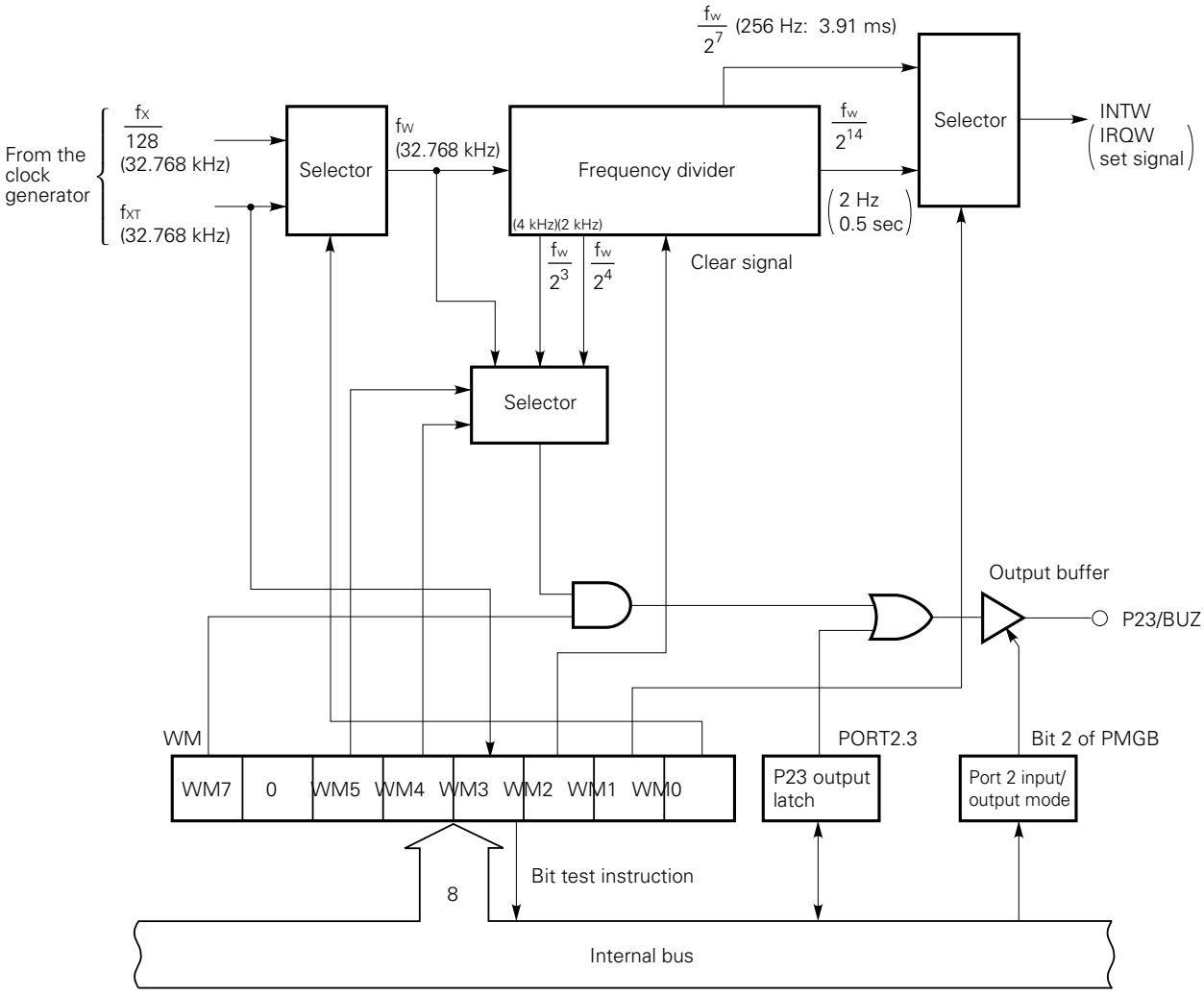
Note Instruction execution

5.5 Watch Timer

The μPD75068 has an on-chip 1-ch watch timer. The watch timer has the following functions:

- Sets the test flag (IRQW) with a 0.5-sec interval. The standby mode can be released by IRQW.
- The 0.5-second interval can be generated from either the main system clock or subsystem clock.
- The time interval can be made 128 times faster (3.91 ms) by selecting the fast mode. This is convenient for program debugging, testing, etc.
- Any of the frequencies 2.048 kHz, 4.096 kHz, and 32.768 kHz can be output to the P23/BUZ pin. This can be used for beep and system clock frequency trimming.
- The frequency divider circuit can be cleared so that a zero-second start of the watch can be made.

Figure 5-4. Watch Timer Block Diagram



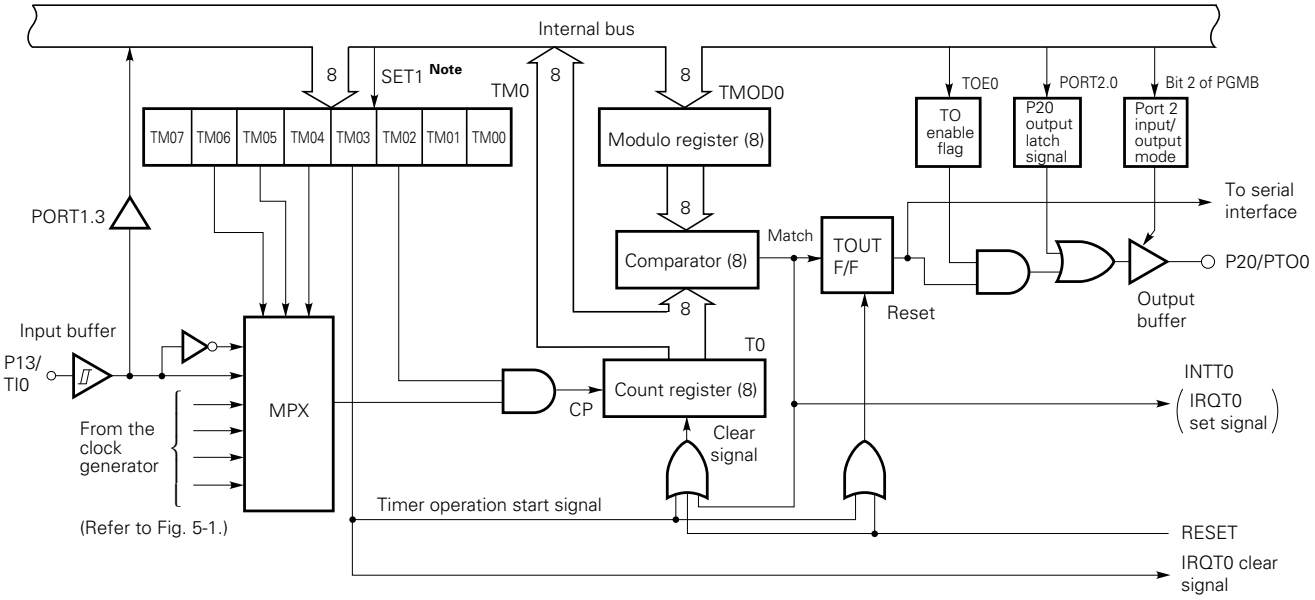
Remark ( ) is for fX = 4.194304 MHz, fXT = 32.768 kHz.

5.6 Timer/Event Counter

The μPD75068 has an on-chip 1-ch timer/event counter. The timer/event counter has the following functions:

- Programmable interval timer operation
- Outputs square-wave signal of a user-selectable frequency to the PTO0 pin
- Event counter operation
- Divides the TI0 pin input by N and outputs to the PTO0 pin (frequency divider operation)
- Supplies serial shift clock to the serial interface circuit
- Count condition read-out function.

Figure 5-5. Block Diagram of Timer / Event Counter



Note Instruction execution

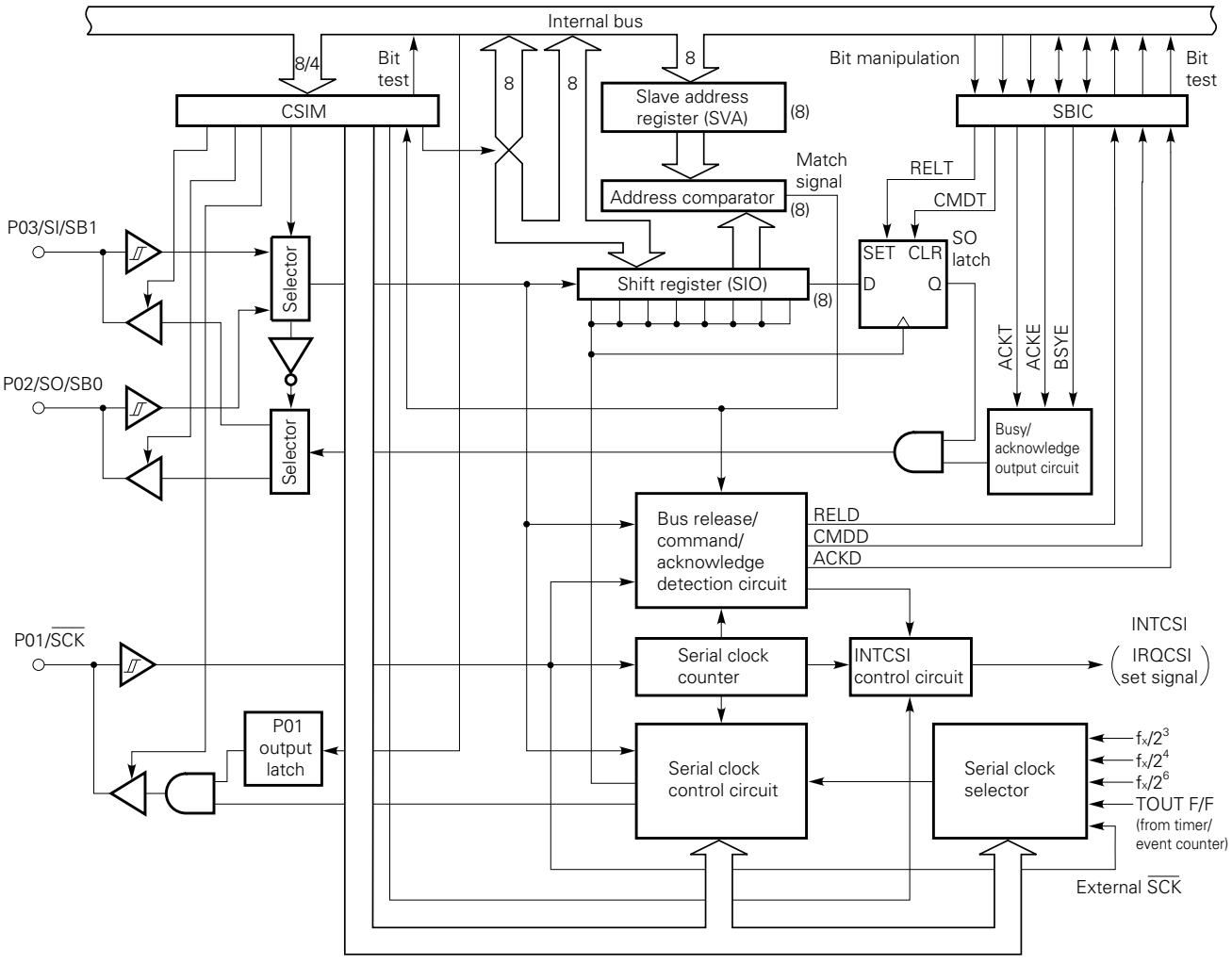
5.7 Serial Interface

(1) Serial interface function

The μPD75068 contains a clock synchronous 8-bit serial interface, which has four modes.

- Operation halt mode
- 3-wire serial I/O mode
- 2-wire serial I/O mode
- SBI (serial bus interface mode)

Figure 5-6. Block Diagram of Serial Interface

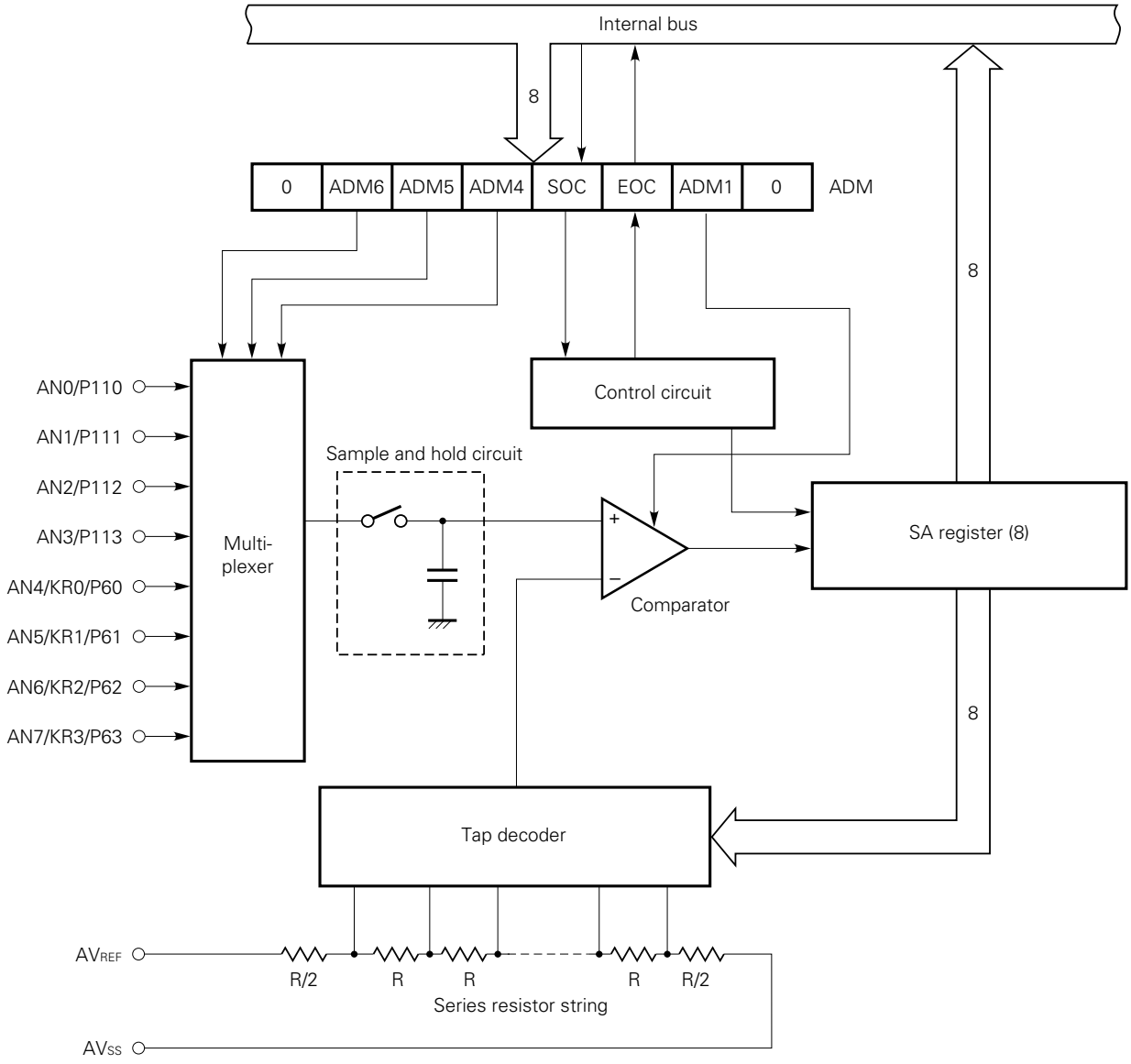


5.8 A/D Converter

The μPD75068 contains an 8-bit analog/digital (A/D) converter that has eight analog input channels (AN0 - AN7).

The A/D converter employs the successive-approximation method.

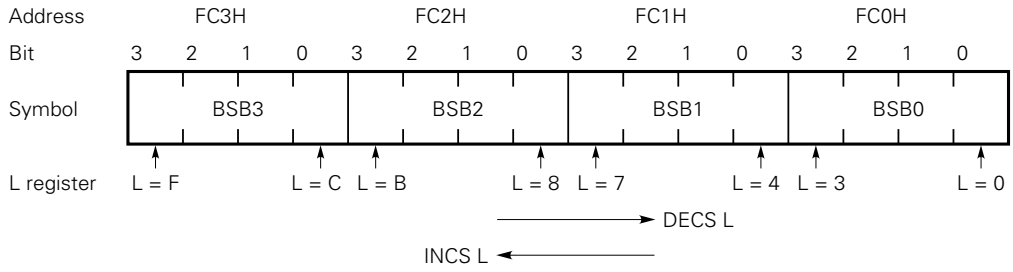
Figure 5-7. Block Diagram of A/D Converter



5.9 Bit Sequential Buffer: 16 Bits

The bit sequential buffer is a data memory specifically provided for bit manipulation. With this buffer, addresses and bit specifications can be sequentially updated by bit manipulation operation. Therefore, this buffer is very useful for processing long data in bit units.

Figure 5-8. Bit Sequential Buffer Format



Remark For "pmem.@L" addressing, the specification bit is shifted according to the L register.

6. INTERRUPT FUNCTIONS

The μPD75068 has six different interrupt sources. In addition, multiple interrupts with priority control are possible. Two types of test sources are provided. Of these test sources, INT2 has two types of edge detection testable inputs.

Table 6-1. Interruption Source Types

Interruption Source		IN/OUT	Interruption Order[Note1]	Vectored Interrupt Request Signal (Vector table address)
INTBT	(Reference time interval signal from basic interval timer)	IN	1	VRQ1 (0002H)
INT4	(Detection of both rising edge and falling edge is valid.)	OUT		
INT0	(Selection of rising edge detection or falling edge detection)	OUT	2	VRQ2 (0004H)
INT1		OUT	3	VRQ3 (0006H)
INTCSI	(Serial data transmission completion signal)	IN	4	VRQ4 (0008H)
INTT0	(Coincidence signal of programmable timer/counter count register and modulo register)	IN	5	VRQ5 (000AH)
INT2[Note2]	(Detection of rising edge of input to INT2 pin or detection of falling edge of any input to KR0 to KR3)	OUT	Test input signal (Set IRQ and IRQW)	
INTW[Note2]	(Signal from watch timer)	IN		

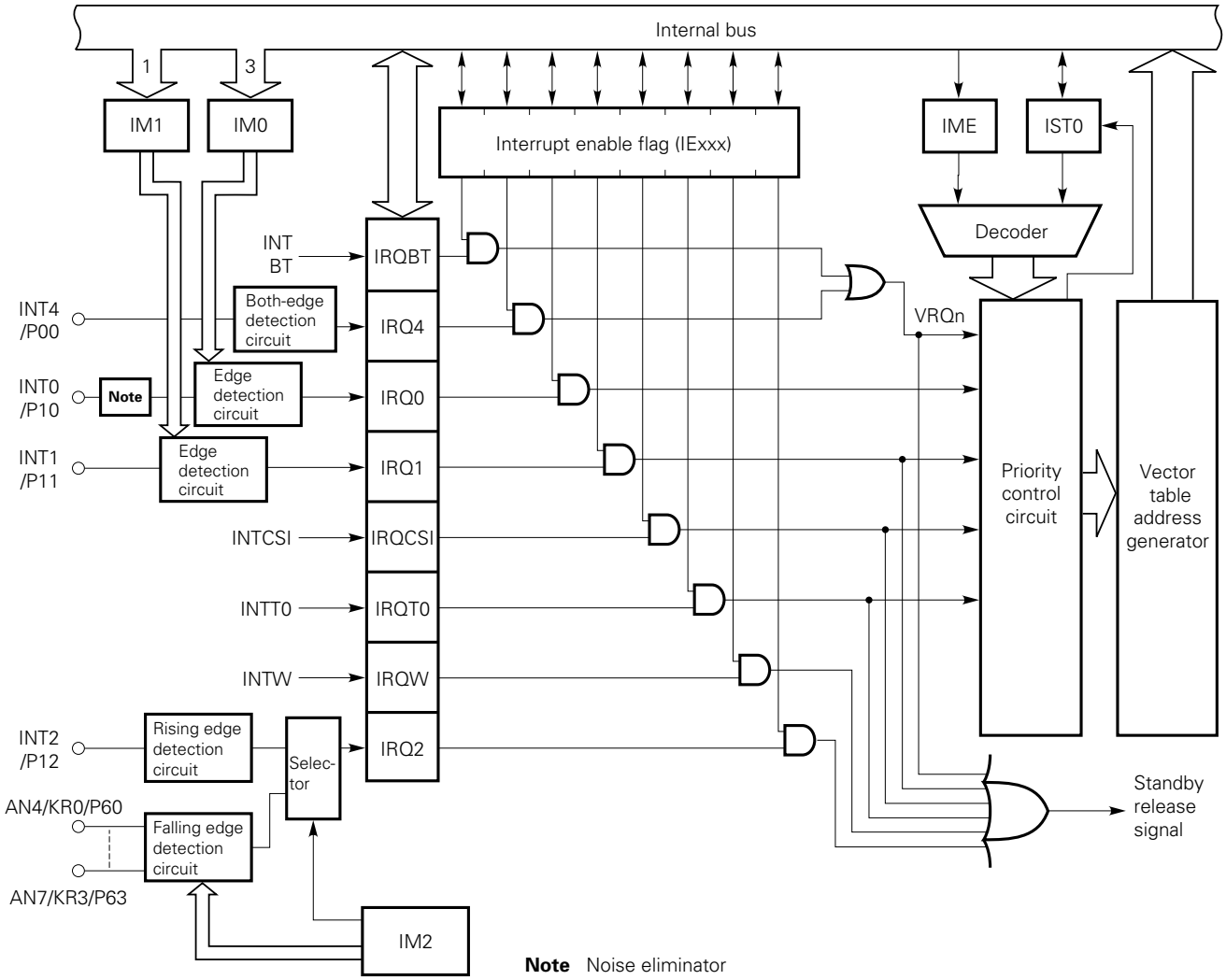
Notes 1. The interruption order shows the priority order of the pins when several interruption requests occur at the same time.

2. Test source. Like the interruption source, it is influenced by the interruption enable flag. However, vectored interrupt will not occur.

The interrupt control circuit of the μPD75068 has the following functions:

- Hardware controlled vectored interrupt function which can control whether or not to acknowledge an interrupt based on the interrupt flag (IE×××) and interrupt master enable flag (IME)
- The interrupt start address can be set arbitrarily.
- Interrupt request flag (IRQ×××) test function (an interrupt generation can be confirmed by software)
- Standby mode release (interrupts to be released can be selected by the interrupt enable flag)

Figure 6-1. Block Diagram of Interrupt Control Circuit



Note Noise eliminator

7. STANDBY FUNCTION

The μPD75068 has two different standby modes (STOP mode and HALT mode) to reduce power dissipation while waiting for program execution.

Table 7-1. Standby Mode Statuses

		STOP mode	HALT mode
Instruction for setting		STOP instruction	HALT instruction
System clock for setting		Can be set only when operating on the main system clock.	Can be set either with the main system clock or the subsystem clock.
Operation status	Clock oscillator	Only the main system clock stops its operation.	Only the CPU clock Φ stops its operation (oscillation continues).
	Basic interval timer	Does not operate.	Can operate only at main system clock oscillation (IRQBT is set at reference time intervals.).
	Serial interface	Can operate only when the external $\overline{SCK}$ input is selected for the serial clock.	Can operate only when external $\overline{SCK}$ input is selected as the serial clock or at main system clock oscillation.
	Timer/event counter	Can operate only when the TI0 pin input is selected for the count clock.	Can operate only when TI0 pin input is specified as the count clock or at main system clock oscillation.
	Watch timer	Can operate when f_{XT} is selected as the count clock.	Can operate.
	A/D converter	Does not operate.	Can operate.[Note]
	External interrupt	INT1, INT2, and INT4 can operate. Only INT0 cannot operate.	
	CPU	Does not operate.	
Release signal		An interrupt request signal from hardware whose operation is enabled by the interrupt enable flag or the $\overline{RESET}$ signal input	An interrupt request signal from hardware whose operation is enabled by the interrupt enable flag or the $\overline{RESET}$ signal input

Note A/D converter's operation in HALT mode is possible only when the main system clock operates.

8. RESET OPERATION

When the $\overline{\text{RESET}}$ signal is input, the μPD75068 is reset and all hardware is initialized as indicated in Table 8-1. Figure 8-1 shows the reset operation timing.

Figure 8-1. Reset Operation by $\overline{\text{RESET}}$ Input

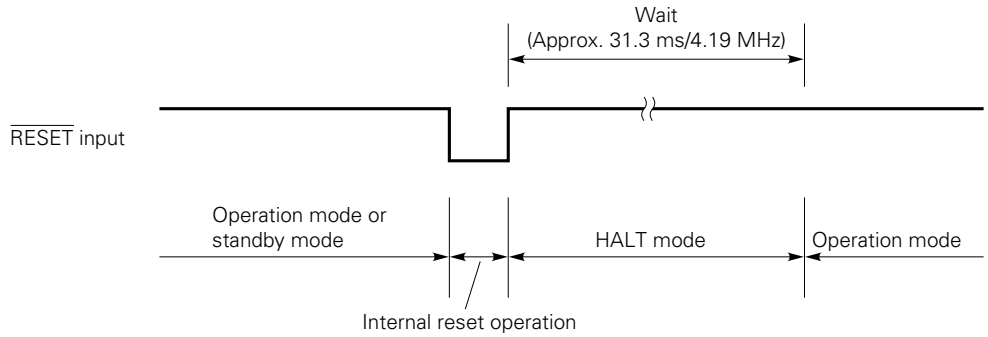


Table 8-1. Status of All Hardware after Reset (1/2)

Hardware			$\overline{\text{RESET}}$ input in standby mode	$\overline{\text{RESET}}$ input during operation
Program counter (PC)		μPD75064	Contents of lower 4 bits of address 0000H in program memory are set to PC11 - 8, and that of 0001H are set to PC7 - 0.	Same operation as that in standby state
		μPD75066 μPD75068	Contents of lower 5 bits of address 0000H in program memory are set to PC12 - 8, and that of 0001H are set to PC7 - 0.	Same operation as that in standby state
PSW	Carry flag (CY)		Retained	Undefined
	Skip flag (SK0-2)		0	0
	Interrupt status flag (IST0)		0	0
	Bank enable flag (MBE)		The contents of bit 7 of address 0000H of the program memory is set to MBE.	Same operation as that in standby state
Stack pointer (SP)			Undefined	Undefined
Data memory (RAM)			Retained[Note]	Undefined
General purpose register (X, A, H, L, D, E, B, C)			Retained	Undefined
Bank selection register (MBS)			0	0
Basic interval timer	Counter (BT)		Undefined	Undefined
	Mode register (BTM)		0	0
Timer/event counter	Counter (T0)		0	0
	Modulo register (TMOD0)		FFH	FFH
	Mode register (TM0)		0	0
	TOE0, TOUT F/F		0, 0	0, 0
Watch timer	Mode register (WM)		0	0

Note Data of address 0F8H to 0FDH of the data memory becomes undefined when the $\overline{\text{RESET}}$ signal is input.

Table 8-1. Status of All Hardware after Reset (2/2)

Hardware			$\overline{\text{RESET}}$ input in standby mode	$\overline{\text{RESET}}$ input during operation
Serial interface	Shift register (SIO)		Retained	Undefined
	Operation mode register (CSIM)		0	0
	SBI control register (SBIC)		0	0
	Slave address register (SVA)		Retained	Undefined
Clock generator, Clock output circuit	Processor clock control register (PCC)		0	0
	System clock control register (SCC)		0	0
	Clock output mode register (CLOM)		0	0
Interrupt function	Interrupt request flag (IRQxxx)	IRQ1, IRQ2, and IRQ4	Undefined	Undefined
		Other than above	0	0
	Interrupt enable flag (IE×××)		0	0
	Interrupt master enable flag (IME)		0	0
	INT0, 1, 2, mode register (IM0, IM1, IM2)		0, 0, 0	0, 0, 0
Digital port	Output buffer		Off	Off
	Output latch		Clear (0)	Clear (0)
	Input/output mode register (PMGA, PMGB)		0	0
	Pull-up resistor specification register (POGA)		0	0
A/D converter	Mode register (ADM)		04H	04H
	SA register (SA)		Undefined	Undefined
Bit sequential buffer (BSB0-BSB3)			Retained	Undefined

9. INSTRUCTION SET

(1) Operand identifier and its descriptive method

The operands are described in the operand column of each instruction according to the descriptive method for the operand format of the appropriate instructions. Details should be followed by "**RA75X Assembler Package User's Manual, Language**." For descriptions in which alternatives exist, one element should be selected. Capital letters and plus and minus signs are keywords; therefore, they should be described as they are.

For immediate data, the appropriate numerical values or labels should be described.

Identifier	Description	
reg reg1	X, A, B, C, D, E, H, L X, B, C, D, E, H, L	
rp rp1 rp2	XA, BC, DE, HL BC, DE, HL BC, DE	
rpa rpa1	HL, DE, DL DE, DL	
n4 n8	4-bit immediate data or label 8-bit immediate data or label	
mem[Note] bit	8-bit immediate data or label 2-bit immediate data or label	
fmem pmem	FB0H - FBFH, FF0H - FFFH immediate data or label FC0H - FFFH immediate data or label	
addr	μPD75064	0000H - 0FFFH immediate data or label
	μPD75066	0000H - 177FH immediate data or label
	μPD75068	0000H - 1F7FH immediate data or label
caddr	12-bit immediate data or label	
faddr	11-bit immediate data or label	
taddr	20H - 7FH immediate data (however, bit 0 = 0) or label	
PORTn IExxx MBn	PORT0 - PORT6, PORT11 IEBT, IECSI, IET0, IE0, IE1, IE2, IE4, IEW MB0, MB1, MB15	

Note Only even address can be specified for mem when processing 8-bit data.

(2) Symbol definitions in operation description

A : A register; 4-bit accumulator
B : B register
C : C register
D : D register
E : E register
H : H register
L : L register
X : X register
XA : Pair register (XA); 8-bit accumulator
BC : Pair register (BC)
DE : Pair register (DE)

HL : Pair register (HL)
PC : Program counter
SP : Stack pointer
CY : Carry flag; Bit accumulator
PSW : Program status word
MBE : Memory bank enable flag
PORTn : Port n (n = 0 to 6, 11)
IME : Interrupt master enable flag
IE××× : Interrupt enable flag
MBS : Memory bank selection register
PCC : Processor clock control register
. : Address bit delimiter
(××) : Contents addressed by ××
××H : Hexadecimal data

(3) Symbols used for the addressing area column

*1	MB = MBE · MBS (MBS = 0, 1, 15)	Data memory addressing
*2	MB = 0	
*3	MBE = 0: MB = 0 (00H - 7FH) MB = 15 (80H - FFH) MBE = 1: MB = MBS (MBS = 0, 1, 15)	
*4	MB = 15, fmem = FB0H - FBFH, FF0H - FFFH	
*5	MB = 15, pmem = FC0H - FFFH	
*6	μPD75064 addr = 0000H - 0FFFH	Program memory addressing
	μPD75066 addr = 0000H - 177FH	
	μPD75068 addr = 0000H - 1F7FH	
*7	addr = (Current PC) – 15 to (Current PC) – 1 (Current PC) + 2 to (Current PC) + 16	
*8	μPD75064 caddr = 0000H - 0FFFH	
	μPD75066 caddr = 0000H - 0FFFH (PC_{12} = 0) or = 1000H - 177FH (PC_{12} = 1)	
	μPD75068 caddr = 0000H - 0FFFH (PC_{12} = 0) or = 1000H - 1F7FH (PC_{12} = 1)	
*9	faddr = 0000H - 07FFH	
*10	taddr = 0020H - 007FH	

Remarks 1. MB indicates the memory bank that can be accessed.
2. For *2, MB = 0 regardless of MBE and MBS settings.
3. For *4 and *5, MB = 15 regardless of MBE and MBS.
4. For *6 to *10, each addressable area is indicated.

(4) Description of machine cycle column

S indicates the number of machine cycles necessary for skipping any skip instruction. The value of S changes as follows:

- When no skip is performed ..... S = 0
- When a 1-byte or 2-byte instruction is skipped ..... S = 1
- When a 3-byte instruction (BR !addr [Note] , CALL !addr instruction) is skipped ..... S = 2

Note BR !addr instruction is not provided in the μPD75064.

Caution The GETI instruction is skipped in one machine cycle.

One machine cycle is equivalent to one CPU clock Φ cycle. Therefore, the length of the machine cycle can be selected from three different lengths by the PCC setting.

★ **(5) Representative products listed in operation column**

The products listed in the operation column (μPD75064, 75066, 75068) stand for the products listed below.

μPD75064	μPD75064, μPD75064(A)
μPD75066	μPD75066, μPD75066(A)
μPD75068	μPD75068, μPD75068(A)

Group	Mnemonic	Operand	Bytes	Machine cycle	Operation	Addressing area	Skip condition
Transfer	MOV	A, #n4	1	1	A ← n4		String A
		reg1, #n4	2	2	reg1 ← n4		
		XA, #n8	2	2	XA ← n8		String A
		HL, #n8	2	2	HL ← n8		String B
		rp2, #n8	2	2	rp2 ← n8		
		A, @HL	1	1	A ← (HL)	*1	
		A, @rpa1	1	1	A ← (rpa1)	*2	
		XA, @HL	2	2	XA ← (HL)	*1	
		@HL, A	1	1	(HL) ← A	*1	
		@HL, XA	2	2	(HL) ← XA	*1	
		A, mem	2	2	A ← (mem)	*3	
		XA, mem	2	2	XA ← (mem)	*3	
		mem, A	2	2	(mem) ← A	*3	
		mem, XA	2	2	(mem) ← XA	*3	
		A, reg	2	2	A ← reg		
		XA, rp	2	2	XA ← rp		
		reg1, A	2	2	reg1 ← A		
		rp1, XA	2	2	rp1 ← XA		
	XCH	A, @HL	1	1	A ↔ (HL)	*1	
		A, @rpa1	1	1	A ↔ (rpa1)	*2	
		XA, @HL	2	2	XA ↔ (HL)	*1	
		A, mem	2	2	A ↔ (mem)	*3	
		XA, mem	2	2	XA ↔ (mem)	*3	
		A, reg1	1	1	A ↔ reg1		
		XA, rp	2	2	XA ↔ rp		
Table reference	MOVT	XA, @PCDE	1	3	• **μPD75064** XA ← $(PC_{11-8} + DE)_{ROM}$ • **μPD75066, 75068** XA ← $(PC_{12-8} + DE)_{ROM}$		
		XA, @PCXA	1	3	• **μPD75064** XA ← $(PC_{11-8} + XA)_{ROM}$ • **μPD75066, 75068** XA ← $(PC_{12-8} + XA)_{ROM}$		
Arithmetic	ADDS	A, #n4	1	1 + S	A ← A + n4		carry
		A, @HL	1	1 + S	A ← A + (HL)	*1	carry
	ADDC	A, @HL	1	1	A, CY ← A + (HL) + CY	*1	
	SUBS	A, @HL	1	1 + S	A ← A – (HL)	*1	borrow
	SUBC	A, @HL	1	1	A, CY ← A – (HL) – CY	*1	

Group	Mnemonic	Operand	Bytes	Machine cycle	Operation	Addressing area	Skip condition
Arithmetic	AND	A, #n4	2	2	A ← A ∧ n4		
		A, @HL	1	1	A ← A ∧ (HL)	*1	
	OR	A, #n4	2	2	A ← A ∨ n4		
		A, @HL	1	1	A ← A ∨ (HL)	*1	
	XOR	A, #n4	2	2	A ← A ∀ n4		
		A, @HL	1	1	A ← A ∀ (HL)	*1	
Accumulator manipulation	RORC	A	1	1	$CY \leftarrow A_0$, $A_3 \leftarrow CY$, $A_{n-1} \leftarrow A_n$		
	NOT	A	2	2	$A \leftarrow \overline{A}$		
Increment/ decrement	INCS	reg	1	1 + S	reg ← reg + 1		reg = 0
		@HL	2	2 + S	(HL) ← (HL) + 1	*1	(HL) = 0
		mem	2	2 + S	(mem) ← (mem) + 1	*3	(mem) = 0
	DECS	reg	1	1 + S	reg ← reg – 1		reg = FH
Comparison	SKE	reg, #n4	2	2 + S	Skip if reg = n4		reg = n4
		@HL, #n4	2	2 + S	Skip if (HL) = n4	*1	(HL) = n4
		A, @HL	1	1 + S	Skip if A = (HL)	*1	A = (HL)
		A, reg	2	2 + S	Skip if A = reg		A = reg
Carry flag manipulation	SET1	CY	1	1	CY ← 1		
	CLR1	CY	1	1	CY ← 0		
	SKT	CY	1	1 + S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	$CY \leftarrow \overline{CY}$		
Memory bit manipulation	SET1	mem.bit	2	2	(mem.bit) ← 1	*3	
		fmem.bit	2	2	(fmem.bit) ← 1	*4	
		pmem.@L	2	2	$(pmem_{7-2} + L_{3-2}.bit(L_{1-0})) \leftarrow 1$	*5	
		@H+mem.bit	2	2	$(H + mem_{3-0}.bit) \leftarrow 1$	*1	
	CLR1	mem.bit	2	2	(mem.bit) ← 0	*3	
		fmem.bit	2	2	(fmem.bit) ← 0	*4	
		pmem.@L	2	2	$(pmem_{7-2} + L_{3-2}.bit(L_{1-0})) \leftarrow 0$	*5	
		@H+mem.bit	2	2	$(H + mem_{3-0}.bit) \leftarrow 0$	*1	
	SKT	mem.bit	2	2 + S	Skip if (mem.bit) = 1	*3	(mem.bit) = 1
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 1	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if $(pmem_{7-2} + L_{3-2}.bit(L_{1-0})) = 1$	*5	(pmem.@L) = 1
		@H+mem.bit	2	2 + S	Skip if $(H + mem_{3-0}.bit) = 1$	*1	(@H + mem.bit) = 1
	SKF	mem.bit	2	2 + S	Skip if (mem.bit) = 0	*3	(mem.bit) = 0
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 0	*4	(fmem.bit) = 0
		pmem.@L	2	2 + S	Skip if $(pmem_{7-2} + L_{3-2}.bit(L_{1-0})) = 0$	*5	(pmem.@L) = 0
		@H+mem.bit	2	2 + S	Skip if $(H + mem_{3-0}.bit) = 0$	*1	(@H + mem.bit) = 0
	SKTCLR	fmem.bit	2	2 + S	Skip if (fmem.bit) = 1 and clear	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if $(pmem_{7-2} + L_{3-2}.bit(L_{1-0})) = 1$ and clear	*5	(pmem.@L) = 1
		@H+mem.bit	2	2 + S	Skip if $(H + mem_{3-0}.bit) = 1$ and clear	*1	(@H + mem.bit) = 1

Group	Mnemonic	Operand	Bytes	Machine cycle	Operation	Addressing area	Skip condition
Memory bit manipulation	AND1	CY, fmem.bit	2	2	CY ← CY ∧ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∧ ($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0}))	*5	
		CY, @H+mem.bit	2	2	CY ← CY ∧ (H + mem_{3-0}.bit)	*1	
	OR1	CY, fmem.bit	2	2	CY ← CY ∨ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∨ ($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0}))	*5	
		CY, @H+mem.bit	2	2	CY ← CY ∨ (H + mem_{3-0}.bit)	*1	
	XOR1	CY, fmem.bit	2	2	CY ← CY ⊻ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ⊻ ($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0}))	*5	
		CY, @H+mem.bit	2	2	CY ← CY ⊻ (H + mem_{3-0}.bit)	*1	
Branch	BR	addr	–	–	• **μPD75064** PC_{11-0} ← addr (Appropriate instructions are selected from BRCB !caddr, and BR $addr by the assembler.) • **μPD75066, 75068** PC_{12-0} ← addr (Appropriate instructions are selected from BR !addr, BRCB !caddr, and BR $addr by the assembler.)	*6	
		!addr **Note**	3	3	• **μPD75066, 75068** PC_{12-0} ← addr	*6	
		$addr	1	2	• **μPD75064** PC_{11-0} ← addr • **μPD75066, 75068** PC_{12-0} ← addr	*7	
	BRCB	!caddr	2	2	• **μPD75064** PC_{11-0} ← $caddr_{11-0}$ • **μPD75066, 75068** PC_{12-0} ← PC_{12} + $caddr_{11-0}$	*8	
Subroutine stack control	CALL	!addr	3	3	• **μPD75064** (SP – 4)(SP – 1)(SP – 2) ← PC_{11-0} (SP – 3) ← MBE, 0, 0, 0 PC_{11-0} ← addr, SP ← SP – 4 • **μPD75066, 75068** (SP – 4)(SP – 1)(SP – 2) ← PC_{11-0} (SP–3) ← MBE, 0, 0, PC_{12} PC_{12-0} ← addr, SP ← SP – 4	*6	

Note BR !addr instruction is not provided in the μPD75064.

Group	Mnemonic	Operand	Bytes	Machine cycle	Operation	Addressing area	Skip condition
Subroutine stack control	CALLF	!faddr	2	2	• **μPD75064** (SP – 4)(SP – 1)(SP – 2) ← PC_{11-0} (SP–3) ← MBE, 0, 0, 0 PC_{11-0} ← 00, faddr, SP ← SP – 4 • **μPD75066, 75068** (SP – 4)(SP – 1)(SP – 2) ← PC_{11-0} (SP–3) ← MBE, 0, 0, PC_{12} PC_{12-0} ← 00, faddr, SP ← SP – 4	*9	
	RET		1	3	• **μPD75064** MBE, 0, 0, 0 ← (SP + 1) PC_{11-0} ← (SP)(SP + 3)(SP + 2) SP ← SP + 4 • **μPD75066, 75068** MBE, 0, 0, PC_{12} ← (SP + 1) PC_{11-0} ← (SP)(SP + 3)(SP + 2) SP ← SP + 4		
	RETS		1	3 + S	• **μPD75064** MBE, 0, 0, 0 ← (SP + 1) PC_{11-0} ← (SP)(SP + 3)(SP + 2) SP ← SP + 4, then skip unconditionally • **μPD75066, 75068** MBE, 0, 0, PC_{12} ← (SP + 1) PC_{11-0} ← (SP)(SP + 3)(SP + 2) SP ← SP + 4, then skip unconditionally		Unconditional
	RETI		1	3	• **μPD75064** MBE, 0, 0, 0 ← (SP + 1) PC_{11-0} ← (SP)(SP + 3)(SP + 2) PSW ← (SP + 4)(SP + 5), SP ← SP + 6 • **μPD75066, 75068** MBE, 0, 0, PC_{12} ← (SP + 1) PC_{11-0} ← (SP)(SP + 3)(SP + 2) PSW ← (SP + 4)(SP + 5), SP ← SP + 6		
	PUSH	rp	1	1	(SP – 1)(SP – 2) ← rp, SP ← SP – 2		
		BS	2	2	(SP – 1) ← MBS, (SP – 2) ← 0, SP ← SP – 2		
	POP	rp	1	1	rp ← (SP + 1)(SP), SP ← SP + 2		
		BS	2	2	MBS ← (SP + 1), SP ← SP + 2		

Group	Mnemonic	Operand	Bytes	Machine cycle	Operation	Addressing area	Skip condition
Interrupt control	EI		2	2	IME ← 1		
		IExxx	2	2	IExxx ← 1		
	DI		2	2	IME ← 0		
		IExxx	2	2	IExxx ← 0		
Input/output	IN	A, PORTn	2	2	A ← PORTn (n = 0 - 6, 11)		
		XA, PORTn	2	2	XA ← PORTn+1,PORTn (n = 4, 6)		
	OUT	PORTn, A	2	2	PORTn ← A (n = 2 - 6)		
		PORTn, XA	2	2	PORTn+1, PORTn ← XA (n = 4, 6)		
CPU control	HALT		2	2	Set HALT Mode (PCC.2 ← 1)		
	STOP		2	2	Set STOP Mode (PCC.3 ← 1)		
	NOP		1	1	No Operation		
Special	SEL	MBn	2	2	MBS ← n (n = 0, 1, 15)		
	GETI	taddr	1	3	• **μPD75064** • For the TBR instruction $PC_{11-0} \leftarrow (taddr)_{3-0} + (taddr + 1)$	*10	
					• For the TCALL instruction $(SP - 4)(SP - 1)(SP - 2) \leftarrow PC_{11-0}$ $(SP - 3) \leftarrow$ MBE, 0, 0, 0 $PC_{11-0} \leftarrow (taddr)_{3-0} + (taddr + 1)$ $SP \leftarrow SP - 4$		
					• For other than the TBR and TCALL instruction (taddr) (taddr + 1) is executed.		Depends on the reference instruction.
					• **μPD75066, 75068** • For the TBR instruction $PC_{12-0} \leftarrow (taddr)_{4-0} + (taddr + 1)$		
					• For the TCALL instruction $(SP - 4)(SP - 1)(SP - 2) \leftarrow PC_{11-0}$ $(SP - 3) \leftarrow$ MBE, 0, 0, PC_{12} $PC_{12-0} \leftarrow (taddr)_{4-0} + (taddr + 1)$ $SP \leftarrow SP - 4$		
					• For other than the TBR and TCALL instruction (taddr) (taddr + 1) is executed.		Depends on the reference instruction.

Caution When executing the IN/OUT instruction, MBE must be set to 0, or MBE and MBS must be set to 1 and 15, respectively.

10. ELECTRICAL SPECIFICATIONS

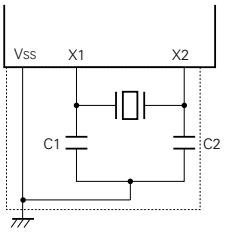
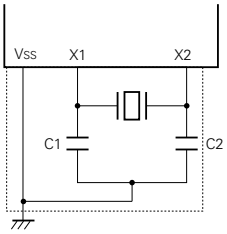
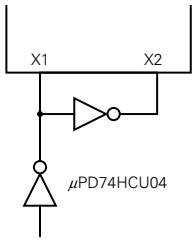
Absolute Maximum Ratings (T_a = 25 °C)

Parameter	Symbol	Conditions		Ratings	Unit
Power supply voltage	V_{DD}			–0.3 to +7.0	V
Input voltage	V_{I1}	Except ports 4 and 5		–0.3 to V_{DD}+0.3	V
	V_{I2}	Ports 4 and 5	On-chip pull-up resistor	–0.3 to V_{DD}+0.3	V
			N-ch open–drain	–0.3 to +11	V
Output voltage	V_O			–0.3 to V_{DD}+0.3	V
High level output current	I_{OH}	Per pin		–10	mA
		All output pins		–30	mA
Low level output current	I_{OL}**Note**	One pin of ports 0, 3, 4, and 5	Peak value	30	mA
			rms value	15	mA
		One pin of ports 2 and 6	Peak value	20	mA
			rms value	5	mA
		Total of ports 0, 3, 4 and 5	Peak value	160	mA
			rms value	120	mA
		Total of ports 2 and 6	Peak value	30	mA
			rms value	20	mA
Operating ambient temperature	T_{opt}			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note Rms value is calculated using the following expression: [rms value] = [peak value] × $\sqrt{\text{duty ratio}}$

Caution If any of the items exceeds the absolute maximum ratings, even momentarily, this may damage product quality. The absolute maximum ratings are values that may physically damage products. Be sure to use the products within the ratings.

Main System Clock Oscillator Characteristics (T_a = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Resonator	Recommended Constant	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_x)Note1	V_{DD} = Oscillation voltage range	1.0		5.0 Note3	MHz
		Oscillation stabilization timeNote2				4	ms
Crystal resonator		Oscillation frequency (f_x)Note1		1.0	4.19	5.0 Note3	MHz
		Oscillation stabilization timeNote2	V_{DD} = 4.5 to 6.0 V			10	ms
						30	ms
External clock		X1 input frequency (f_x)Note1		1.0		5.0 Note3	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		100		500	ns

Notes 1. The oscillation frequency indicates characteristics of the oscillator only. For the instruction execution time, refer to the AC characteristics.

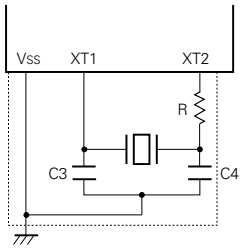
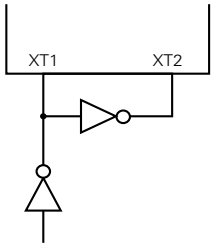
2. The oscillation stabilization time is the required time for oscillation to stabilize after the voltage level of V_{DD} reaches the MIN. value of the oscillation voltage range or releasing the STOP mode.

3. When the oscillation frequency is "4.19 MHz < fx ≤ 5.0 MHz", selection of "PCC = 0011" with 1 machine cycle of less than 0.95 μs for instruction execution time is not possible.

Caution If the main system clock oscillator is used, the wiring in the area indicated with broken lines in the recommended constant illustration should be routed observing the points described below to avoid influence of wiring capacitance, etc.

- **Route as short as possible.**
- **Do not cross the wires.**
- **Route the wires away from lines where changing high current flows.**
- **Make the connecting point of the capacitors in the oscillation circuit to have always the same potential as V_{SS}. Do not route the connecting point to another ground pattern on the board where high current flows.**
- **Do not use the oscillator as a signal source of other circuits.**

Subsystem Clock Oscillator Characteristics (T_a = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Resonator	Recommended Constant	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})Note1		32	32.768	50	kHz
		Oscillation stabilization time Note2	V_{DD} = 4.5 to 6.0 V		1.0	2	s
						10	s
External clock		XT1 input frequency (f_{XT})Note1		32		100	kHz
		XT1 input high-/low-level width (t_{XTH},t_{XTL})		5		15	μs

Notes 1. The oscillation frequency indicates characteristics of the oscillator only. For the instruction execution time, refer to the AC characteristics.

2. The oscillation stabilization time is the required time for oscillation to stabilize after the voltage level of V_{DD} reaches the MIN. value of the oscillation voltage range.

Caution If the subsystem clock oscillator is used, the wiring in the area indicated with broken lines in the recommended constant illustration should be routed observing the points described below to avoid influence of wiring capacitance, etc.

- **Route as short as possible.**
- **Do not cross the wires.**
- **Route the wires away from lines where changing high current flows.**
- **Make the connecting point of the capacitors in the oscillation circuit to have always the same potential as V_{SS}. Do not route the connecting point to another ground pattern on the board where high current flows.**
- **Do not use the oscillator as a signal source of other circuits.**

Especially when using the subsystem clock, be sure to design wiring so as to minimize noise. The subsystem clock oscillator uses a low-amplification circuit to minimize power dissipation. As a result, malfunctions due to noise are more liable to occur than with the main system clock oscillator.

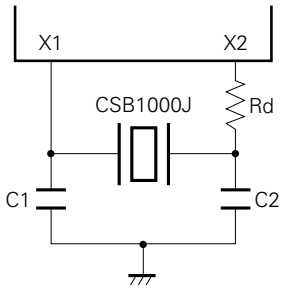
Recommended Oscillator Constant

Main system clock: Ceramic (T_a = –40 to +85°C)

Manufacturer	Part number	Frequency (MHz)	Recommended circuit constant		Oscillation voltage range		Remarks
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
KYOCERA	KBR-2.0 MS	2.00	47	47	2.5	6.0	
	PBRC 2.00A						
	KBR-4.19 MSA	4.19	33	33	2.7		
	PBRC 4.19A						
	KBR-4.19 MKS	4.19	Internal	Internal			
	KBR-4.19 MWS						
MURATA Manufacturing	CSB1000J[Note]	1.00	100	100	2.7	6.0	Rd = 5.6 kΩ
	CSA2.0MG040	2.00	100	100	2.8		
	CST2.0MGW093		Internal	Internal	2.7		
	CSAC2.0MGCME		15	15			Chip product
	CSA4.19MGU	4.19	30	30			
	CST4.19MGUW		Internal	Internal			

Note When the Murata's CSB1000J ceramic resonator (1.00 MHz) is used, the limiting resistor (Rd = 5.6 kΩ) is required (see figure below). When using other recommended resonators, the limiting resistor is not required.

Example of Recommended Main System Clock Circuit (when using CSB1000J of Murata)



Main System Clock: XTAL

Manufacturer	Part number	Frequency (MHz)	Recommended circuit constant		Oscillation voltage range		Remarks
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
DAISINKU	HC-49/U	2.00	8	8	2.8	6.0	(T_a = –40 to +85°C)
		4.19			2.7		
		5.00					
KINSEKI	HC-49/U	2.00	22	22	3.1	6.0	(T_a = –20 to +70°C)
		4.19			3.2		

DC Characteristics (T_a = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH1}	Ports 2, 3, and 11		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0,1,6, $\overline{RESET}$		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	Ports 4 and 5	On-chip pull-up resistor	0.7 V_{DD}		V_{DD}	V
			N-ch open-drain	0.7 V_{DD}		10	V
	V_{IH4}	X1, X2, XT1, XT2		V_{DD} –0.5		V_{DD}	V
Low-level input voltage	V_{IL1}	Ports 2 through 5 and 11		0		0.3 V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, $\overline{RESET}$		0		0.2 V_{DD}	V
	V_{IL3}	X1, X2, XT1, XT2		0		0.4	V
High-level output voltage	V_{OH}	V_{DD} = 4.5 to 6.0 V , I_{OH} = –1 mA		V_{DD} –1.0			V
		I_{OH} = –100 μA		V_{DD} –0.5			V
Low-level output voltage	V_{OL}	Ports 4 and 5	V_{DD} = 4.5 to 6.0 V I_{OL} = 15 mA		0.7	2.0	V
		Port 3	V_{DD} = 4.5 to 6.0 V I_{OL} = 15 mA		0.3	2.0	V
		V_{DD} = 4.5 to 6.0 V , I_{OL} = 1.6 mA				0.4	V
		I_{OL} = 400 μA				0.5	V
		SB0, SB1	N-ch open-drain pull-up resistor ≥ 1 kΩ			0.2 V_{DD}	V
High-level input leakage current	I_{LIH1}	V_I = V_{DD}	Other than pins below			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
	I_{LIH3}	V_I = 10 V	Ports 4 and 5 (N-ch open-drain)			20	μA
Low-level input leakage current	I_{LIL1}	V_I = 0 V	Other than pins below			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
High-level output leakage current	I_{LOH1}	V_O = V_{DD}				3	μA
	I_{LOH2}	V_O = 10 V	Ports 4 and 5 (N-ch open-drain)			20	μA
Low-level output leakage current	I_{LOL}	V_O = 0 V				–3	μA
On-chip pull-up resistor	R_{U1}	P01, 02, 03, Ports 1, 2, 3 and 6 V_I = 0 V	V_{DD} = 5.0 V ±10 %	15	40	80	kΩ
			V_{DD} = 3.0 V ±10 %	30		300	kΩ
	R_{U2}	Ports 4 and 5 V_O = V_{DD} – 2.0 V	V_{DD} = 5.0 V ±10 %	15	40	70	kΩ
			V_{DD} = 3.0 V ±10 %	10		60	kΩ

(Cont.)

DC Characteristics (T_a = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current Note1	I_{DD1}	4.19 MHz Note2 crystal oscillation C1 = C2 = 22 pF	V_{DD} = 5.0 V ±10 % Note3			2.0	6.0	mA
			V_{DD} = 3.0 V ±10 % Note4			0.2	0.6	mA
	I_{DD2}		HALT mode	V_{DD} = 5.0 V ±10 %		400	1200	μA
				V_{DD} = 3.0 V ±10 %		120	400	μA
	I_{DD3}	32.768 kHz Note5 crystal oscillation	V_{DD} = 3.0 V ±10 %			10	30	μA
	I_{DD4}		HALT mode	V_{DD} = 3.0 V ±10 %		5	15	μA
	I_{DD5}	XT1 = 0 V STOP mode	V_{DD} = 5.0 V ±10 %			0.5	20	μA
			V_{DD} = 3.0 V ±10 %			0.1	10	μA
				T_a = 25 °C		0.1	5	μA

Notes 1. Current which flows in the on-chip pull-up resistor is not included.

2. Including oscillation of the subsystem clock.

3. When the processor clock control register (PCC) is set to 0011 and the device is operated in the high-speed mode.

4. When PCC is set to 0000 and the device is operated in the low-speed mode.

5. When the system clock control register (SCC) is set to 1001 and the device is operated on the sub-system clock, with main system clock oscillation stopped.

Capacitance (T_a = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz Unmeasured pins returned to 0 V.			15	pF
Output capacitance	C_O				15	pF
I/O capacitance	C_{IO}				15	pF

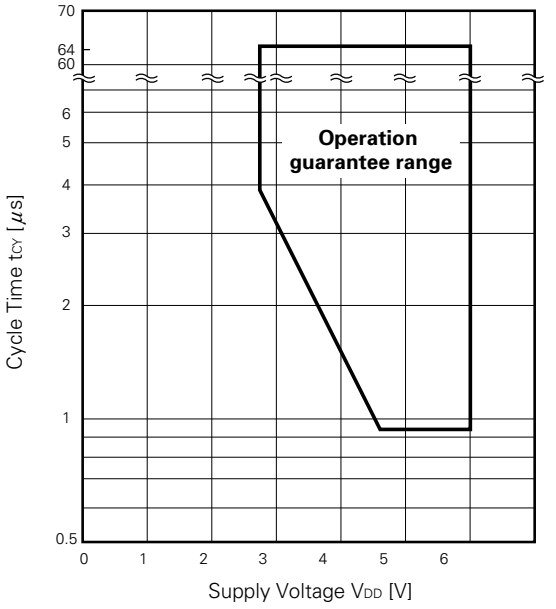
AC Characteristics (T_a = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
CPU clock cycle time Note1 (minimum instruction execution time = 1 machine cycle)	t_{CY}	Operating on main system clock	V_{DD} = 4.5 to 6.0 V	0.95		64	μs
				3.8		64	μs
		Operating on subsystem clock		114	122	125	μs
TI0 input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		1	MHz
				0		275	kHz
TI0 input high and low level width	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		0.48			μs
				1.8			μs
Interrupt input high and low level width	t_{INTH}, t_{INTL}	INT0		**Note2**			μs
		INT1, INT2, INT4		10			μs
		KR0 to KR3		10			μs
$\overline{\text{RESET}}$ low level width	t_{RSL}			10			μs

Notes 1. The cycle time (minimum instruction execution time) of the CPU clock (Φ) is determined by the oscillation frequency of the connected resonator, the system clock control register (SCC), and the processor clock control register (PCC). The figure at the right indicates the cycle time t_{CY} versus supply voltage V_{DD} characteristic with the main system clock operating.

2. $2t_{CY}$ or 128/f_X is set by setting the interrupt mode register (IM0).

t_{CY} vs V_{DD}
(Operating on Main System Clock)



Serial Transfer Operation

2-Wire and 3-Wire Serial I/O Modes ($\overline{SCK}$ ... Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high- and low-level width	t_{KL1}, t_{KH1}	V_{DD} = 4.5 to 6.0 V		t_{KCY1}/2-50			ns
				t_{KCY1}/2-150			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK1}			150			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI1}			400			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO1}	R_L = 1 kΩ, C_L = 100 pF Note	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns

2-Wire and 3-Wire Serial I/O Modes ($\overline{SCK}$ ... External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high- and low-level width	t_{KL2}, t_{KH2}	V_{DD} = 4.5 to 6.0 V		400			ns
				1600			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK2}			100			ns
SI hold time (from $\overline{SCK}$ ↑)	t_{KSI2}			400			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO2}	R_L = 1 kΩ, C_L = 100 pF Note	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns

Note R_L and C_L are load resistance and load capacitance of the SO output line, respectively.

SBI Mode ($\overline{SCK}$ ... Internal clock output (Master))

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high- and low-level width	t_{KL3} t_{KH3}	V_{DD} = 4.5 to 6.0 V		t_{KCY3}/2-50			ns
				t_{KCY3}/2-150			ns
SB0, 1 setup time (to $\overline{SCK}$ ↑)	t_{SIK3}			150			ns
SB0, 1 hold time (from $\overline{SCK}$ ↑)	t_{KSI3}			t_{KCY3}/2			ns
SB0, 1 output delay time from $\overline{SCK}$ ↓	t_{KSO3}	R_L = 1 kΩ, C_L = 100 pF Note	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
SB0, 1 ↓ from $\overline{SCK}$ ↑	t_{KSB}			t_{KCY3}			ns
$\overline{SCK}$ ↓ from SB0, 1 ↓	t_{SBK}			t_{KCY3}			ns
SB0, 1 low-level width	t_{SBL}			t_{KCY3}			ns
SB0, 1 high-level width	t_{SBH}			t_{KCY3}			ns

SBI Mode ($\overline{SCK}$ ... External clock input (Slave))

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high- and low-level width	t_{KL4} t_{KH4}	V_{DD} = 4.5 to 6.0 V		400			ns
				1600			ns
SB0, 1 setup time (to $\overline{SCK}$ ↑)	t_{SIK4}			100			ns
SB0, 1 hold time (from $\overline{SCK}$ ↑)	t_{KSI4}			t_{KCY4}/2			ns
SB0, 1 output delay time from $\overline{SCK}$ ↓	t_{KSO4}	R_L = 1 kΩ, C_L = 100 pF Note	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
SB0, 1 ↓ from $\overline{SCK}$ ↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK}$ ↓ from SB0, 1 ↑	t_{SBK}			t_{KCY4}			ns
SB0, 1 low-level width	t_{SBL}			t_{KCY4}			ns
SB0, 1 high-level width	t_{SBH}			t_{KCY4}			ns

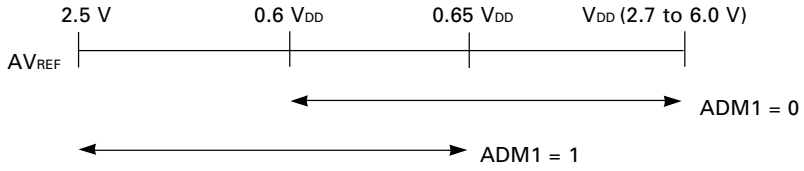
Note R_L and C_L are load resistance and load capacitance, respectively, for the SB0 and SB1 output lines.

A/D Converter (T_a = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution				8	8	8	bit
Absolute accuracy Note1		2.5 V ≤ AV_{REF} ≤ V_{DD} Note2	–10 ≤ T_a ≤ +85 °C			±1.5	LSB
			–40 ≤ T_a < –10 °C			±2.0	LSB
Conversion time Note3	t_{CONV}					168/fx	μs
Sampling time Note4	t_{SAMP}					44/fx	μs
Reference input voltage	AV_{REF}			2.5		V_{DD}	V
Analog input voltage	V_{IAN}			AV_{SS}		AV_{REF}	V
Analog input impedance	R_{AN}				1000		MΩ
AV_{REF} current	AI_{REF}				0.7	2.0	mA

Notes 1. Absolute accuracy excluding quantization error (±1/2 LSB)

2. ADM1 should be set according to the A/D converter reference voltage (AV_{REF}) as follows:
When the AV_{REF} is between 0.6V_{DD} and 0.65V_{DD}, either 1 or 0 can be set.

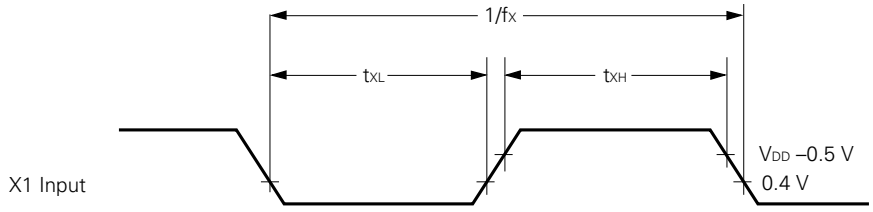


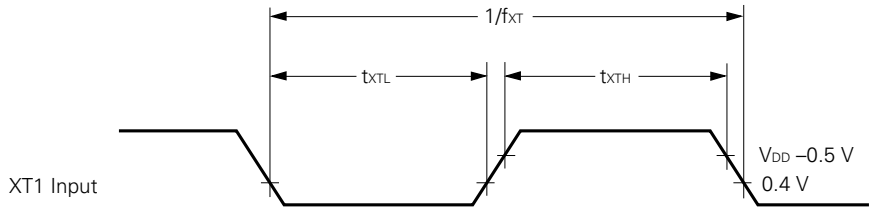
3. The time from conversion start instruction execution to conversion end (EOC=1) (40.1 μs : at f_X = 4.19 MHz)

4. The time from conversion start instruction execution to sampling end (10.5 μs : at f_X = 4.19 MHz)

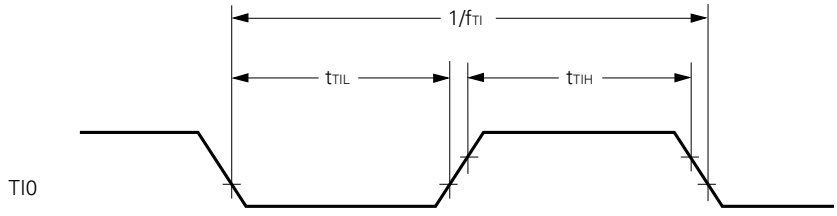
AC Timing Test Points (excluding X1 and XT1 inputs):

Clock Timings:



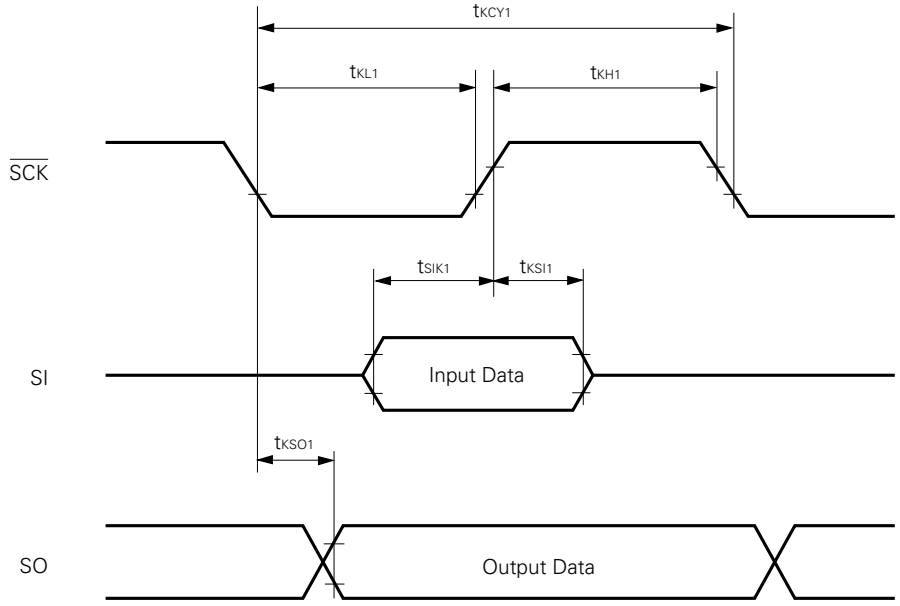


TI0 Timings:

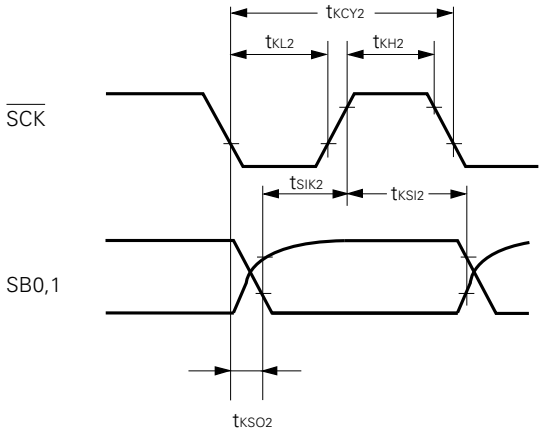


Serial Transfer Timing

3-wire serial I/O mode:

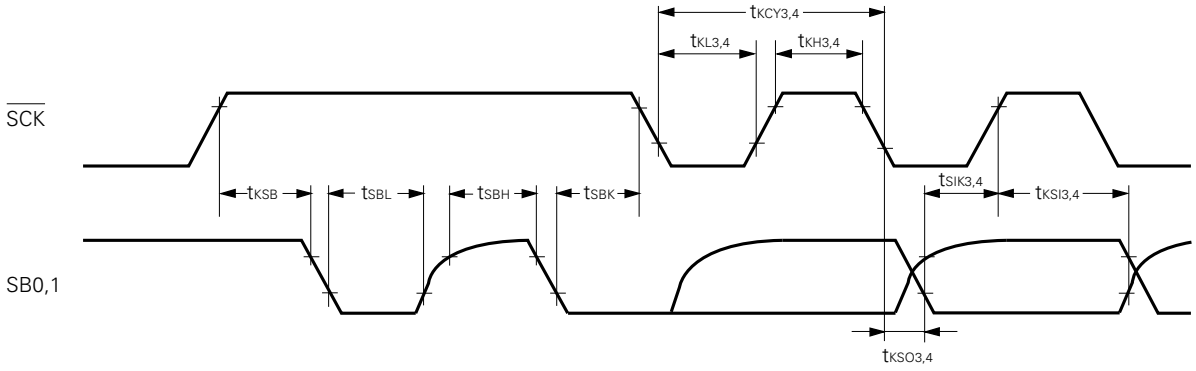


2-wire serial I/O mode:

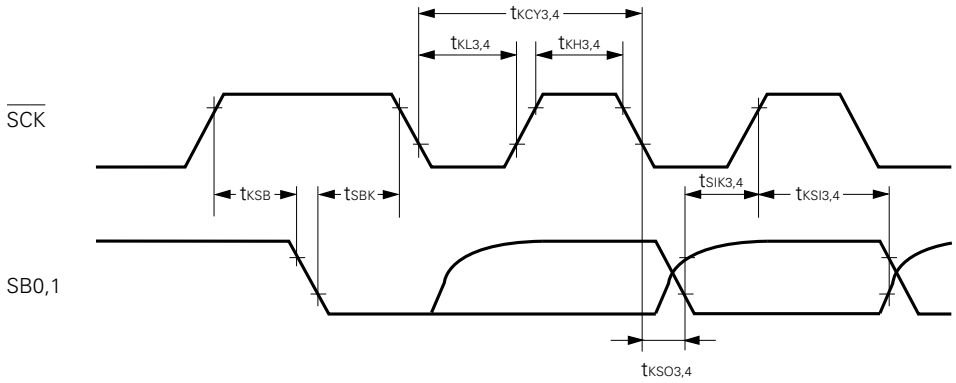


Serial Transfer Timing

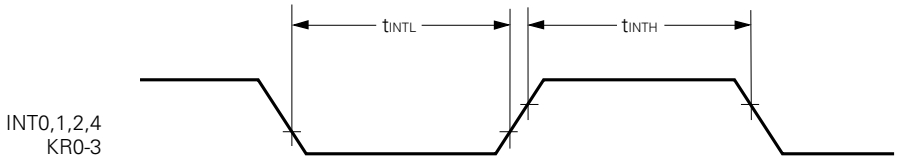
Bus release signal transfer:



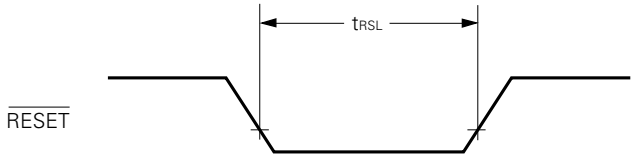
Command signal transfer:



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_a = –40 to +85 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		6.0	V
Data retention supply current Note1	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release signal setting time	t_{SREL}		0			μs
Oscillation stabilization wait time Note2	t_{WAIT}	Release by $\overline{RESET}$		2^{17}/fx		ms
		Release by interrupt request		**Note3**		ms

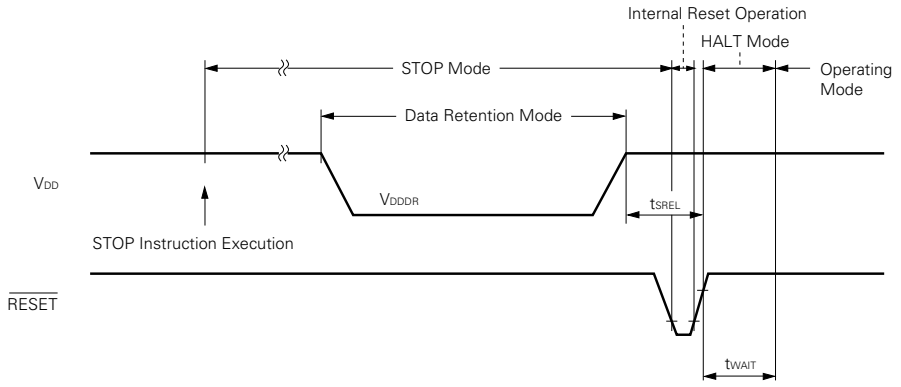
Notes 1. Current which flows in the on-chip pull-up resistor is not included.

2. The oscillation stabilization wait time is the time during which the CPU operation is stopped to prevent unstable operation at the oscillation start.

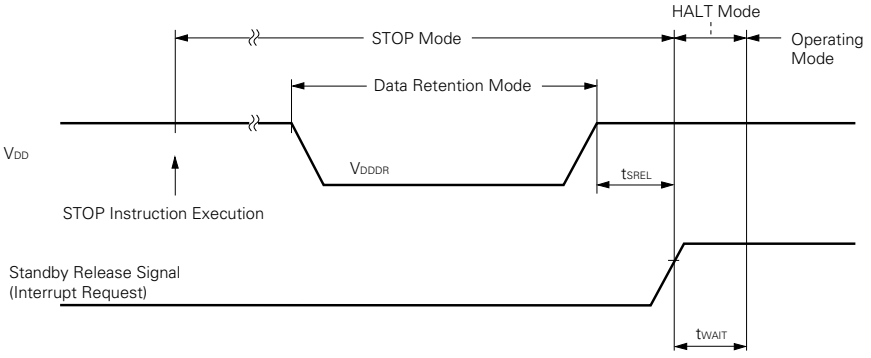
3. Depends on the basic interval timer mode register (BTM) settings (See the table below).

BTM3	BTM2	BTM1	BTM0	Wait Time (Figures in parentheses are for operation at fx = 4.19 MHz)
—	0	0	0	2^{20}/fx (approx. 250 ms)
—	0	1	1	2^{17}/fx (approx. 31.3 ms)
—	1	0	1	2^{15}/fx (approx. 7.82 ms)
—	1	1	1	2^{13}/fx (approx. 1.95 ms)

Data Retention Timing (STOP mode release by $\overline{RESET}$)

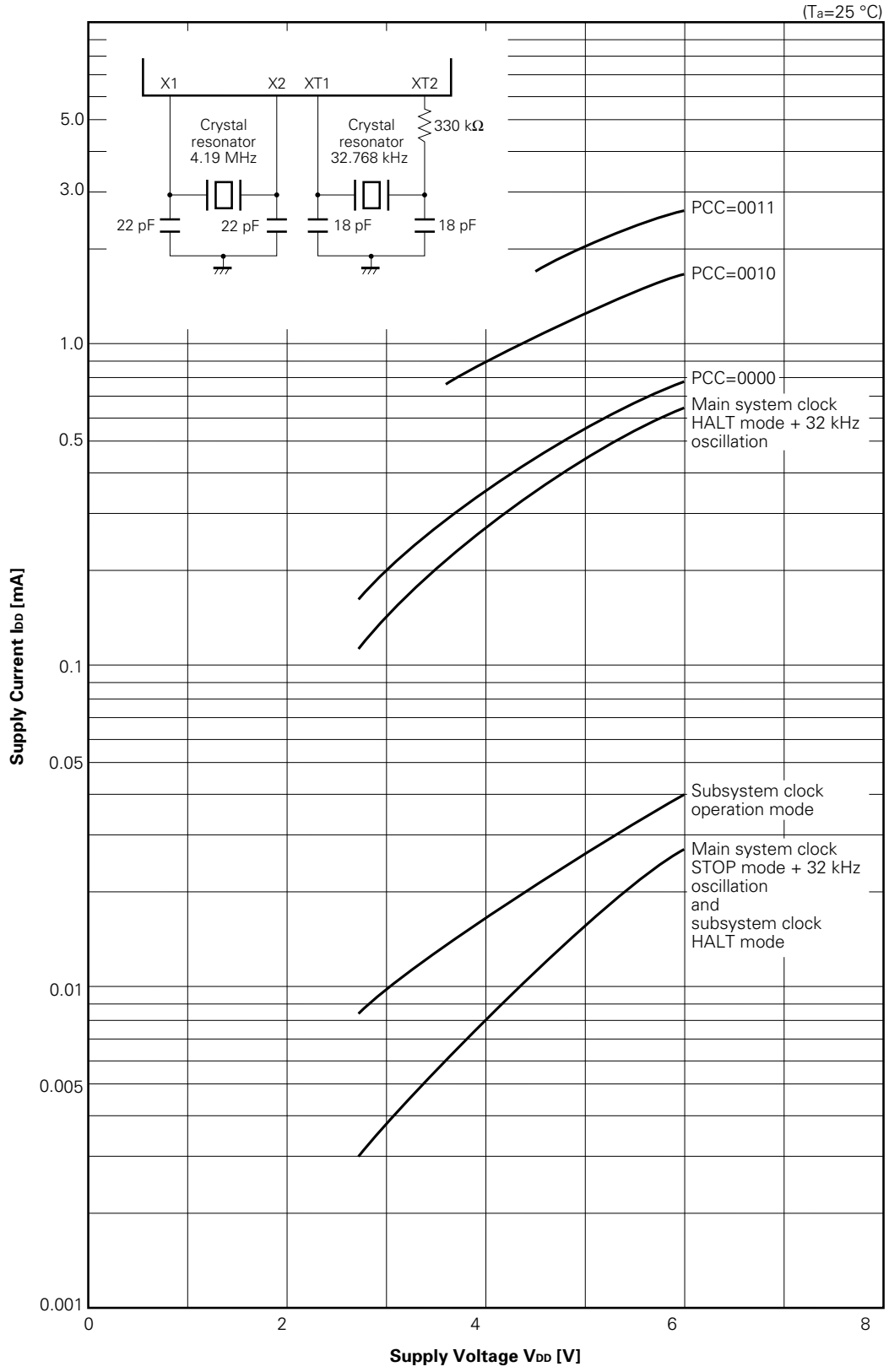


Data Retention Timing (Standby release signal: STOP mode release by interrupt signal)

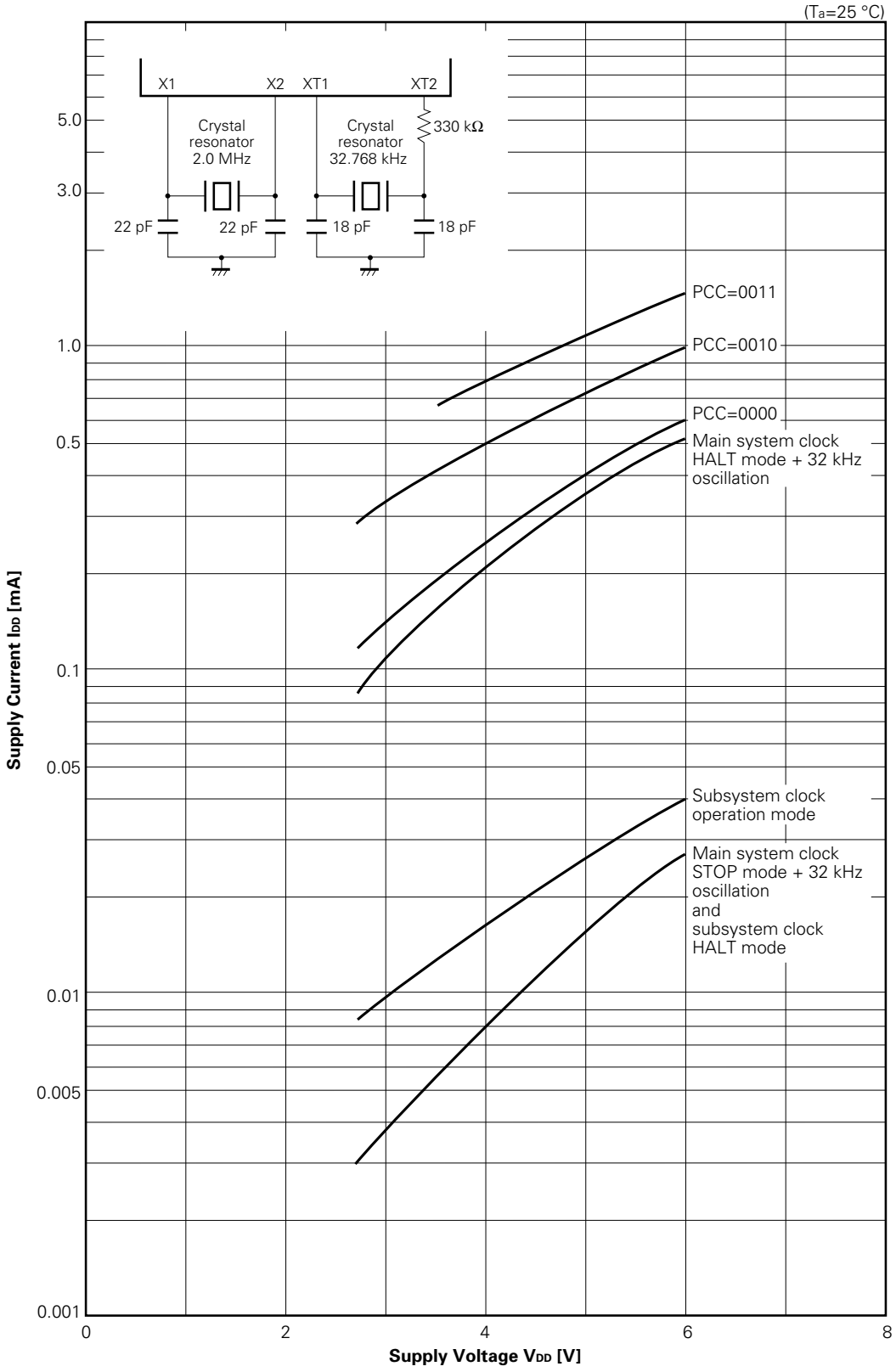


11. CHARACTERISTIC CURVES (FOR REFERENCE ONLY)

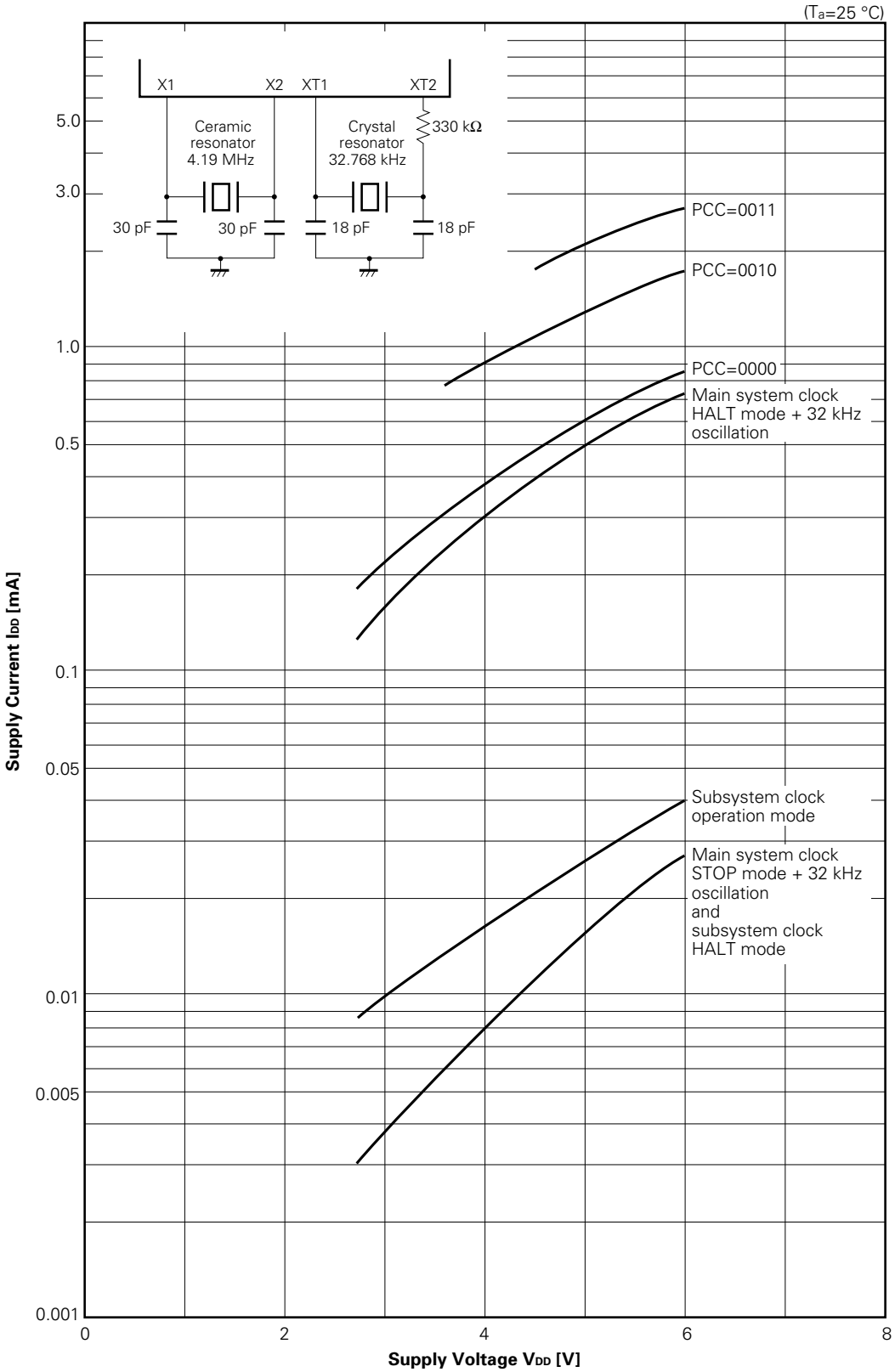
I_{DD} vs V_{DD} (Main system clock: 4.19-MHz crystal resonator)



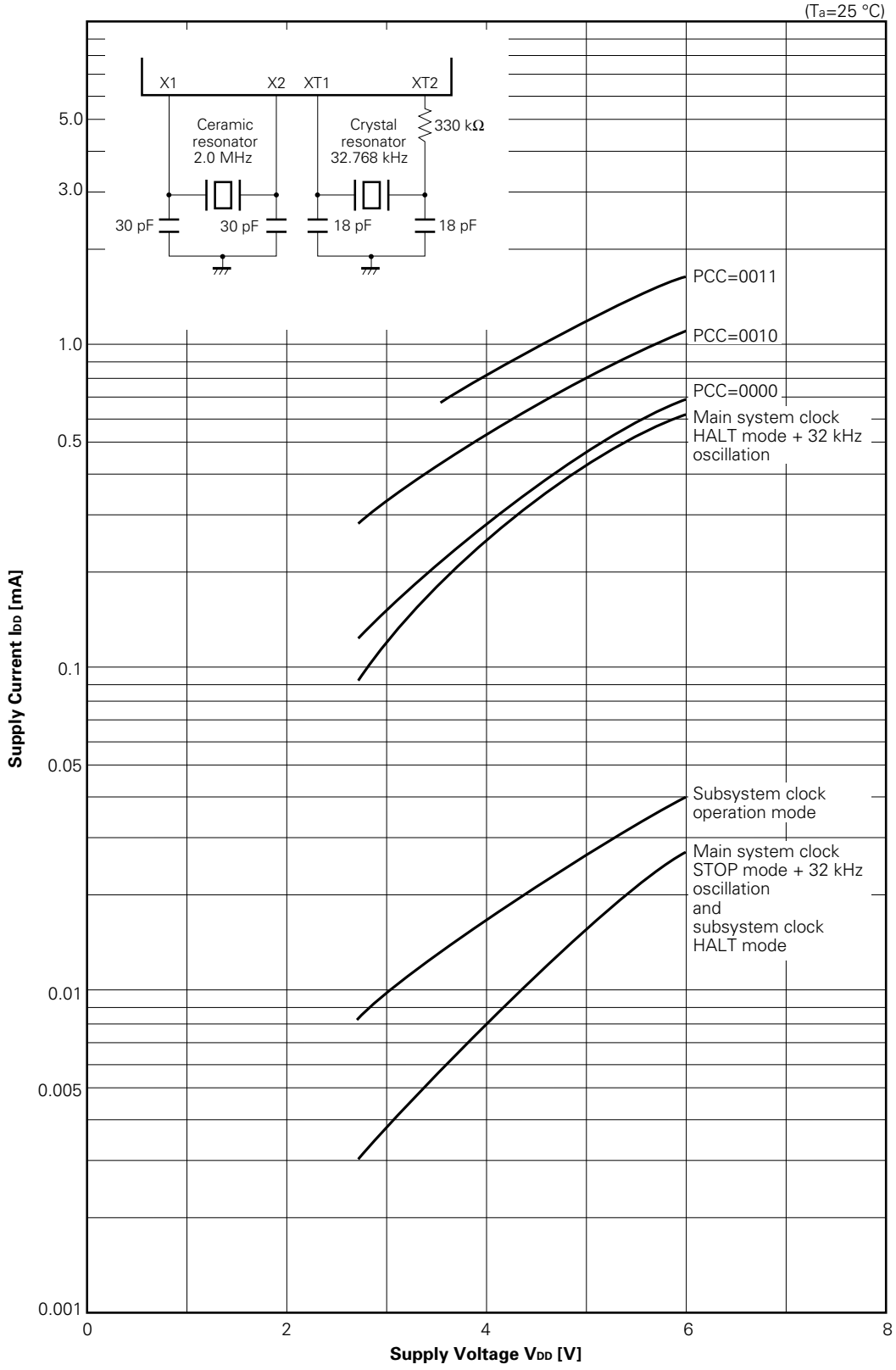
I_{DD} vs V_{DD} (Main system clock: 2.0-MHz crystal resonator)



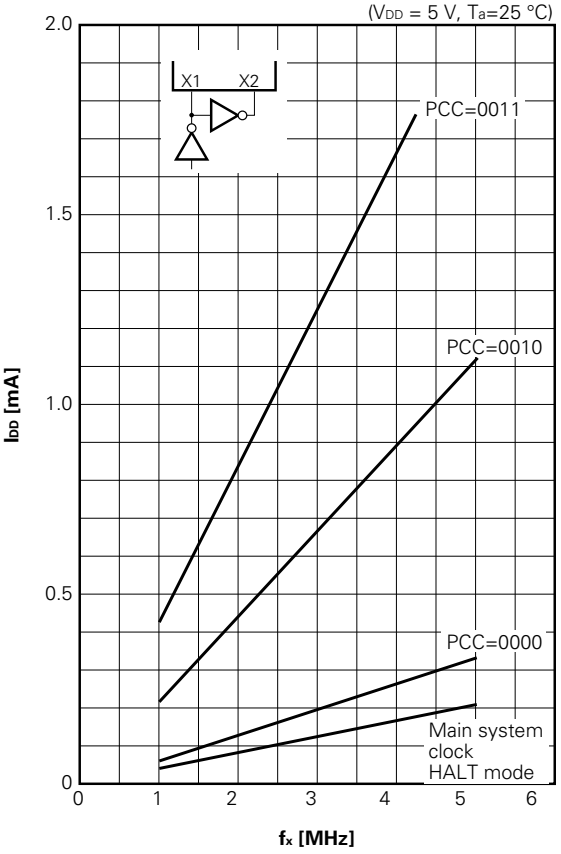
I_{DD} vs V_{DD} (Main system clock: 4.19-MHz ceramic resonator)



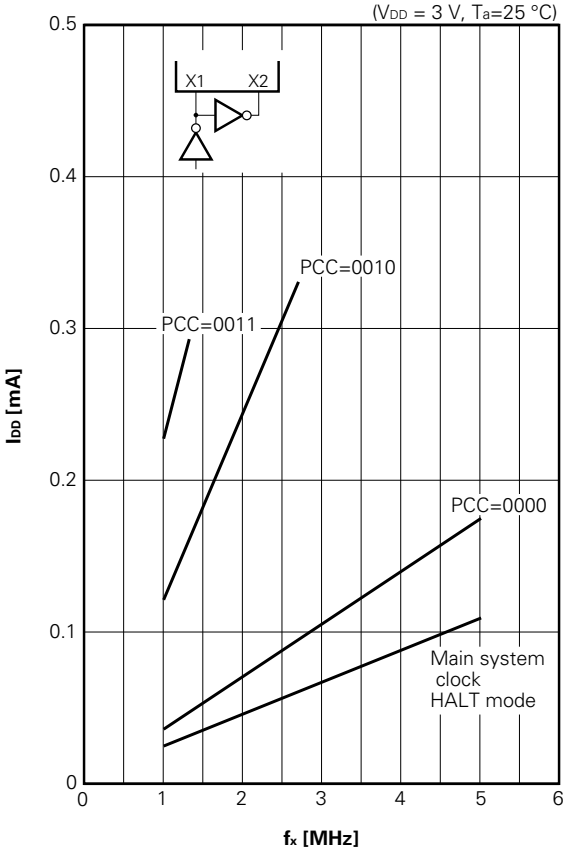
I_{DD} vs V_{DD} (Main system clock: 2.0-MHz ceramic resonator)



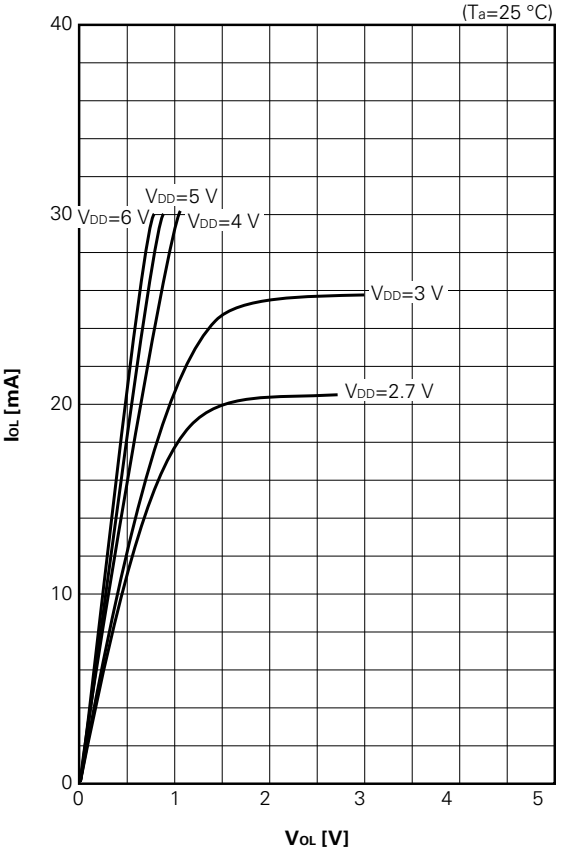
I_{DD} vs f_X



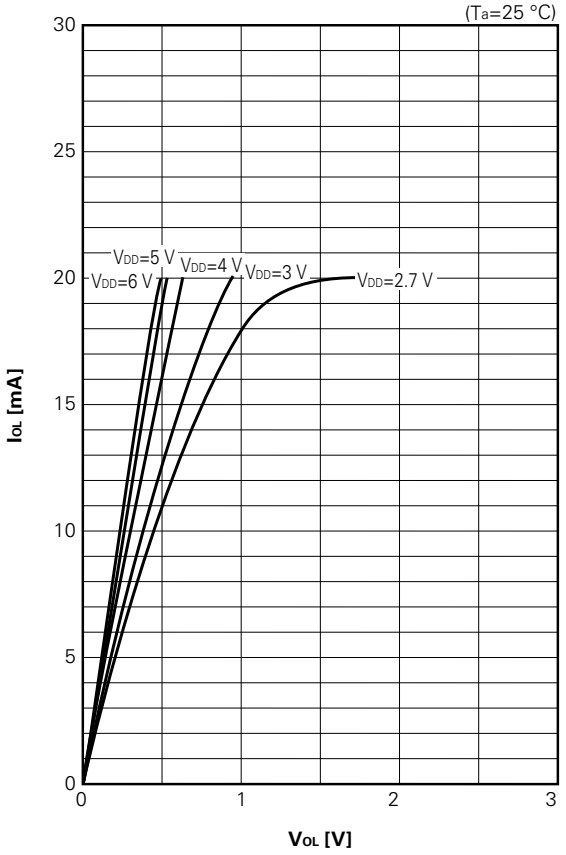
I_{DD} vs f_X



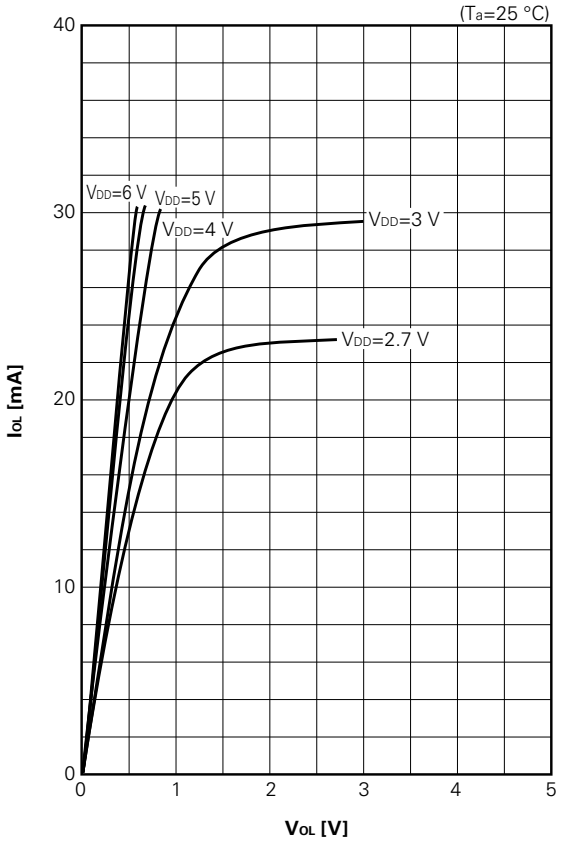
I_{OL} vs V_{OL} (Port 0)



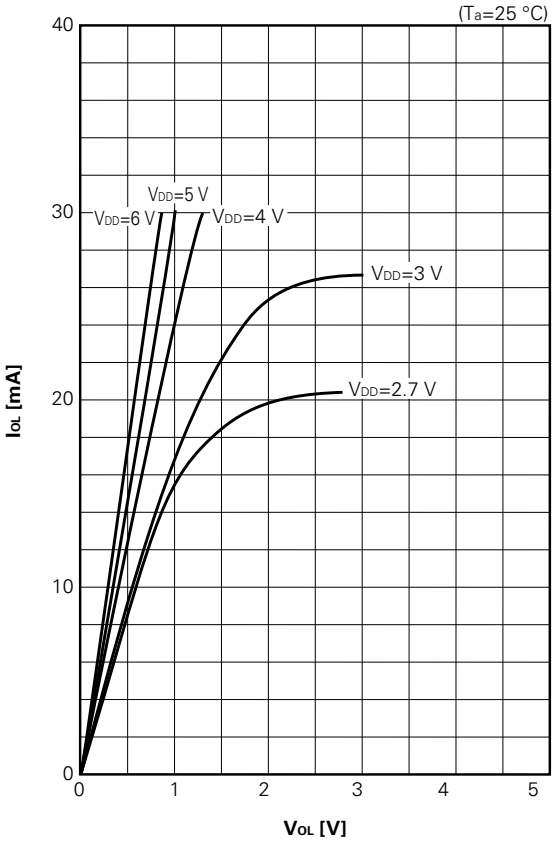
I_{OL} vs V_{OL} (Ports 2, 6)



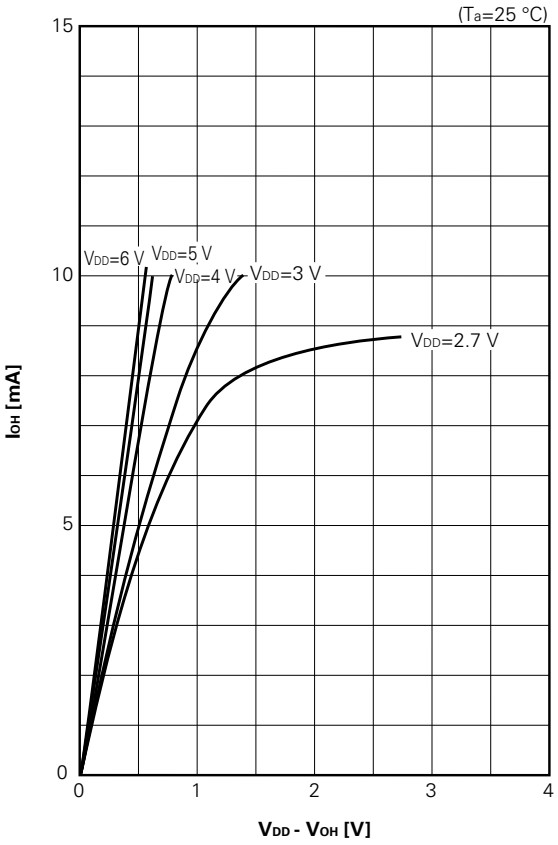
I_{OL} vs V_{OL} (Port 3)



I_{OL} vs V_{OL} (Ports 4, 5)

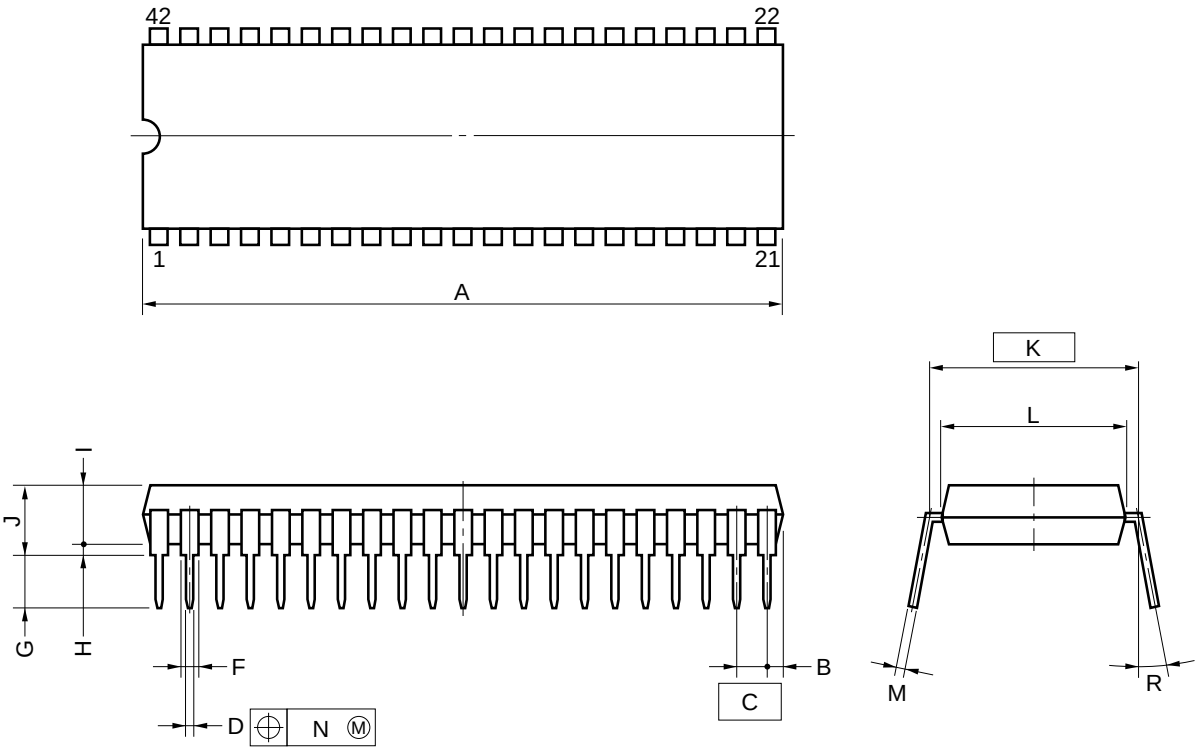


I_{OH} vs V_{OH}



12. PACKAGE DRAWINGS

42PIN PLASTIC SHRINK DIP (600 mil)



NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

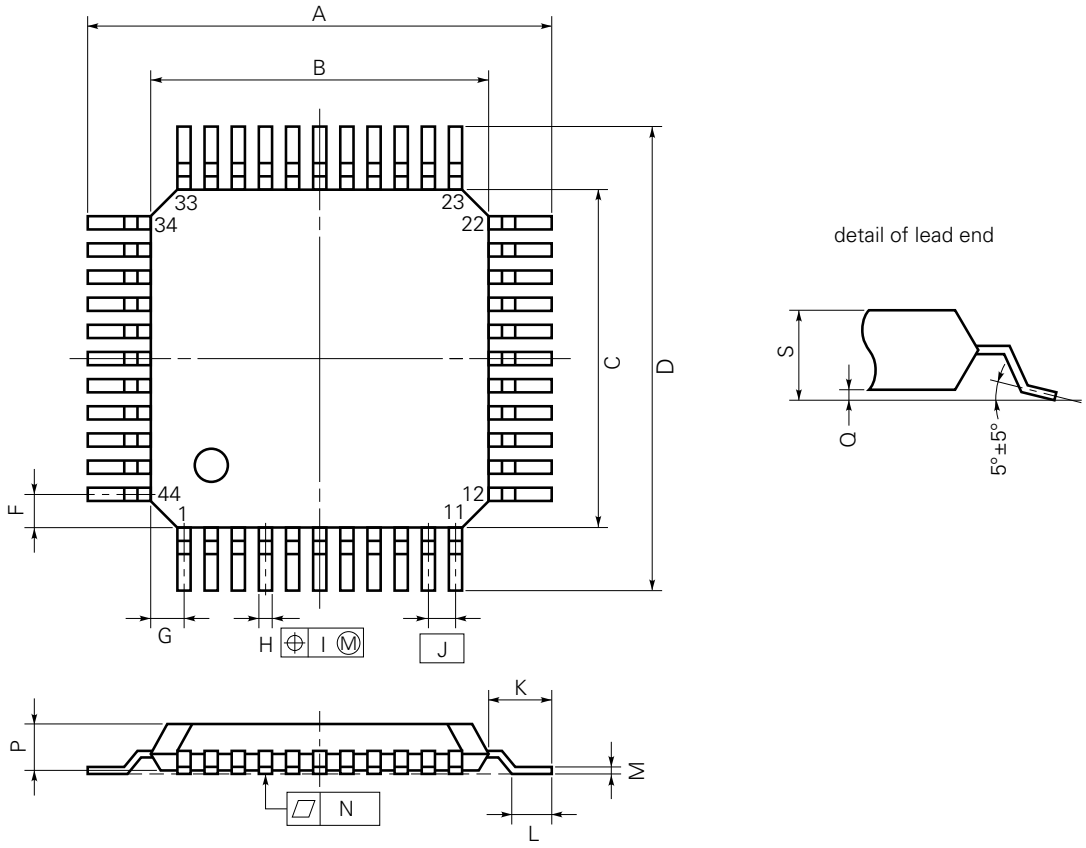
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	39.13 MAX.	1.541 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P42C-70-600A-1

★ **Remark** The outline dimensions and materials of ES versions are the same as for mass-produced versions.

44 PIN PLASTIC QFP (□10)



P44GB-80-3B4-2

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.6±0.4	$0.535^{+0.017}_{-0.016}$
B	10.0±0.2	$0.394^{+0.008}_{-0.009}$
C	10.0±0.2	$0.394^{+0.008}_{-0.009}$
D	13.6±0.4	$0.535^{+0.017}_{-0.016}$
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.12	0.005
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

Remark The outline dimensions and materials of ES versions are the same as for mass-produced versions. ★

★ 13. RECOMMENDED SOLDERING CONDITIONS

Solder the μPD75064, 75066, 75068 under the soldering conditions indicated below.

For further information on the recommended soldering conditions, refer to information document **"SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (IEI-1207)"**.

For soldering methods and conditions other than those of recommended, consult NEC.

Table 13-1. Soldering Conditions for Surface Mounting Devices

μPD75064GB-×××-3B4 : 44-pin plastic QFP (10 x 10 mm)
μPD75066GB-×××-3B4 : 44-pin plastic QFP (10 x 10 mm)
μPD75068GB-×××-3B4 : 44-pin plastic QFP (10 x 10 mm)
μPD75064GB(A)-×××-3B4 : 44-pin plastic QFP (10 x 10 mm)
μPD75066GB(A)-×××-3B4 : 44-pin plastic QFP (10 x 10 mm)
μPD75068GB(A)-×××-3B4 : 44-pin plastic QFP (10 x 10 mm)

Soldering method	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C, Time : 30 seconds max. (210 °C min.), Number of reflow processes : 2 or less <Note> (1) Start second reflow after the device temperature, which rose because of the first reflow, has dropped to the normal level. (2) Do not clean the flux with water after the first reflow.	IR35-00-2
VPS	Peak temperature of package surface : 215 °C, Time : 40 seconds max. (200 °C min.), Number of reflow processes : 2 or less <Note> (1) Start second reflow after the device temperature, which rose because of the first reflow, has dropped to the normal level. (2) Do not clean the flux with water after the first reflow.	VP15-00-2
Wave soldering	Solder temperature : 260 °C max., Time : 10 seconds max., Number of reflow processes : 1 Preheating temperature : 120 °C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature : 300 °C max., Time : 3 seconds max., (per one side of device)	—

Caution Do not apply two or more soldering methods (except partial heating method) to the same device.

Table 13-2. Soldering Conditions for Through-Hole Type Devices

μPD75064CU-×××: 42-pin plastic shrink DIP (600 mil)
μPD75066CU-×××: 42-pin plastic shrink DIP (600 mil)
μPD75068CU-×××: 42-pin plastic shrink DIP (600 mil)
μPD75064CU(A)-×××: 42-pin plastic shrink DIP (600 mil)
μPD75066CU(A)-×××: 42-pin plastic shrink DIP (600 mil)
μPD75068CU(A)-×××: 42-pin plastic shrink DIP (600 mil)

Soldering method	Soldering conditions
Wave soldering (Only leads)	Soldering bath temperature : 260 °C max., Time : 10 seconds max.
Partial heating	Pin temperature : 300 °C max., Time : 3 seconds max. (per pin)

Caution Solder only the leads by means of wave soldering , and exercise care that the jetted solder does not come in contact with the package.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are provided for the development of a system which employs the μPD75064, 75066, 75068, 75064(A), 75066(A), 75068(A).

Hardware	IE-75000-R [Note1] IE-75001-R	In-circuit emulator for 75X series
	IE-75000-R-EM [Note2]	Emulation board for IE-75000-R or IE-75001-R
	EP-75068CU-R	Emulation probe for all shrink DIP versions of this series
	EP-75068GB-R EV-9200G-44	Emulation probe for all QFP versions of this series. A 44-pin conversion socket EV-9200G-44 is contained in this product.
	PG-1500	PROM programming equipment
	PA-75P008CU	An adapter for connecting the PG-1500 to the μPD75P068CU/GB.
Software	IE control program	Host machines: PC-9800 series (MS-DOS™ Ver. 3.30 to Ver. 5.00A [Note3]) IBM PC/AT™ (refer to **OS for IBM PC**)
	PG-1500 controller	
	RA75X relocatable assembler	

Notes 1. Available for maintenance only
2. The IE-75000-R-EM is not installed in the IE-75001-R.
3. Ver. 5.00/5.00A has the task swap function, but it cannot be used with this software.

★ **OS for IBM PC**

The following products are supported as OS for IBM PCs.

OS	Version
PC DOS™	Ver. 5.02 to Ver. 6.1
MS-DOS	Ver. 3.30 to Ver. 5.00 [Note1], 5.0/V [Note2]
IBM DOS™	J5.02/V [Note2]

Notes 1. Ver. 5.0 and later have the task swap function, but it cannot be used with this software.
2. Only the English mode is supported.

Remark For development tools supplied by third-party manufacturers, refer to **75X Series Selection Guide (IF-1027)**.

APPENDIX B. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents related to device

Document	Doc. No.
User's Manual	IEU-1366
Instruction Quick Reference	—
Application Note	IEA-1296
75X Series Selection Guide	IF-1027

Documents related to development tool

Document			Doc. No.
Hardware	IE-75000-R/IE-75001-R User's Manual		EEU-1416
	IE-75000-R-EM User's Manual		EEU-1294
	EP-75068CU-R User's Manual		EEU-1429
	EP-75068GB-R User's Manual		EEU-1428
	PG-1500 User's Manual		EEU-1335
Software	RA75X Assembler Package User's Manual	Operation	EEU-1346
		Language	EEU-1363
	PG-1500 Controller User's Manual		EEU-1291

Other related documents

Document	Doc. No.
Package Manual	IEI-1231
Semiconductor Device Mounting Technology Manual	IEI-1207
Quality Grades on NEC Semiconductor Devices	IEI-1209
NEC Semiconductor Device Reliability/Quality Control System	—
Electrostatic Discharge (ESD) Test	—
Guide to Quality Assurance for Semiconductor Devices	MEI-1202
Microcomputer-Related Product Guide - Third Party Products	—

Caution The contents of the documents listed above are subject to change without prior notice to users. Make sure to use the latest edition when starting design.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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