NEC

MOS INTEGRATED CIRCUIT

μPD75312(A), 75316(A)

4-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD75316(A) is one of the 75X Series 4-bit single-chip microcomputer having a built-in LCD controller/driver, and has a data processing capability comparable to that of an 8-bit microcomputer.

In addition to high-speed operation with 0.95 μs minimum instruction execution time for the CPU, the μPD75316(A) can also process data in 1-, 4-, and 8-bit units. Therefore, as a 4-bit single-chip microcomputer chip having a built-in LCD panel controller/driver, its data processing capability is the highest in its class in the world.

Detailed functions are described in the following user's manual. Be sure to read it for designing.
μPD75308 User's Manual: IEM-5016

FEATURES

- Higher reliability than μPD75316
- Internal memory
  - Program memory (ROM)
    : 16256 × 8 bits (μPD75316(A))
    : 12160 × 8 bits (μPD75312(A))
  - Data memory
    : 512 × 4 bits
- Capable of high-speed operation and variable instruction execution time to power save
  - 0.95 μs, 1.91 μs, 15.3 μs (operating at 4.19 MHz)
  - 122 μs (operating at 32.768 kHz)
- 75X architecture comparable to that for an 8-bit microcomputer is employed
- Built-in programmable LCD controller/driver
- Clock operation at reduced power dissipation: 5 μA TYP. (operating at 3 V)
- Enhanced timer function (3 channels)
- Interrupt functions especially enhanced for applications, such as remote control receiver
- Pull-up resistors can be provided for 31 I/O lines
- Built-in NEC standard serial bus interface (SBI)
- Upgraded model of μPD7514 (μPD7500 Series)
- PROM version (μPD75P316, μPD75P316A) available

APPLICATIONS

Suitable for controlling automotive and transportation equipment.

The μPD75316(A) is treated as the representative model throughout this document, unless there are differences between μPD75312(A) and μPD75316(A) functions.

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(O. D. No. IC-8270A)
Date Published December 1993 P
Printed in Japan

The mark ★ shows major revised points.

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPD75312GF(A)-xxx-3B9	80-pin plastic QFP (14×20 mm)	Special
μPD75316GF(A)-xxx-3B9	80-pin plastic QFP (14×20 mm)	Special

Remarks: xxx is ROM code number.

Please refer to "Quality Grade on NEC Semiconductor Devices" (Document Number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

DIFFERENCE BETWEEN μPD75316(A) and μPD75316

Item \ Product		μPD75316(A)	μPD75316
Quality Grade		Special	Standard
Directly Driving LED		Not offered	Offered
Electrical Characteristics	Absolute Maximum Ratings	Differ in high-level output currrent and low-level output current	
	DC Characteristics	Differ in low-level output voltage	

FUNCTIONAL OUTLINE (1/2)

<table>
<tr><th colspan="2">Item</th><th colspan="4">Function</th></tr>
<tr><td colspan="2">Number of Basic Instructions</td><td colspan="4">41</td></tr>
<tr><td colspan="2">Instruction Cycle</td><td colspan="4">• 0.95 μs, 1.91 μs, 15.3 μs (Main system clock: operating at 4.19 MHz)
• 122 μs (Subsystem clock: operating at 32.768 kHz)</td></tr>
<tr><td rowspan="2">Internal Memory</td><td>ROM</td><td colspan="4">16256 × 8-bit (μPD75316(A)), 12160 × 8-bit (μPD75312(A))</td></tr>
<tr><td>RAM</td><td colspan="4">512 × 4 bits</td></tr>
<tr><td colspan="2">General-Purpose Registers</td><td colspan="4">• 4-bit manipulation: 8 (B, C, D, E, H, L, X, A)
• 8-bit manipulation: 4 (BC, DE, HL, XA)</td></tr>
<tr><td colspan="2">Accumulator</td><td colspan="4">• Bit accumulator (CY)
• 4-bit accumulator (A)
• 8-bit accumulator (XA)</td></tr>
<tr><td colspan="2">Instruction Set</td><td colspan="4">• Abundant bit manipulation instructions
• Efficient 4-bit data manipulation instructions
• 8-bit data transfer instructions
• GETI instruction executing 2-/3-byte instruction with a single byte</td></tr>
<tr><td colspan="2" rowspan="4">I/O Line</td><td rowspan="4">40</td><td>8</td><td>CMOS input pins</td><td rowspan="2">Pull-up by software is possible.
: 23</td></tr>
<tr><td>16</td><td>CMOS input/output pins</td></tr>
<tr><td>8</td><td>CMOS output pins</td><td>Also serve as segment pins</td></tr>
<tr><td>8</td><td>N-ch open-drain input/output</td><td>Withstand voltage: 10 V
Pull-up by mask option is possible.
: 8</td></tr>
<tr><td colspan="2">LCD Controller/ Driver</td><td colspan="4">• Segment number selection: 24/28/32 segments
(4/8 pins can also be used as bit ports.)
• Display mode selection: Static, 1/2 duty, 1/3 duty (1/2 bias), 1/3 duty (1/3 bias), 1/4 duty
• Dividing resistor for LCD driving can be built-in by mask option.</td></tr>
<tr><td colspan="2">Supply Voltage Range</td><td colspan="4">V_{DD} = 2.7 to 6.0 V</td></tr>
<tr><td colspan="2" rowspan="3">Timer</td><td rowspan="3">3 chs</td><td colspan="3">• 8-bit timer/event counter
• Clock source: 4 steps
• Event count is possible</td></tr>
<tr><td colspan="3">• 8-bit basic interval timer
• Reference time generation: 1.95 ms, 7.82 ms, 31.3 ms, 250 ms (operating at 4.19 MHz)
• Can be used as watchdog timer</td></tr>
<tr><td colspan="3">• Watch timer
• Generates 0.5-second time intervals
• Count clock source: Main system clock or subsystem clock (selectable)
• Watch fast forward mode (generates 3.9-ms time intervals)
• Buzzer output (2 kHz)</td></tr>
</table>

FUNCTIONAL OUTLINE (2/2)

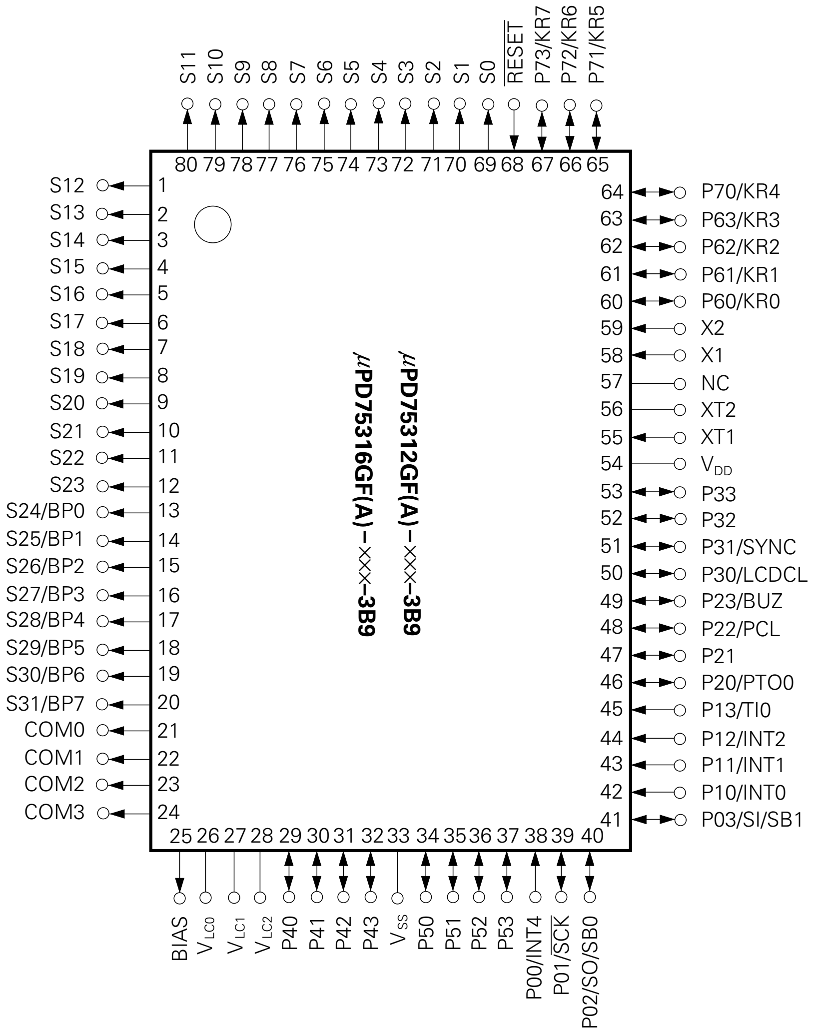
Item	Function

8-bit Serial Interface	• Three modes:
	  • 3-line serial I/O mode
	  • 2-line serial I/O mode
	  • SBI mode

	• LSB/MSB first selectable
Bit Sequential Buffer	Special bit manipulation memory: 16 bits • Ideal for remote controller
Clock Output Function	Timer/event counter output (PTO0): Output of square wave at specified frequency
	Clock output (PCL): Φ, 524, 262, 65.5 kHz (operating at 4.19 MHz)
	Buzzer output (BUZ): 2 kHz (operating at 4.19 MHz or 32.768 kHz)
Vector Interrupt	• External: 3 • Internal: 3
Test Input	• External: 1 • Internal: 1
System Clock Oscillator Circuit	• Ceramic/crystal oscillator circuit for main system clock oscillation: 4.194304 MHz • Crystal oscillator circuit for subsystem clock oscillation: 32.768 kHz
Standby	STOP/HALT mode
Package	80-pin plastic QFP (14 × 20 mm)

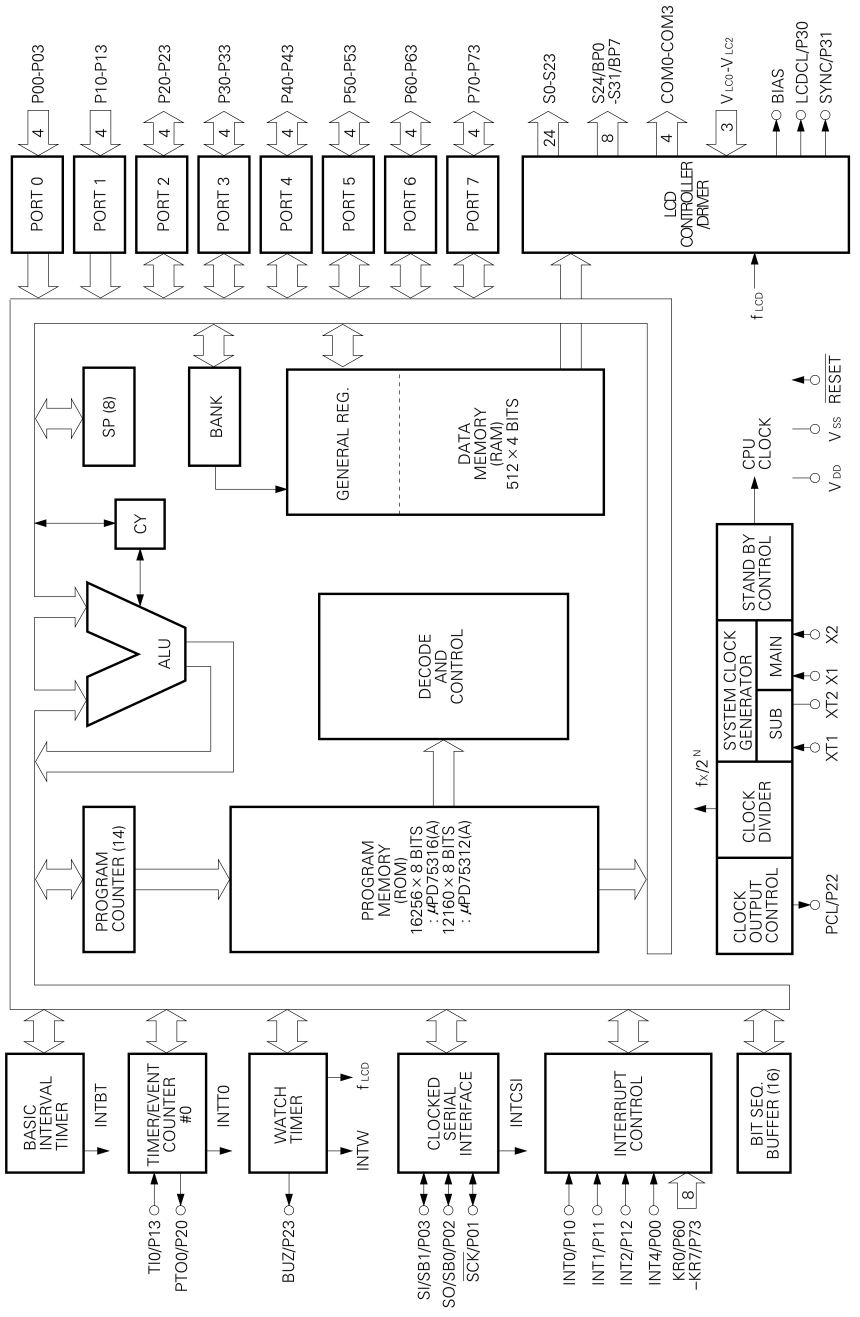
CONTENTS

1. PIN CONFIGURATION (Top View)



P00-P03	: Port 0	S0-S31	: Segment Output 0-31
P10-P13	: Port 1	COM0-COM3	: Common Output 0-3
P20-P23	: Port 2	V_{LC0}-V_{LC2}	: LCD Power Supply 0-2
P30-P33	: Port 3	BIAS	: LCD Power Supply Bias Control
P40-P43	: Port 4	LCDCL	: LCD Clock
P50-P53	: Port 5	SYNC	: LCD Synchronization
P60-P63	: Port 6	TI0	: Timer Input 0
P70-P73	: Port 7	PTO0	: Programmable Timer Output 0
BP0-BP7	: Bit Port	BUZ	: Buzzer Clock
KR0-KR7	: Key Return	PCL	: Programmable Clock
SCK	: Serial Clock	INT0, INT1, INT4	: External Vectored Interrupt 0, 1, 4
SI	: Serial Input	INT2	: External Test Input 2
SO	: Serial Output	X1, X2	: Main System Clock Oscillation 1, 2
SB0, SB1	: Serial Bus 0,1	XT1, XT2	: Subsystem Clock Oscillation 1, 2
RESET	: Reset Input	NC	: No Connection

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 PORT PINS (1/2)

Pin Name	Input/Output	Also Served As	Function	8-Bit I/O	When Reset	Input/ Output Circuit TYPE *
P00	Input	INT4	4-bit input port (PORT0) Pull-up resistors can be specified in 3-bit units for the P01 to P03 pins by software.	×	Input	Ⓑ
P01	Input/ Output	$\overline{SCK}$				Ⓕ-A
P02	Input/ Output	SO/SB0				Ⓕ-B
P03	Input/ Output	SI/SB1				Ⓜ-C
P10	Input	INT0	With noise elimination function 4-bit input port (PORT1) Internal pull-up resistors can be specified in 4-bit units by software.	×	Input	Ⓑ-C
P11		INT1				
P12		INT2				
P13		TI0				
P20	Input/ Output	PTO0	4-bit input/output port (PORT2) Internal pull-up resistors can be specified in 4-bit units by software.	×	Input	E-B
P21		—				
P22		PCL				
P23		BUZ				
P30	Input/ Output	LCDCL	Programmable 4-bit input/output port (PORT3) This port can be specified for input/ output in bit units. Internal pull-up resistors can be specified in 4-bit units by software.	×	Input	E-B
P31		SYNC				
P32		—				
P33		—				
P40-43	Input/ Output	—	N-ch open-drain 4-bit input/output port (PORT4) Internal pull-up resistors can be specified in bit units. (mask option) Withstand voltage is 10 V in the open-drain mode.	○	High level (with internal pull-up resistor) or high imped-ance	M
P50-53	Input/ Output	—	N-ch open-drain 4-bit input/output port (PORT5) Internal pull-up resistors can be specified in bit units. (mask option) Withstand voltage is 10 V in the open-drain mode.		High level (with internal pull-up resistor) or high imped-ance	M

*: Circles indicate Schmitt trigger inputs.

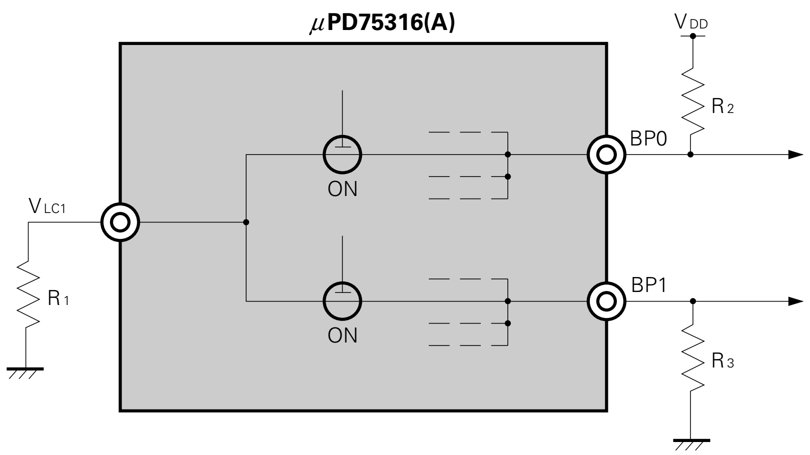
3.1 PORT PINS (2/2)

Pin Name	Input/Output	Also Served As	Function	8-Bit I/O	When Reset	Input/ Output Circuit TYPE*1
P60	Input/ Output	KR0	Programmable 4-bit input/output port (PORT6) This port can be specified for input/ output in bit units. Internal pull-up resistors can be specified in 4-bit units by software.	○	Input	(F)-A
P61		KR1				
P62		KR2				
P63		KR3				
P70	Input/ Output	KR4	4-bit input/output port (PORT7) Internal pull-up resistors can be specified in 4-bit units by software.		Input	(F)-A
P71		KR5				
P72		KR6				
P73		KR7				
BP0	Output	S24	1-bit output port (BIT PORT) Shared with a segment output pin.	×	*2	G-C
BP1		S25				
BP2		S26				
BP3		S27				
BP4	Output	S28				
BP5		S29				
BP6		S30				
BP7		S31				

*1: Circles indicate Schmitt trigger inputs.

2: For BP0-7, V_{LC1} indicated below are selected as the input source. However, the output level is changed depending on BP0-7 and the V_{LC1} external circuits.

Example: Since BP0-7 are connected to each other within the μPD75316(A) as shown in the diagram below, the output level of BP0-7 depends on the sizes of R_1, R_2 and R_3.



3.2 NON PORT PINS

Pin Name	Input/Output	Also Served As	Functon		When Reset	Input/ Output Circuit TYPE*1
TI0	Input	P13	Timer/event counter external event pulse Input		Input	Ⓑ-C
PTO0	Input/ Output	P20	Timer/event counter output		Input	E-B
PCL	Input/ Output	P22	Clock output		Input	E-B
BUZ	Input/ Output	P23	Fixed frequency output (for buzzer or for trimming the system clock)		Input	E-B
$\overline{SCK}$	Input/ Output	P01	Serial clock input/output		Input	Ⓕ-A
SO/SB0	Input/ Output	P02	Serial data output Serial bus input/output		Input	Ⓕ-B
SI/SB1	Input/ Output	P03	Serial data input Serial bus input/output		Input	Ⓜ-C
INT4	Input	P00	Edge detection vector interrupt input (both rising and falling edge detection are effective)		Input	Ⓑ
INT0	Input	P10	Edge detection vector interrupt input (detection edge can be selected)	Clock synchronous	Input	Ⓑ-C
INT1		P11		Asynchronous		
INT2	Input	P12	Edge detection testable input (rising edge detection)	Asynchronous	Input	Ⓑ-C
KR0-KR3	Input/ Output	P60-P63	Parallel falling edge detection testable input		Input	Ⓕ-A
KR4-KR7	Input/ Output	P70-P73	Parallel falling edge detection testable input		Input	Ⓕ-A
S0-S23	Output	—	Segment signal output		*2	G-A
S24-S31	Output	BP0-7	Segment signal output		*2	G-C
COM0-COM3	Output	—	Common signal output		*2	G-B
V_{LC0}-V_{LC2}	—	—	LCD drive power Internal dividing resistor (mask option)		—	—
BIAS	Output	—	Disconnect output for external expanded driver		*3	—
LCDCL*4	Input/ Output	P30	Externally expanded driver clock output		Input	E-B
SYNC*4	Input/ Output	P31	Externally expanded driver sync clock output		Input	E-B
X1, X2	Input	—	To connect the crystal/ceramic oscillator to the main system clock generator. When inputting the external clock, input the external clock to pin X1, and the reverse phase of the external clock to pin X2.		—	—
XT1	Input	—	To connect the crystal oscillator to the subsystem clock generator. When the external clock is used, pin XT1 inputs the external clock. In this case, pin XT2 must be left open. Pin XT1 can be used as a 1-bit input (test) pin.		—	—
XT2	—	—				

(to be cont'd)

(cont'd)

Pin Name	Input/Output	Also Served As	Function	When Reset	Input/ Output Circuit TYPE*1
$\overline{RESET}$	Input	—	System reset input	—	Ⓑ
NC *5	—	—	No connection	—	—
V_{DD}	—	—	Positive power supply	—	—
V_{SS}	—	—	GND	—	—

*1: Circles indicate Schmitt trigger inputs.

2: For these display output, V_{LCX} indicated below are selected as the input source.
S0 to S31: V_{LC1}, COM0 to COM2: V_{LC2}, COM3: V_{LC0}
However, display output level varies depending on the particular display output and V_{LCX} external circuit.

3: Internal dividing resistor provided : Low level
Internal dividing resistor not provided : High impedance

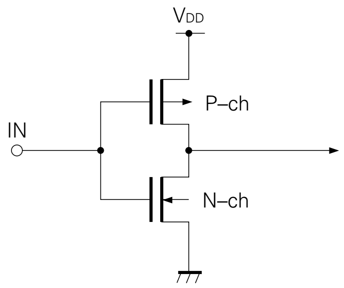
4: These pins are provided for future system expansion. At present, these pins are used only as pins P30 and P31.

5: When sharing the printed circuit board with the μPD75P316 and 75P316A, the NC pin must be connected to V_{DD}.

3.3 PIN INPUT/OUTPUT CIRCUITS

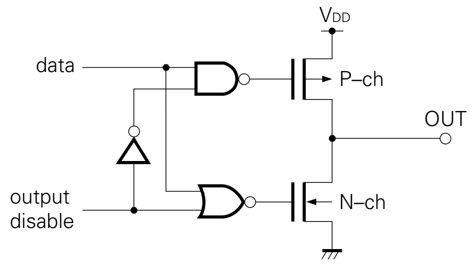
The following shows a simplified input/output circuit diagram for each pin of the μPD75316(A).

TYPE A (for TYPE E–B)



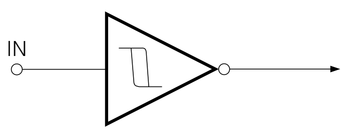
Input buffer of CMOS standard

TYPE D (for TYPE E–B, F–A)



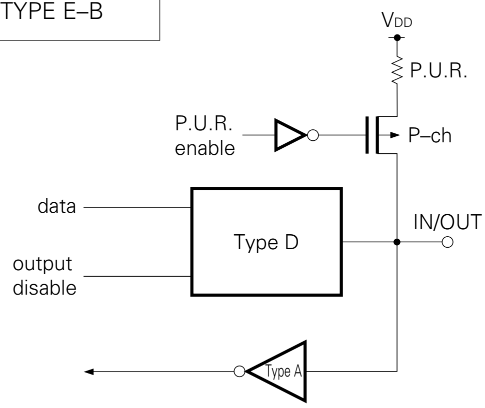
Push–pull output that can be set in a output high–impedance state (both P–ch and N–ch are off)

TYPE B



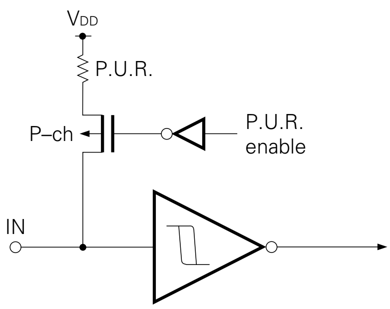
Schmitt trigger input with hysteresis characteristics

TYPE E–B



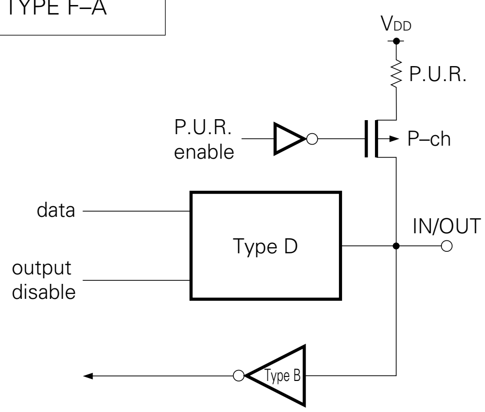
P.U.R. : Pull–Up Resistor

TYPE B–C



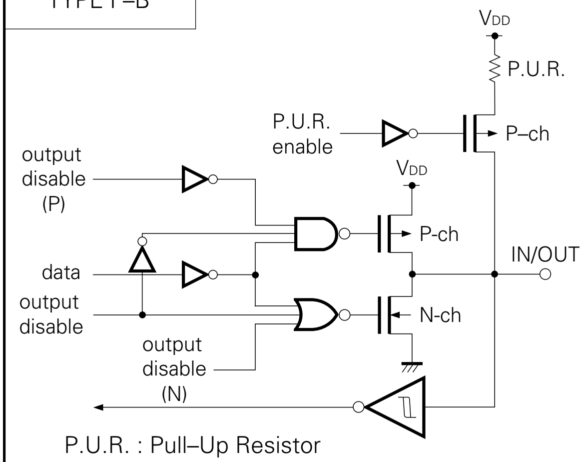
P.U.R. : Pull–Up Resistor

TYPE F–A



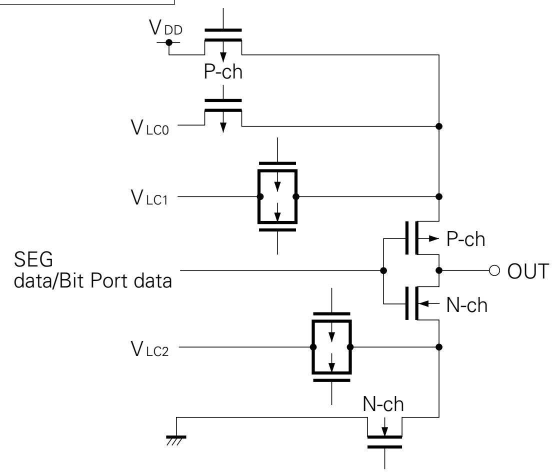
P.U.R. : Pull–Up Resistor

TYPE F–B

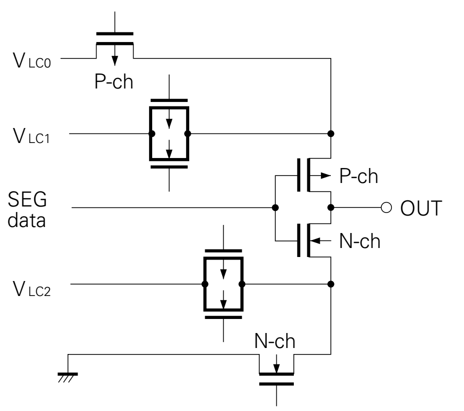


P.U.R. : Pull–Up Resistor

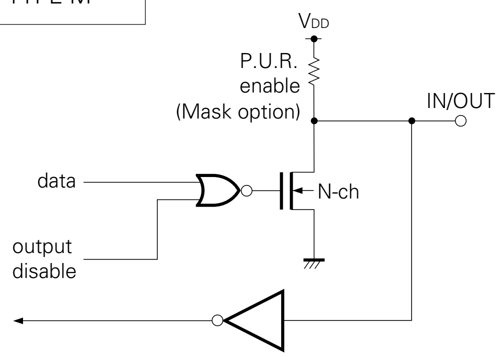
TYPE G–C



TYPE G–A



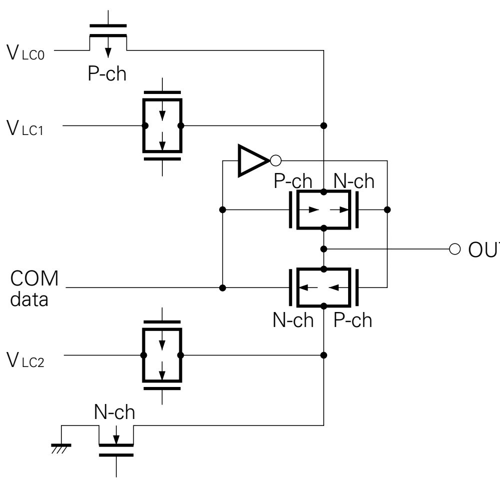
TYPE M



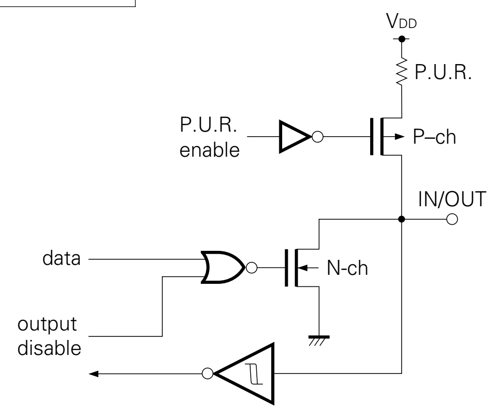
Middle voltage input buffer
(withstand voltage: +10 V)

P.U.R. : Pull–Up Resistor

TYPE G–B



TYPE M–C



P.U.R. : Pull–Up Resistor

3.4 RECOMMENDED PROCESSING OF UNUSED PINS

Table 3-1 Unused Pins Processing

Pin	Recommended Connections
P00/INT4	Connect to V_{SS}
P01/$\overline{SCK}$	Connect to V_{SS} or V_{DD}
P02/SO/SB0	
P03/SI/SB1	
P10/INT0-P12/INT2	Connect to V_{SS}
P13/TI0	
P20/PTO0	Input : Connect to V_{SS} or V_{DD} Output: Open
P21	
P22/PCL	
P23/BUZ	
P30/LCDCL	
P31/SYNC	
P32	
P33	
P40-P43	
P50-P53	
P60/KR0-P63/KR3	
P70/KR4-P73/KR7	
S0-S23	Open
S24/BP0-S31/BP7	
COM0-COM3	
V_{LC0}-V_{LC2}	Connect to V_{SS}
BIAS	Connect to V_{SS} only when all of the V_{LC0}-V_{LC2} pins are unused, otherwise, open.
XT1	Connect to V_{SS} or V_{DD}
XT2	Open

3.5 NOTES ON USING THE P00/INT4, AND $\overline{\text{RESET}}$ PINS

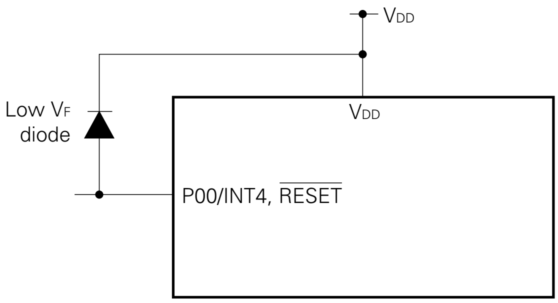
In addition to the functions described in Sections 3.1 and 3.2, an exclusive function for setting the test mode, in which the internal fuctions of the μPD75316(A) are tested, is provided to the P00/INT4 and $\overline{\text{RESET}}$ pins.

If a voltage exceeding V_{DD} is applied to either of these pins, the μPD75316(A) is put into test mode. Therefore, even when the μPD75316(A) is in normal operation, if noise exceeding the V_{DD} is input into any of these pins, the μPD75316(A) will enter the test mode, and this will cause problems for normal operation.

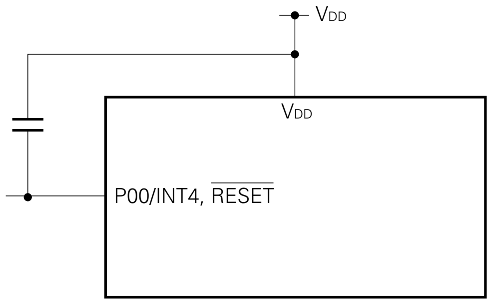
As an example, if the wiring to the P00/INT4 pin or the $\overline{\text{RESET}}$ pin is long, stray noise may be picked up and the above montioned problem may occur.

Therefore, all wiring to these pins must be made short enough to not pick up stray noise. If noise cannot be avoided, suppress the noise using a capacitor or diode as shown in the figure below.

- Connect a diode having a low V_F across P00/INT4 and $\overline{\text{RESET}}$, and V_{DD}.



- Connect a capacitor across P00/INT4 and $\overline{\text{RESET}}$, and V_{DD}.



4. MEMORY CONFIGURATION

- Program memory (ROM) ...16256 × 8 bits (0000H-3F7FH): μPD75316(A)
  ...12160 × 8 bits (0000H-2F7FH): μPD75312(A)
  - 0000H, 0001H : Vector table to which address from which program is started is written after reset
  - 0002H-000BH: Vector table to which address from which program is started is written after interrupt
  - 0020H-007FH: Table area referenced by GETI instruction

- Data memory
  - Data area .... 512 × 4 bits (000H–1FFH)
  - Peripheral hardware area .... 128 × 4 bits (F80H–FFFH)

(a) μPD75316(A)

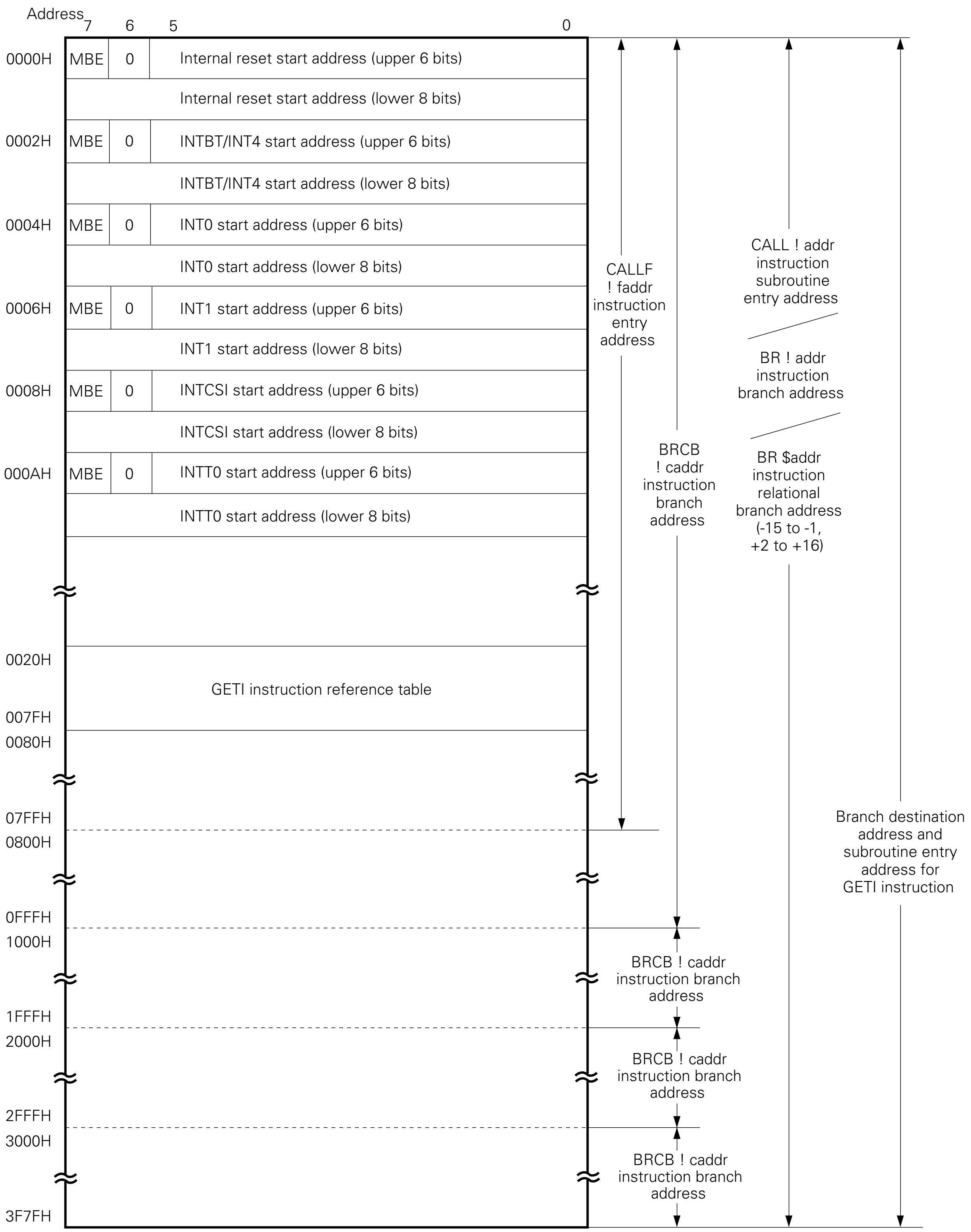


Fig. 4-1 Program Memory Map (1/2)

(b) μPD75312(A)

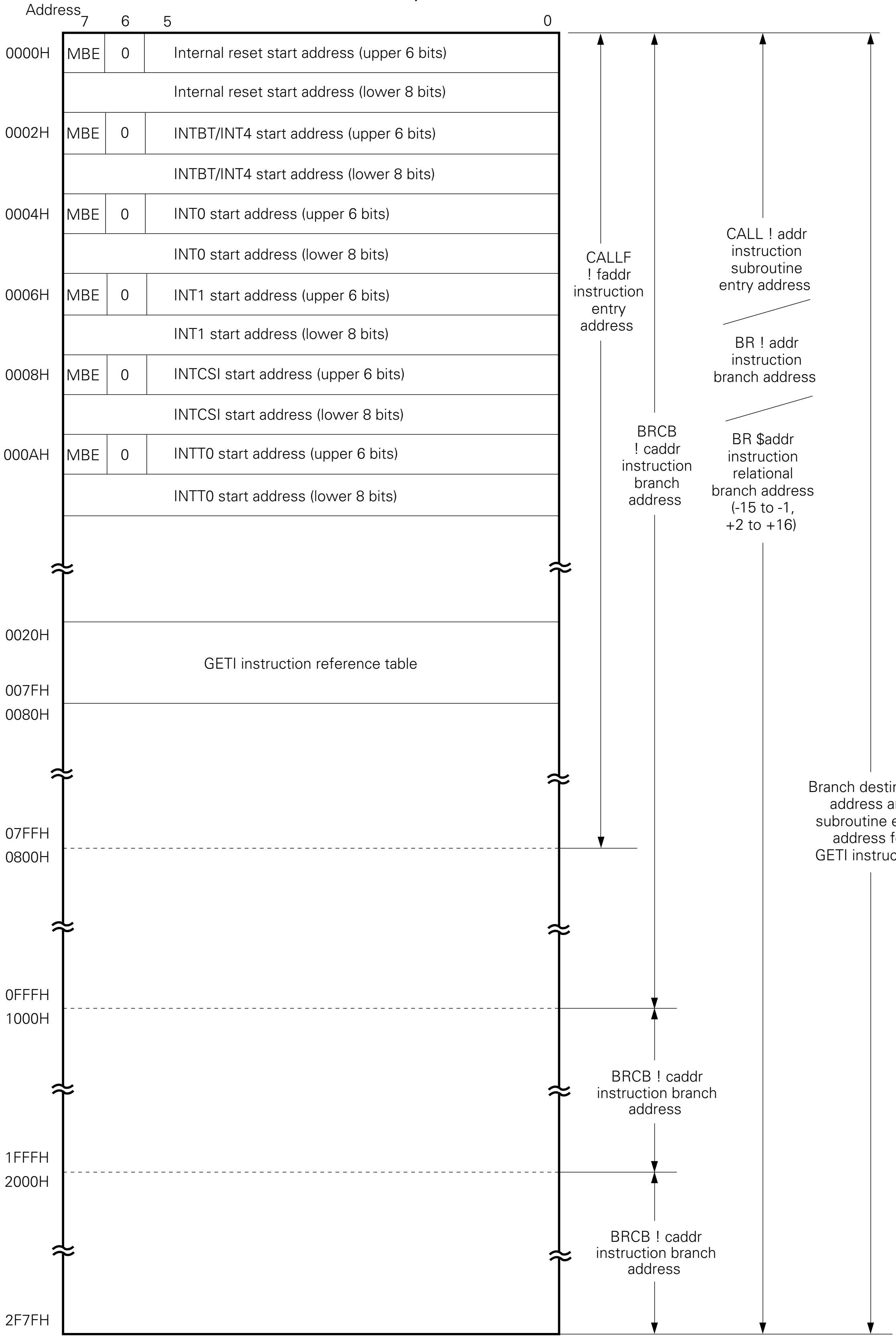


Fig. 4-1 Program Memory Map (2/2)

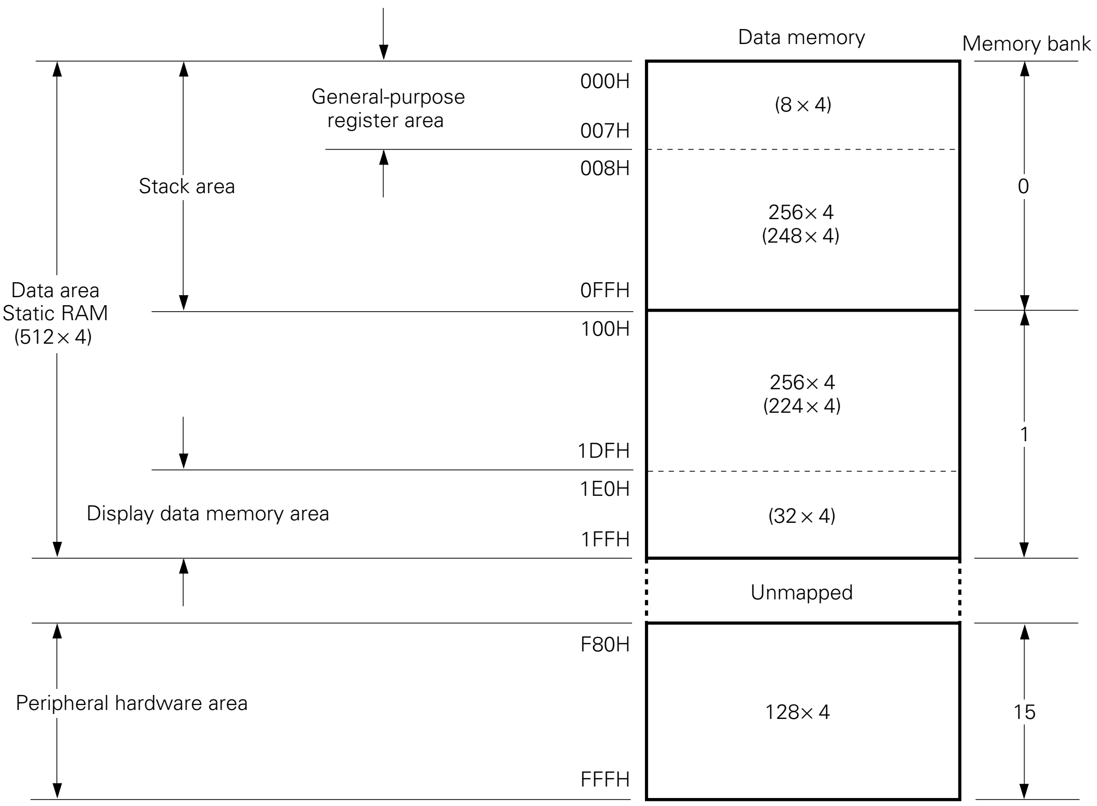


Fig. 4-2 Data Memory Map

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 PORTS

I/O ports are classified into the following 4 kinds:

• CMOS input (PORT0, 1)	: 8
• CMOS input/output (PORT2, 3, 6, 7)	: 16
• N-ch open-drain (PORT4, 5)	: 8
• CMOS output (BP0-BP7)	: 8
Total	: 40

<table>
<tr><th>Port Name</th><th>Function</th><th>Operation and Feature</th><th>Remarks</th></tr>
<tr><td>PORT0</td><td rowspan="2">4-bit input</td><td rowspan="2">Can be always read or tested regardless of operation mode of multiplexed pin.</td><td>Multiplexed with INT4, SCK, SO/SB0, and SI/SB1</td></tr>
<tr><td>PORT1</td><td>Multiplexed with INT0-INT2 and TI0</td></tr>
<tr><td>PORT2</td><td rowspan="4">4-bit Input/Output</td><td rowspan="2">Can be set in input or output mode in 4-bit units. Ports 6 and 7 are used in pairs to input/output data in 8-bit units.</td><td>Multiplexed with PTO0, PCL, and BUZ</td></tr>
<tr><td>PORT7</td><td>Multiplexed with KR4-KR7</td></tr>
<tr><td>PORT3</td><td rowspan="2">Can be set in input or output mode in 1-bit units.</td><td>Multiplexed with LCDCL and SYNC</td></tr>
<tr><td>PORT6</td><td>Multiplexed with KR0-KR3</td></tr>
<tr><td>PORT4
PORT5</td><td>4-bit Input/Output (N-ch open-drain, 10 V)</td><td>Can be set in input or output mode in 4-bit units. Ports 4 and 5 are used in pairs to input/output data in 8-bit units.</td><td>Can be connected to a pull-up resistor in 1-bit units by using mask option.</td></tr>
<tr><td>BP0-BP7</td><td>1-bit output</td><td>Output data in 1-bit units. Can be used as LCD drive segment output pins S24-S31 through software.</td><td>Low drive capability
For driving CMOS load</td></tr>
</table>

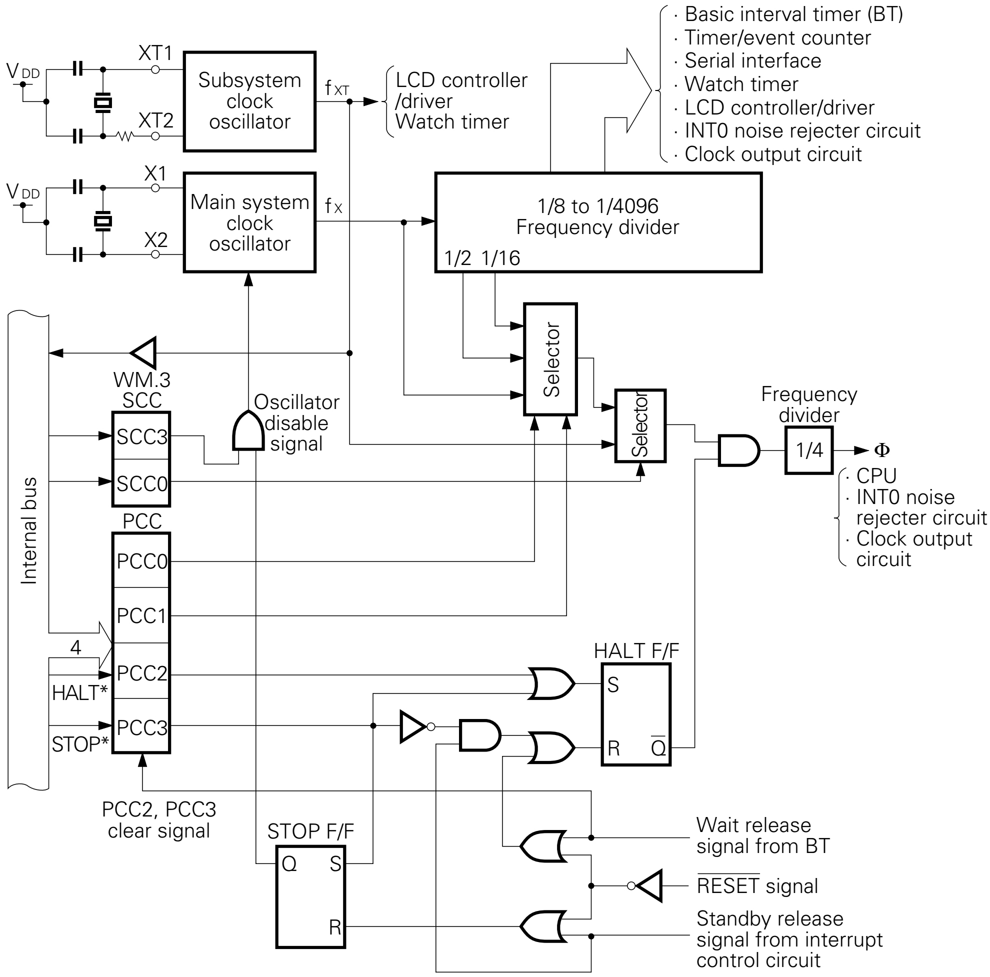
5.2 CLOCK GENERATOR CIRCUIT

The operation of the clock generator circuit is determined by the processor clock control regiser (PPC) and system clock control register (SCC).

This circuit can generate two types of clocks: main system clock and subsystem clock.

In addition, it can also change the instruction execution time.

- 0.95 μs/1.91 μs/15.3 μs (main system clock: 4.19 MHz)
- 122 μs (subsystem clock: 32.768 kHz)



Remarks 1: f_X = Main system clock frequency

2: f_{XT} = Subsystem clock frequency

3: PCC: Processor clock control register

4: SCC: System clock control register

5: *: instruction execution.

6: One clock cysle (t_{CY}) of Φ is one machine cycle of an instruction. For t_{CY}, refer to AC characteristics in 11. ELECTRICAL SPECIFICATIONS. ★

Fig. 5-1 Clock Generator Block Diagram

5.3 CLOCK OUTPUT CIRCUIT

The clock output circuit outputs clock pulse from the P22/PCL pin. This clock pulse is used for the remote control output, peripheral LSIs, etc.

- Clock output (PCL) : Φ, 524, 262, 65.5 kHz (operating at 4.19 MHz)
- Buzzer output (BUZ) : 2 kHz (operating at 4.19 MHz or 32.768 kHz)

Fig. 5-2 shows the clock output circuit configuration.

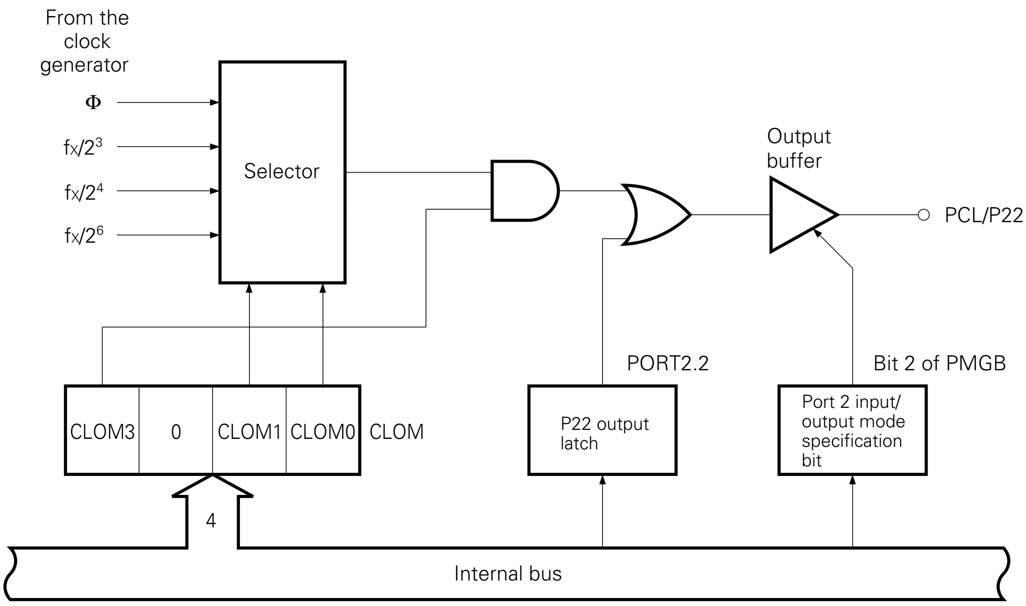


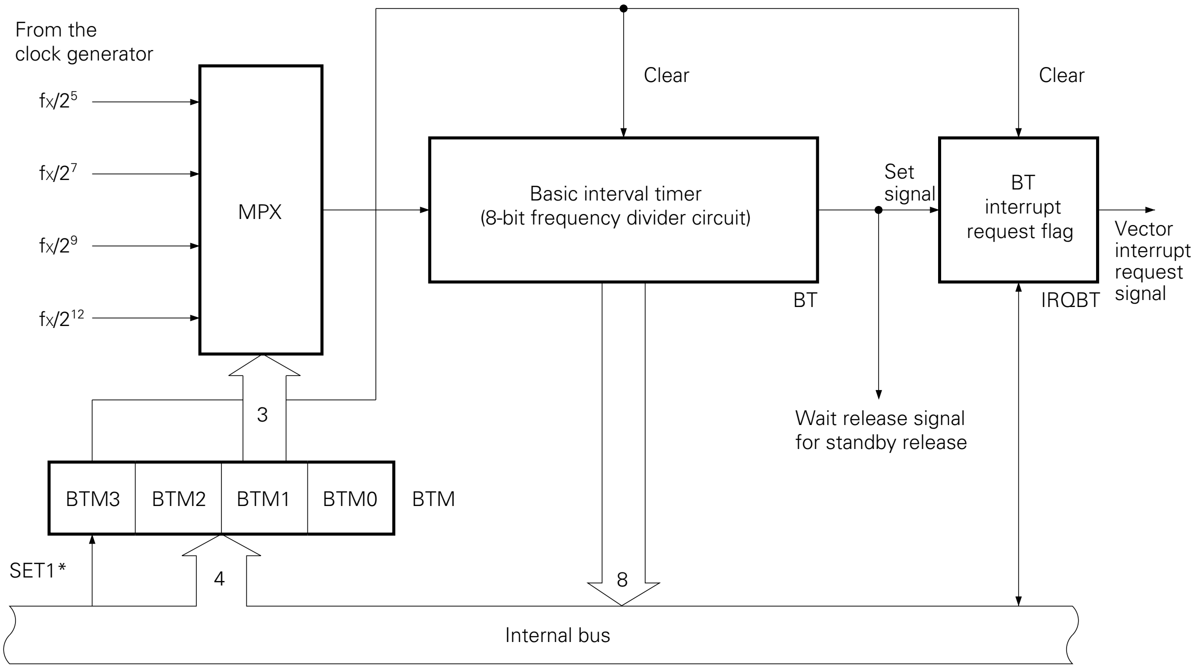
Fig. 5-2 Clock Output Circuit Configuration

Remarks: A measures to prevent outputting narrow width pulse when selecting clock output enable/ disable is taken.

5.4 BASIC INTERVAL TIMER

The basic interval timer has these functions:

- Interval timer operation which generates a reference time interrupt
- Watchdog timer application which detects a program runaway
- Selects the wait time for releasing the standby mode and counts the wait time
- Reads out the count value



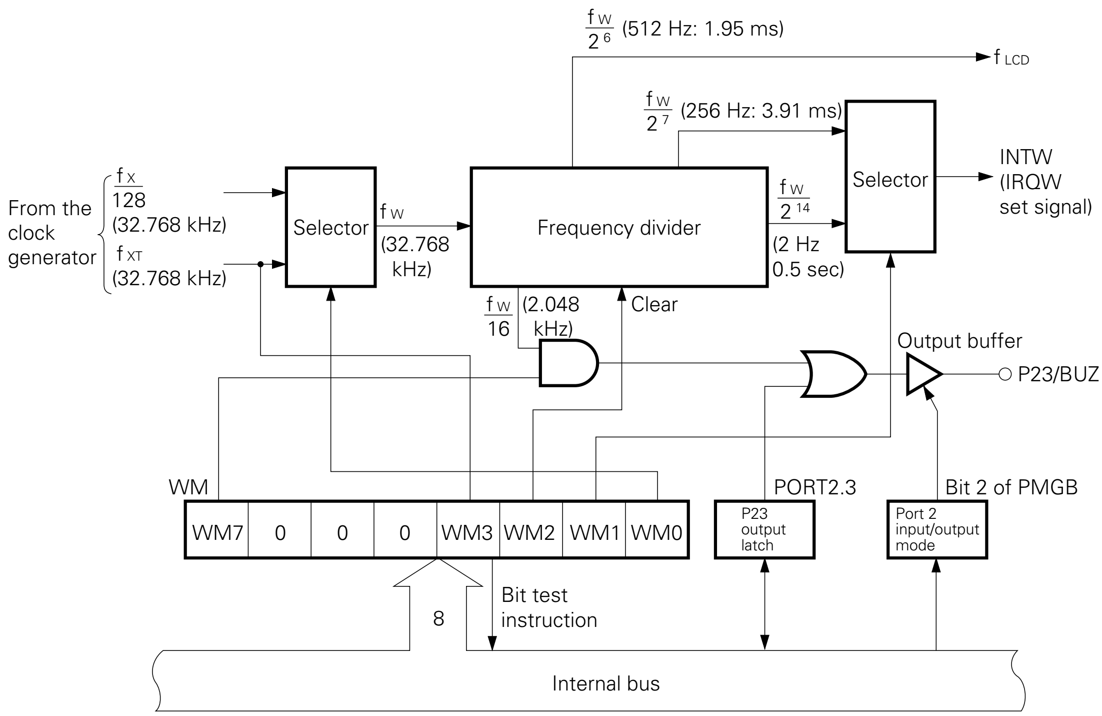
Remarks : *: Instruction execution

Fig. 5-3 Basic Interval Timer Configuration

5.5 WATCH TIMER

The μPD75316(A) has a built-in 1-ch watch timer. The watch timer is configured as shown in Fig. 5-4.

- Sets the test flag (IRQW) with 0.5 sec interval.
  The standby mode can be released by IRQW.
- 0.5 second interval can be generated either from the main system clock or subsystem clock.
- Time interval can be advanced to 128 times faster (3.91 ms) by setting the fast mode. This is convenient for program debugging, test, etc.
- Fixed frequency (2.048 kHz) can be output to the P23/BUZ pin. This can be used for beep and system clock frequency trimming.
- The frequency divider circuit can be cleared so that zero second watch start is possible.



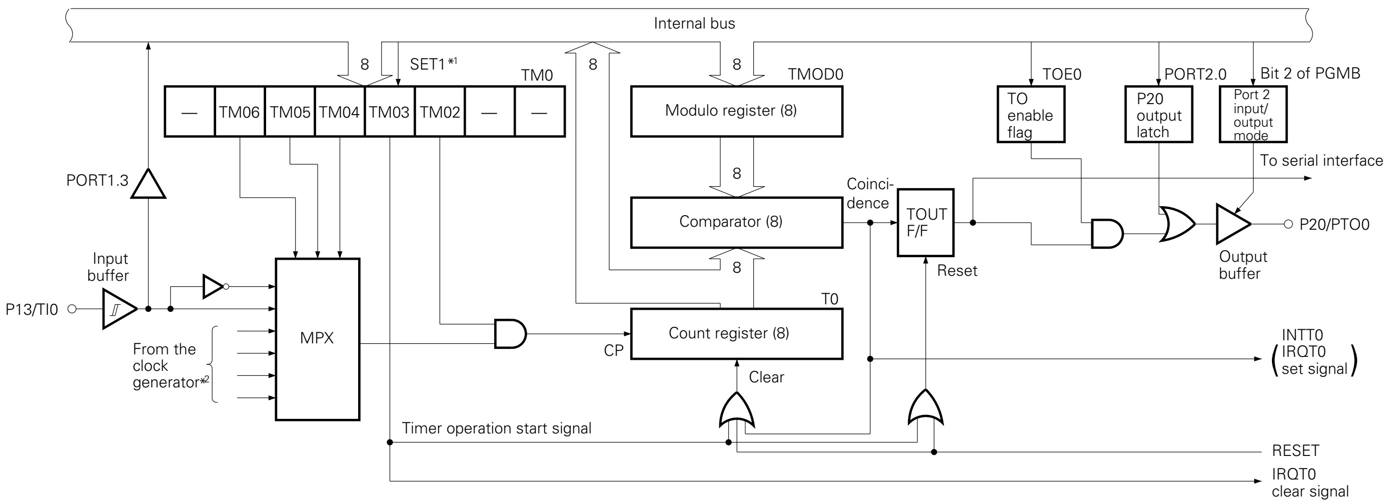
( ) is for fX = 4.194304 MHz, fXT = 32.768 kHz.

Fig. 5-4 Watch Timer Block Diagram

5.6 TIMER/EVENT COUNTER

The μPD75316(A) has a built-in 1-ch timer/event counter. The timer/even counter has these functions:

- Programmable interval timer operation
- Outputs square-wave signal of an arbitrary frequency to the PTO0 pin.
- Event counter operation
- Divides the TI0 pin input in N and outputs to the PTO0 pin (frequency divider operation).
- Supplies serial shift clock to the serial interface circuit.
- Count condition read out function



*1: SET1: Instruction execution
2: For details, refer to Fig. 5-1.

Fig. 5-5 Timer/Event Counter Block Diagram

5.7 SERIAL INTERFACE

The μPD75316(A) is equipped with an 8-bit clocked serial interface that operates in the following three modes:

- Three-line serial I/O mode
- Two-line serial I/O mode
- SBI mode (serial bus interface mode)

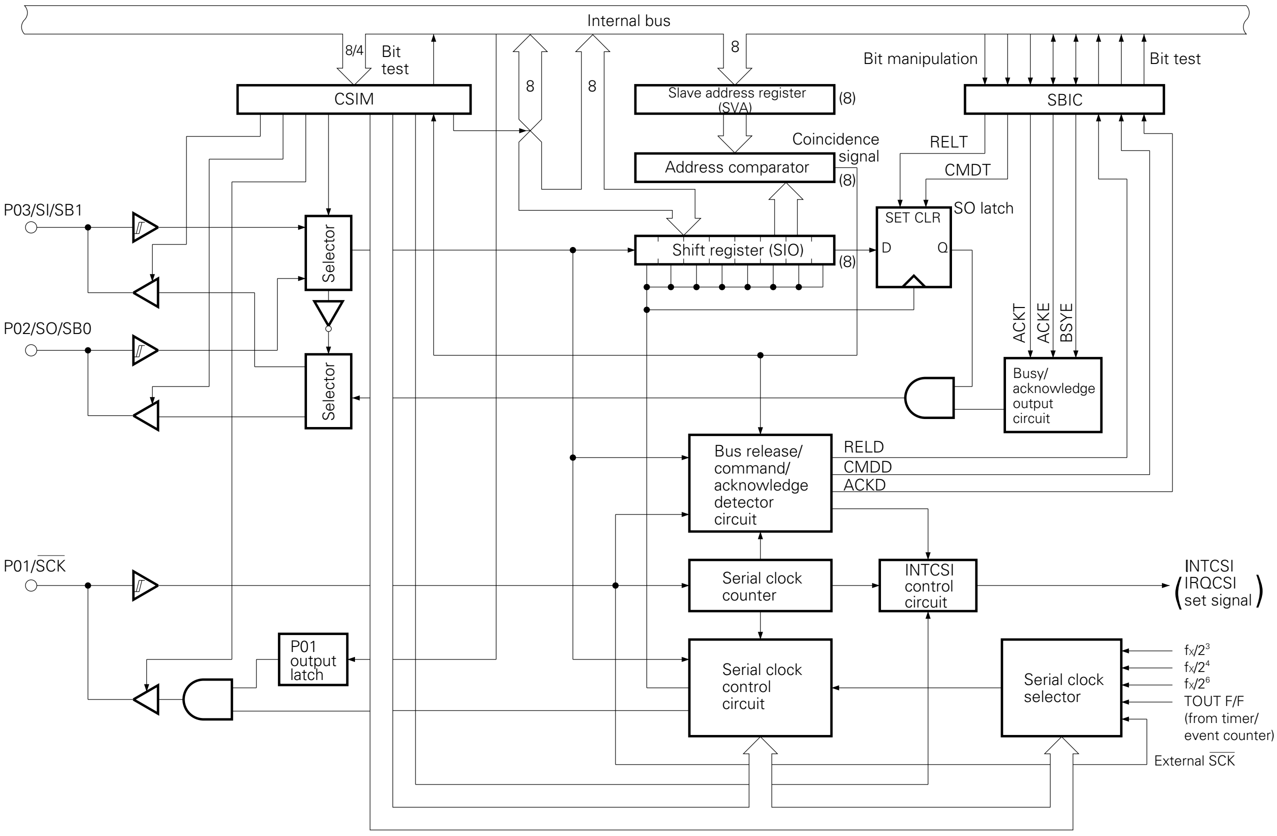


Fig. 5-6 Serial Interface Block Diagram

5.8 LCD CONTROLLER/DRIVER

The μPD75316(A) is provided with a display controller that generates segment and common signals and a segment driver and a common driver that can directly drive an LCD panel.

Figure 5-7 shows the LCD controller/driver configuration.

These LCD controller and drivers have the following functions:

- Generate segment and common signals by automatically reading the display data memory by means of DMA
- Five display modes selectable
  ① Static
  ② 1/2 duty (1/2 bias)
  ③ 1/3 duty (1/2 bias)
  ④ 1/3 duty (1/3 bias)
  ⑤ 1/4 duty (1/3 bias)
- Four types of frame frequencies selectable in each display mode
- Up to 32 segment signals (S0-S31) and four common signals (COM0-COM3) can be output.
- Four segment signal output pins (S24-S27, S28-S31) can be used as an output port (BP0-BP3, BP4-BP7).
- Dividing resistor for LCD driving power source can be provided (by mask option).
  - All bias modes and LCD drive voltages can be used.
  - Current flowing to dividing resistor can be cut when display is off.
- Display data memory not used for display can be used as ordinary data memory.
- Can also operate on subsystem clock.

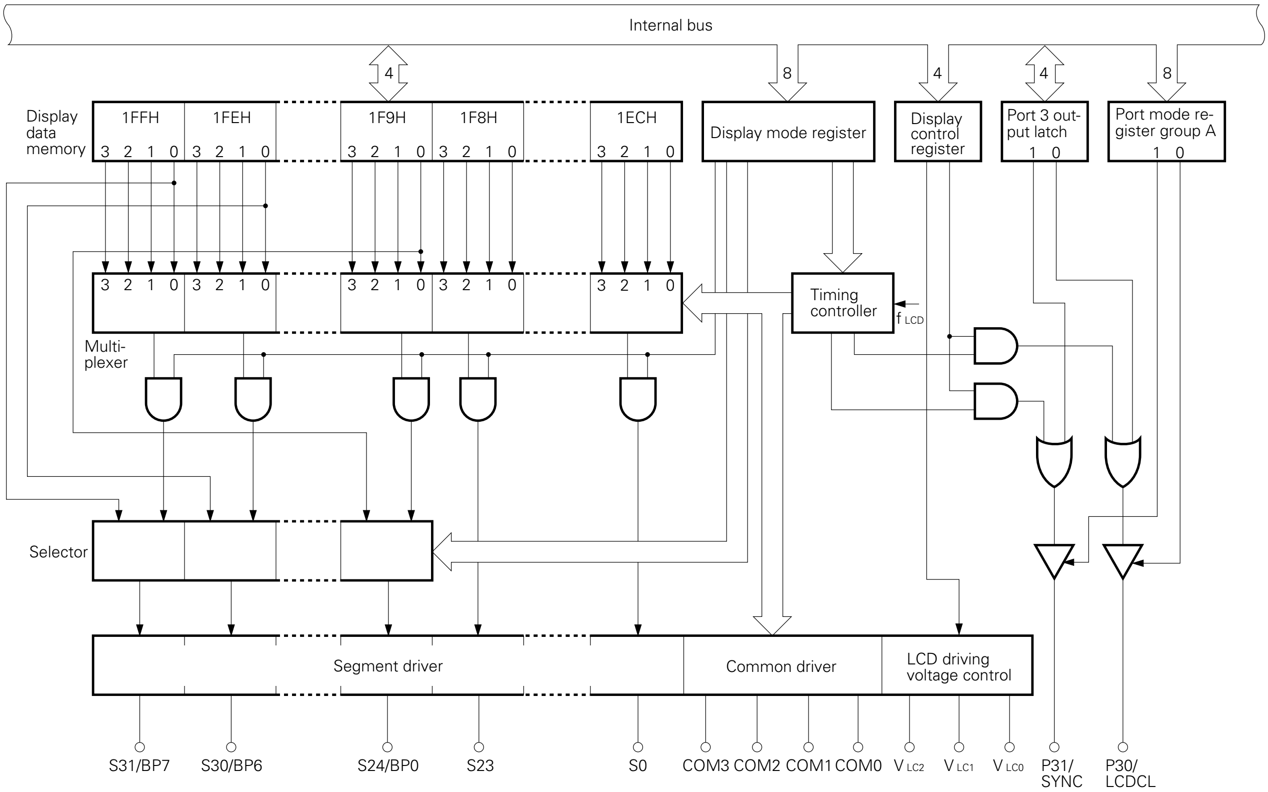
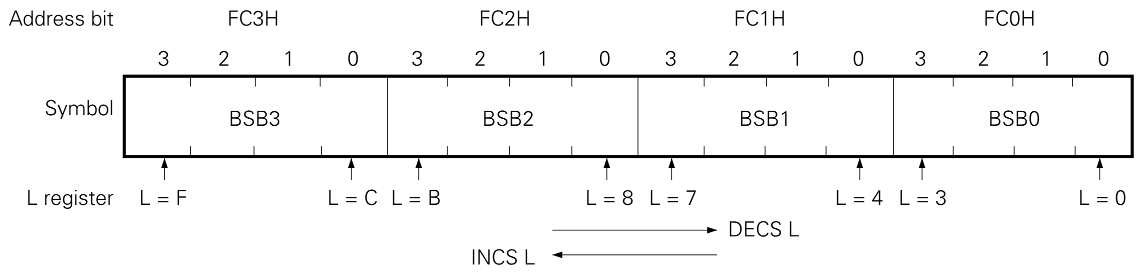


Fig. 5-7 LCD Controller/Driver Block Diagram

5.9 BIT SEQUENTIAL BUFFER .... 16 BITS

The bit sequential buffer is a data memory specifically provided for bit manipulation. With this buffer, addresses and bit specifications can be sequentially up-dated in bit manipulation operation. Therefore, this buffer is very useful for processing long data in bit units.



Remarks: For the pmem.@L addressing, the specification bit is shifted according to the L register.

Fig. 5-8 Bit Sequential Buffer Format

6. INTERRUPT FUNCTIONS

The μPD75316(A) has 6 different interrupt sources and multiple interrupt by software control is also possible. The μPD75316(A) is also provided with two types of test sources, of which INT2 has two types of edge detection testable inputs.

The interrupt control circuit of the μPD75316(A) has these functions:

- Hardware controlled vector interrupt function which can control whether or not to accept an interrupt by using the interrupt flag (IExxx) and interrupt master enable flag (IME).
- The interrupt start address can be arbitrarily set.
- Interrupt request flag (IRQxxx) test function (an interrupt generation can be confirmed by means of software).
- Standby mode release (Interrupts to be released can be selected by the interrupt enable flag).

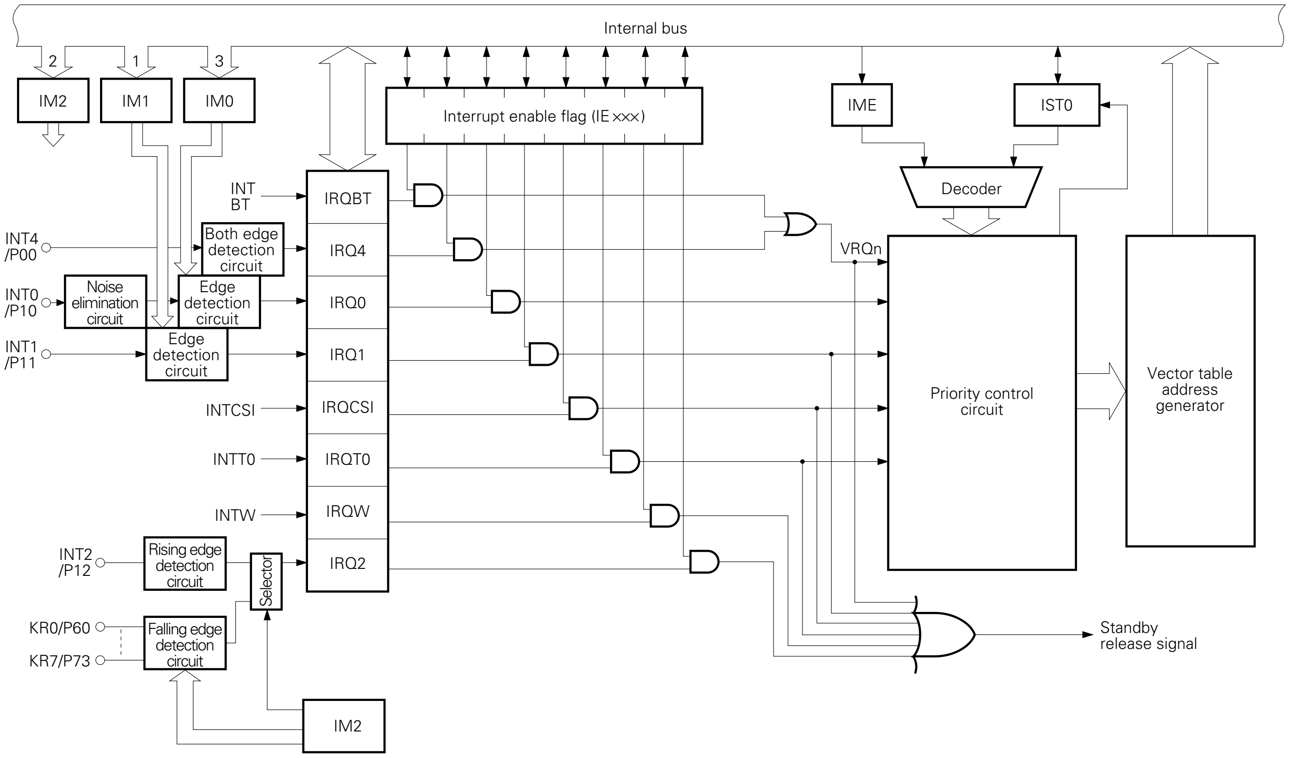


Fig. 6-1 Interrupt Control Block Diagram

7. STANDBY FUNCTIONS

The μPD75316(A) has two different standby modes (STOP mode and HALT mode) to reduce the power consumption while waiting for program execution.

Table 7-1 Each Status in Standby Mode

		STOP Mode	HALT Mode
Setting Instruction		STOP instrtuction	HALT instruction
System Clock for Setting		Can be set only when operating on the main system clock	Can be set either with the main system clock or the subsystem clock
Operation Status	Clock Generator	Only the main system clock stops its operation.	Only the CPU clock Φ stops its operation. (oscillation continues)
	Basic Interval Timer	No operation	Operation (Sets IRQBT at reference time interval) *
	Serial Interface	Can operate only when the external $\overline{SCK}$ input is selected for the serial clock	Can operate *
	Timer/Event Counter	Can operate only when the TI0 pin input is selected for the count clock	Can operate *
	Watch Timer	Can operate when f_{XT} is selected for the count clock	Can operate
	LCD Controller	Can operate only when f_{XT} is selected for LCDCL	Can operate
	External Interrupt	INT1, INT2, and INT4 can operate. Only INT0 cannot operate.	
	CPU	No operation	
Release Signal		An interrupt request signal from a hardware whose operation is enabled by the interrupt enable flag or the $\overline{RESET}$ signal input	An interrupt request signal from a hardware whose operation is enabled by the interrupt enable flag or the $\overline{RESET}$ signal input

*: Operation is possible only when the main system clock is operating.

8. RESET FUNCTION

When the RESET signal is input, the μPD75316(A) is reset and each hardware is initialized as indicated in Table 8-1. Fig. 8-1 shows the reset operation timing.

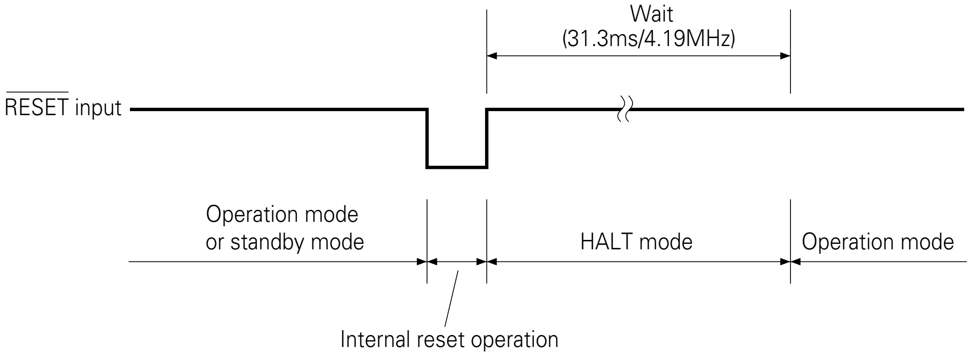


Fig. 8-1 Reset Operation by RESET Input

Table 8-1 Status of Each Hardware after Reset (1/2)

Hardware		RESET Input in Standby Mode	RESET Input during Operation
Program Counter (PC)		The contents of the lower 6 bits of address 0000H of the program memory are set to PC13-8, and the contents of address 0001H are set to PC7-0.	The contents of the lower 6 bits of address 0000H of the program memory are set to PC13-8, and the contents of address 0001H are set to PC7-0.
PSW	Carry Flag (CY)	Retained	Undefined
	Skip Flag (SK0-2)	0	0
	Interrupt Status Flag (IST0)	0	0
	Bank Enable Flag (MBE)	The contents of bit 7 of address 0000H of the program memory are set to MBE.	The contents of bit 7 of address 0000H of the program memory are set to MBE.
Stack Pointer (SP)		Undefined	Undefined
Data Memory (RAM)		Retained *	Undefined
General-Purpose Register (X, A, H, L, D, E, B, C)		Retained	Undefined
Bank Selection Register (MBS)		0	0
Basic Interval Timer	Counter (BT)	Undefined	Undefined
	Mode Register (BTM)	0	0
Timer/Event Counter	Counter (T0)	0	0
	Module Register (TMOD0)	FFH	FFH
	Mode Register (TM0)	0	0
	TOE0, TOUT F/F	0, 0	0, 0
Watch Timer	Mode Register (WM)	0	0

*: Data of address 0F8H to 0FDH of the data memory becomes undefined when a RESET signal is input.

Table 8-1 Status of Each Hardware after Reset (2/2)

Hardware		$\overline{RESET}$ Input in Standby Mode	$\overline{RESET}$ Input during Operation
Serial Interface	Shift Register (SIO)	Retained	Undefined
	Operation Mode Register (CSIM)	0	0
	SBI Control Register (SBIC)	0	0
	Slave Address Register (SVA)	Retained	Undefined
Clock Generator, Clock Output Circuit	Processor Clock Control Register (PCC)	0	0
	System Clock Control Register (SCC)	0	0
	Clock Output Mode Register (CLOM)	0	0
LCD Controller	Display Mode Register (LCMD)	0	0
	Display Control Register (LCDC)	0	0
Interrupt Function	Interrupt Request Flag (IRQxxx)	Reset (0)	Reset (0)
	Interrupt Enable Flag (IExxx)	0	0
	Interrupt Master Enable Flag (IME)	0	0
	INT0, INT1, INT2 Mode Registers (IM0, 1, 2)	0, 0, 0	0, 0, 0
Digital Port	Output Buffer	Off	Off
	Output Latch	Clear (0)	Clear (0)
	Input/Output Mode Register (PMGA, B)	0	0
	Pull-Up Resistor Specification Register (POGA)	0	0
Bit Sequential Buffer (BSB0-3)		Retained	Specified

9. INSTRUCTION SET

(1) Operand representation and description

Describe one or more operands in the operand field of each instruction according to the operand representation and description methods of the instruction (for details, refer to RA75X Assembler Package User's Manual - Language (EEU-730)). With some instructions, only one operand should be selected from several operands. The uppercase characters, +, and – are keywords and must be described as is.

Describe an appropriate numeric value or label as immediate data.

The symbols in the register and flag symbols can be described as labels in the places of mem, fmem, pmem, and bit (for details, refer to μPD75308 User's Manual (IEM-5016)). However, fmem and pmem restricts the label that can be described.

Representation	Description	
reg reg1	X, A, B, C, D, E, H, L X, B, C, D, E, H, L	
rp rp1 rp2	XA, BC, DE, HL BC, DE, HL BC, DE	
rpa rpa1	HL, DE, DL DE, DL	
n4 n8	4-bit immediate data or label 8-bit immediate data or label	
mem * bit	8-bit immediate data or label 2-bit immediate data or label	
fmem pmem	FB0H to FBFH,FF0H to FFFH immediate data or label FC0H to FFFH immediate data or label	
addr	μPD75312(A)	0000H-2F7FH immediate data or label
	μPD75316(A)	0000H-3F7FH immediate data or label
caddr	12-bit immediate data or label	
faddr	11-bit immediate data or label	
taddr	20H to 7FH immediate data (where bit0 = 0) or label	
PORTn IExxx MBn	PORT0 to PORT7 IEBT, IECSI, IET0, IE0, IE1, IE2, IE4, IEW MB0, MB1, MB15	

*: Only even addresses can be described as mem for 8-bit data processing.

(2) Legend of operation field

A	:	A register; 4-bit accumulator
B	:	B register; 4-bit accumulator
C	:	C register; 4-bit accumulator
D	:	D register; 4-bit accumulator
E	:	E register; 4-bit accumulator
H	:	H register; 4-bit accumulator
L	:	L register; 4-bit accumulator
X	:	X register; 4-bit accumulator
XA	:	Register pair (XA); 8-bit accumulator
BC	:	Register pair (BC); 8-bit accumulator
DE	:	Register pair (DE); 8-bit accumulator
HL	:	Register pair (HL); 8-bit accumulator
PC	:	Program counter
SP	:	Stack pointer
CY	:	Carry flag; or bit accumulator
PSW	:	Program status word
MBE	:	Memory bank enable flag
PORTn	:	Port n (n = 0 to 7)
IME	:	Interrupt mask enable flag
IExxx	:	Interrupt enable flag
MBS	:	Memory bank selector register
PCC	:	Processor clock control register
·	:	Delimiter of address and bit
(xx)	:	Contents addressed by xx
xxH	:	Hexadecimal data

(3) Symbols in addressing area field

*1	MB = MBE · MBS (MBS = 0, 1, 15)		Data memory addressing
*2	MB = 0		
*3	MBE = 0 : MB = 0 (00H-7FH) MB = 15 (80H-FFH) MBE = 1 : MB = MBS (MBS = 0, 1, 15)		
*4	MB = 15, fmem = FB0H-FBFH, FF0H-FFFH		
*5	MB = 15, pmem = FC0H-FFFH		
*6	μPD75312(A)	addr = 0000H-2F7FH	Program memory addressing
	μPD75316(A)	addr = 0000H-3F7FH	
*7	addr = (Current PC) – 15 to (Current PC) – 1 (Current PC) + 2 to (Current PC) + 16		
*8	μPD75312(A)	caddr = 0000H-0FFFH (PC_{13} = 0, PC_{12} = 0) or 1000H-1FFFH (PC_{13} = 0, PC_{12} = 1) or 2000H-2F7FH (PC_{13} = 1, PC_{12} = 0)	
	μPD75316(A)	caddr = 0000H-0FFFH (PC_{13} = 0, PC_{12} = 0) or 1000H-1FFFH (PC_{13} = 0, PC_{12} = 1) or 2000H-2FFFH (PC_{13} = 1, PC_{12} = 0) or 3000H-3F7FH (PC_{13} = 1, PC_{12} = 1)	
*9	faddr = 0000H-07FFH		
*10	taddr = 0020H-007FH		

Remarks 1: MB indicates memory bank that can be accessed.
2: In *2, MB = 0 regardless of MBE and MBS.
3: In *4 and *5, MB = 15 regardless of MBE and MBS.
4: *6 to *10 indicate areas that can be addressed.

(4) Machine cycle field

In this field, S indicates the number of machine cycles required when an instruction having a skip function skips. The value of S varies as follows:

- When no instruction is skipped .... S = 0
- When 1-byte or 2-byte instruction is skipped .... S = 1
- When 3-byte instruction (BR ! addr or CALL ! addr) is skipped .... S = 2

Note : The GETI instruction is skipped in one machine cycle.

One machine cycle equals to one cycle of the CPU clock Φ, (=t_{CY}), and can be changed in three steps depending on the setting of the processor clock control register (PCC).

Instructions	Mnemonics	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Conditions
Transfer	MOV	A, #n4	1	1	A ← n4		String effect A
		reg1, #n4	2	2	reg1 ← n4		
		XA, #n8	2	2	XA ← n8		String effect A
		HL, #n8	2	2	HL ← n8		String effect B
		rp2, #n8	2	2	rp2 ← n8		
		A, @HL	1	1	A ← (HL)	*1	
		A, @rpa1	1	1	A ← (rpa1)	*2	
		XA, @HL	2	2	XA ← (HL)	*1	
		@HL, A	1	1	(HL) ← A	*1	
		@HL, XA	2	2	(HL) ← XA	*1	
		A, mem	2	2	A ← (mem)	*3	
		XA, mem	2	2	XA ← (mem)	*3	
		mem, A	2	2	(mem) ← A	*3	
		mem, XA	2	2	(mem) ← XA	*3	
		A, reg	2	2	A ← reg		
		XA, rp	2	2	XA ← rp		
		reg1, A	2	2	reg1 ← A		
		rp1, XA	2	2	rp1 ← XA		
	XCH	A, @HL	1	1	A ↔ (HL)	*1	
		A, @rpa1	1	1	A ↔ (rpa1)	*2	
		XA, @HL	2	2	XA ↔ (HL)	*1	
		A, mem	2	2	A ↔ (mem)	*3	
		XA, mem	2	2	XA ↔ (mem)	*3	
		A, reg1	1	1	A ↔ reg1		
		XA, rp	2	2	XA ↔ rp		
Table Reference	MOVT	XA, @PCDE	1	3	XA ← $(PC_{13\text{-}8}+DE)_{ROM}$		
		XA, @PCXA	1	3	XA ← $(PC_{13\text{-}8}+XA)_{ROM}$		
Arithmetic Operation	ADDS	A, #n4	1	1+S	A ← A+n4		carry
		A, @HL	1	1+S	A ← A+(HL)	*1	carry
	ADDC	A, @HL	1	1	A, CY ← A+(HL)+CY	*1	
	SUBS	A, @HL	1	1+S	A ← A-(HL)	*1	borrow
	SUBC	A, @HL	1	1	A, CY ← A-(HL)-CY	*1	
	AND	A, #n4	2	2	A ← A ∧ n4		
		A, @HL	1	1	A ← A ∧ (HL)	*1	
	OR	A, #n4	2	2	A ← A ∨ n4		
		A, @HL	1	1	A ← A ∨ (HL)	*1	
	XOR	A, #n4	2	2	A ← A ⊻ n4		
		A, @HL	1	1	A ← A ⊻ (HL)	*1	
Accumulator Manipulation	RORC	A	1	1	CY ← A_0, A_3 ← CY, A_{n-1} ← A_n		
	NOT	A	2	2	A ← $\overline{A}$		

Instructions	Mnemonics	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Conditions
Increment/	INCS	reg	1	1+S	reg ← reg+1		reg = 0
Decrement		@HL	2	2+S	(HL) ← (HL)+1	*1	(HL) = 0
		mem	2	2+S	(mem) ← (mem)+1	*3	(mem) = 0
	DECS	reg	1	1+S	reg ← reg-1		reg = FH
Compare	SKE	reg, #n4	2	2+S	Skip if reg = n4		reg = n4
		@HL, #n4	2	2+S	Skip if (HL) = n4		*1 (HL) = n4
		A, @HL	1	1+S	Skip if A = (HL)	*1	A = (HL)
		A, reg	2	2+S	Skip if A = reg		A = reg
Carry flag	SET1	CY	1	1	CY ← 1		
Manipulation	CLR1	CY	1	1	CY ← 0		
	SKT	CY	1	1+S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	CY ← $\overline{CY}$		
Memory/	SET1	mem.bit	2	2	(mem.bit) ← 1	*3	
Bit		fmem.bit	2	2	(fmem.bit) ← 1	*4	
Manipulation		pmem.@L	2	2	(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) ← 1	*5	
		@H+mem.bit	2	2	(H + mem$_{3-0}$.bit) ← 1	*1	
	CLR1	mem.bit	2	2	(mem.bit) ← 0	*3	
		fmem.bit	2	2	(fmem.bit) ← 0	*4	
		pmem.@L	2	2	(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) ← 0	*5	
		@H+mem.bit	2	2	(H+mem$_{3-0}$.bit) ← 0	*1	
	SKT	mem.bit	2	2+S	Skip if (mem.bit) = 1	*3	(mem.bit) = 1
		fmem.bit	2	2+S	Skip if (fmem.bit) = 1	*4	(fmem.bit) = 1
		pmem.@L	2	2+S	Skip if (pmem$_{7-2}$+L$_{3-2}$.bit (L$_{1-0}$)) = 1	*5	(pmem.@L) = 1
		@H+mem.bit	2	2+S	Skip if (H + mem$_{3-0}$.bit) = 1	*1	(@H+mem.bit) = 1
	SKF	mem.bit	2	2+S	Skip if (mem.bit) = 0	*3	(mem.bit) = 0
		fmem.bit	2	2+S	Skip if (fmem.bit) = 0	*4	(fmem.bit) = 0
		pmem.@L	2	2+S	Skip if (pmem$_{7-2}$ +L$_{3-2}$.bit (L$_{1-0}$)) = 0	*5	(pmem.@L) = 0
		@H+mem.bit	2	2+S	Skip if (H + mem$_{3-0}$.bit) = 0	*1	(@H+mem.bit) = 0
	SKTCLR	fmem.bit	2	2+S	Skip if (fmem.bit) = 1 and clear	*4	(fmem.bit) = 1
		pmem.@L	2	2+S	Skip if (pmem$_{7-2}$+L$_{3-2}$.bit (L$_{1-0}$)) = 1 and clear	*5	(pmem.@L) = 1
		@H+mem.bit	2	2+S	Skip if (H+mem$_{3-0}$.bit) = 1 and clear	*1	(@H+mem.bit) = 1
	AND1	CY,fmem.bit	2	2	CY ← CY ∧ (fmem.bit)	*4	
		CY,pmem.@L	2	2	CY ← CY ∧ (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY,@H+mem.bit	2	2	CY ← CY ∧ (H+mem$_{3-0}$.bit)	*1	
	OR1	CY,fmem.bit	2	2	CY ← CY ∨ (fmem.bit)	*4	
		CY,pmem.@L	2	2	CY ← CY ∨ (pmem$_{7-2}$+L$_{3-2}$.bit (L$_{1-0}$))	*5	
		CY,@H+mem.bit	2	2	CY ← CY ∨ (H+mem$_{3-0}$.bit)	*1	
	XOR1	CY,fmem.bit	2	2	CY ← CY $\veebar$ (fmem.bit)	*4	
		CY,pmem.@L	2	2	CY ← CY $\veebar$ (pmem$_{7-2}$+L$_{3-2}$.bit (L$_{1-0}$))	*5	
		CY,@H+mem.bit	2	2	CY ← CY $\veebar$ (H+mem$_{3-0}$.bit)	*1	

Instructions	Mnemonics	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Conditions
Branch	BR	addr	—	—	PC_{13-0} ← addr (The most suitable instruction is selectable from among BR !addr, BRCB !caddr, and BR $addr depending on the assembler.)	*6	
		!addr	3	3	PC_{13-0} ← addr	*6	
		$addr	1	2	PC_{13-0} ← addr	*7	
	BRCB	!caddr	2	2	PC_{13-0} ← $PC_{13,12}$ + $caddr_{11-0}$	*8	
Subroutine/ Stack Control	CALL	!addr	3	3	(SP-4)(SP-1)(SP-2) ← PC_{11-0} (SP-3) ← MBE, 0, PC_{13}, PC_{12} PC_{13-0} ← addr, SP ← SP-4	*6	
	CALLF	!faddr	2	2	(SP-4)(SP-1)(SP-2) ← PC_{11-0} (SP-3) ← MBE, 0, PC_{13}, PC_{12} PC_{13-0} ← 00, faddr, SP ← SP-4	*9	
	RET		1	3	MBE, PC_{13}, PC_{12} ← $(SP+1)_{3,1,0}$ PC_{11-0} ← (SP)(SP+3)(SP+2) SP ← SP+4		
	RETS		1	3+S	MBE, PC_{13}, PC_{12} ← $(SP+1)_{3,1,0}$ PC_{11-0} ← (SP)(SP+3)(SP+2) SP ← SP+4, then skip unconditionally		Undefined
	RETI		1	3	PC_{13}, PC_{12} ← $(SP+1)_{1,0}$ PC_{11-0} ← (SP)(SP+3)(SP+2) PSW ← (SP+4)(SP+5), SP ← SP+6		
	PUSH	rp	1	1	(SP-1)(SP-2) ← rp, SP ← SP-2		
		BS	2	2	(SP-1) ← MBS, (SP-2) ← 0, SP ← SP-2		
	POP	rp	1	1	rp ← (SP+1)(SP), SP ← SP+2		
		BS	2	2	MBS ← (SP+1), SP ← SP+2		
Interrupt Control	EI		2	2	IME ← 1		
		IExxx	2	2	IExxx ← 1		
	DI		2	2	IME ← 0		
		IExxx	2	2	IExxx ← 0		
I/O	IN	A,PORTn	2	2	A ← $PORT_n$ (n = 0-7)		
		XA,PORTn	2	2	XA ← $PORT_{n+1}$,$PORT_n$ (n = 4, 6)		
	OUT	PORTn,A	2	2	$PORT_n$ ← A (n = 2-7)		
		PORTn,XA	2	2	$PORT_{n+1}$,$PORT_n$ ← XA (n = 4, 6)		
CPU Control	HALT		2	2	Set HALT Mode (PCC.2 ← 1)		
	STOP		2	2	Set STOP Mode (PCC.3 ← 1)		
	NOP		1	1	No Operation		
Special	SEL	MBn	2	2	MBS ← n (n = 0, 1, 15)		
	GETI	taddr	1	3	· Where TBR instruction, PC_{13-0} ← $(taddr)_{5-0}$+(taddr+1)	*10	
					· Where TCALL instruction, (SP-4)(SP-1)(SP-2) ← PC_{11-0} (SP-3) ← MBE, 0, PC_{13}, PC_{12} PC_{13-0} ← $(taddr)_{5-0}$+(taddr+1) SP ← SP-4		
					· Except for TBR and TCALL instructions, Instruction execution of (taddr)(taddr+1)		Depends on referenced instruction

Note: When executing the IN/OUT instruction, MBE = 0, or MBE = 1, and MBS = 15.

Remarks: The TBR and TCALL instructions are the assembler pseudo-instructions for the table definition of GETI instruction.

10. SELECTION OF MASK OPTION

The following mask operations are available and can be specified for each pin.

Pin	Mask Option
P40-P43, P50-P53	• With pull-up resistor (Specification in bit units) • Without pull-up resistor (Specification in bit units)
V_{LC0}-V_{LC2}, BIAS	• With dividing resistor for LCD drive power source (Specification in 4-bit units) • Without dividing resistor for LCD drive power source (Specification in 4-bit units)

11. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply Voltage	V_{DD}			-0.3 to +7.0	V
Input Voltage	V_{I1}	Other than ports 4, 5		-0.3 to V_{DD}+0.3	V
	V_{I2}	Ports 4, 5	w/pull-up resistor	-0.3 to V_{DD}+0.3	V
			Open drain	-0.3 to +11	V
Output Voltage	V_O			-0.3 to V_{DD}+0.3	V
High-Level Output Current	I_{OH}	1 pin	Peak	-10	mA
			rms	-5	mA
		All pins	Peak	-30	mA
			rms	-5	mA
Low-Level Output Current	I_{OL}*	1 pin	Peak	10	mA
			rms	5	mA
		Other than ports 0, 2, 3, 5	Peak	100	mA
			rms	60	mA
		Total of ports 4, 6, 7	Peak	100	mA
			rms	50	mA
Operating Temperature	T_{opt}			-40 to +85	°C
Storage Temperature	T_{stg}			-65 to +150	°C

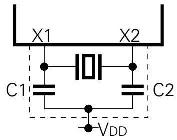
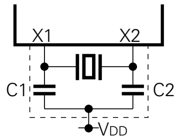
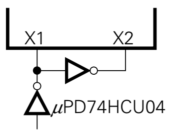
*: rms = Peak value x $\sqrt{Duty}$

CAPACITANCE (T_a = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{IN}	f = 1 MHz			15	pF
Output Capacitance	C_{OUT}	Pins other than thosemeasured are at 0 V			15	pF
Input/Output Capacitance	C_{IO}				15	pF

MAIN SYSTEM CLOCK OSCILLATOR CIRCUIT CHARACTERISTICS

(T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

Oscillator	Recommended Constants	Item	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic *3		Oscillation frequency(f_X)*1		1.0		5.0 *3	MHz
		Oscillation stabilization time*2	After V_{DD} came to MIN. of oscillation voltage range			4	ms
Crystal *3		Oscillation frequency (f_X)*1		1.0	4.19	5.0 *3	MHz
		Oscillation stabilization time*2	V_{DD} = 4.5 to 6.0 V			10	ms
						30	ms
External Clock		X1 input frequency (f_X)*1		1.0		5.0 *3	MHz
		X1 input high-, low-level widths (t_{XH}, t_{XL})		100		500	ns

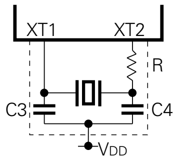
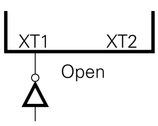
*1: The oscillation frequency and X1 input frequency are indicated only to express the characteristics of the oscillator circuit.
For instruction execution time, refer to AC Characteristics.

2: Time required for oscillation to stabilize after V_{DD} reaches the minimum value of the oscillation voltage range or the STOP mode has been released.

★ 3: When the oscillation frequency is 4.19 MHz < fx ≤ 5.0 MHz, do not select PCC = 0011 as the instruction execution time: otherwise, one machine cycle is set to less than 0.95 μs, falling short of the rated minimum value of 0.95 μs.

SUBSYSTEM CLOCK OSCILLATOR CIRCUIT CHARACTERISTICS

(T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

Oscillator	Recommended Constants	Item	Conditions	MIN.	TYP.	MAX.	Unit
Crystal		Oscillation frequency (f_{XT})		32	32.768	35	kHz
		Oscillation stabilization time*	V_{DD} = 4.5 to 6.0 V		1.0	2	s
						10	s
External Clock		XT1 input frequency (f_{XT})*		32		100	kHz
		XT1 input high-, low-level widths (t_{XTH}, t_{XTL})		5		15	μs

*: Time required for oscillation to stabilize after V_{DD} reaches the minimum value of the oscillation voltage range.

Note: When using the oscillation circuit of the main system clock and subsystem clock, wire the portion enclosed in dotted line in the figures as follows to avoid adverse influences on the wiring capacity:

- Keep the wiring length as short as possible.
- Do not cross the wiring over the other signal lines. Do not route the wiring in the vicinity of lines through which a high alternating current flows.
- Always keep the ground point of the capacitor of the oscillator circuit at the same potential as V_{DD}. Do not connect the power source pattern through which a high current flows.
- Do not extract signals from the oscillation circuit.

The amplification factor of the subsystem clock oscillation circuit is designed to be low to reduce the current dissipation and therefore, the subsystem clock oscillation circuit is influenced by noise more easily than the main system clock oscillation circuit. When using the subsystem clock, therefore, exercise utmost care in wiring the circuit.

DC CHARACTERISTICS (T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-Level Input Voltage	V_{IH1}	Ports 2, 3		$0.7V_{DD}$		V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, 7, $\overline{RESET}$		$0.8V_{DD}$		V_{DD}	V
	V_{IH3}	Ports 4, 5	w/pull-up resistor	$0.7V_{DD}$		V_{DD}	V
			Open-drain	$0.7V_{DD}$		10	V
	V_{IH4}	X1, X2, XT1		V_{DD}-0.5		V_{DD}	V
Low-level Input Voltage	V_{IL1}	Ports 2, 3, 4, 5		0		$0.3V_{DD}$	V
	V_{IL2}	Ports 0, 1, 6, 7, $\overline{RESET}$		0		$0.2V_{DD}$	V
	V_{IL3}	X1, X2, XT1		0		0.4	V
High-Level Output Voltage	V_{OH1}	Ports 0, 2, 3, 6, 7 and BIAS	V_{DD} = 4.5 to 6.0 V I_{OH} = -1 mA	V_{DD}-1.0			V
			I_{OH} = -100 μA	V_{DD}-0.5			V
	V_{OH2}	BP0-7 (with two I_{OH} outputs)	V_{DD} = 4.5 to 6.0 V I_{OH} = -100 μA	V_{DD}-2.0			V
			I_{OH} = -30 μA	V_{DD}-1.0			V
Low-Level Output Voltage	V_{OL1}	Ports 0, 2, 3, 4, 5, 6, 7, and 8	Ports 3, 4, and 5 V_{DD} = 4.5 to 6.0 V I_{OL} = -15 mA		0.2	1.0	V
			V_{DD} = 4.5 to 6.0 V I_{OL} = 1.6 mA			0.4	V
			I_{OL} = 400 μA			0.5	V
		SB0, 1	Open-drain Pull-up resistor ≥ 1 kΩ			$0.2V_{DD}$	V
	V_{OL2}	BP0-7 (with two I_{OL} outputs)	V_{DD} = 4.5 to 6.0 V I_{OL} = 100 μA			1.0	V
			I_{OL} = 50 μA			1.0	V
High-Level Input Leakage Current	I_{LIH1}	V_{IN} = V_{DD}	Other than below			3	μA
	I_{LIH2}		X1, X2, XT1			20	μA
	I_{LIH3}	V_{IN} = 10 V	Ports 4, 5 (open-drain)			20	μA
Low-Level Input Leakage Current	I_{LIL1}	V_{IN} = 0 V	Other than below			-3	μA
	I_{LIL2}		X1, X2, XT1			-20	μA
High-Level Output Leakage Current	I_{LOH1}	V_{OUT} = V_{DD}	Other than below			3	μA
	I_{LOH2}	V_{OUT} = 10 V	Ports 4, 5 (open-drain)			20	μA
Low-Level Output Leakage Current	I_{LOL}	V_{OUT} = 0 V				-3	μA
Internal Pull-Up Resistor	R_{L1}	Ports 0, 1, 2, 3, 6, 7 (except P00) V_{IN} = 0V	V_{DD} = 5.0 V±10%	15	40	80	kΩ
			V_{DD} = 3.0 V±10%	30		300	kΩ
	R_{L2}	Ports 4, 5 V_{OUT} = V_{DD}-2.0 V	V_{DD} = 5.0 V±10%	15	40	70	kΩ
			V_{DD} = 3.0 V±10%	10		60	kΩ
LCD Drive Voltage	V_{LCD}			2.5		V_{DD}	V
LCD Step-down Resistor	R_{LCD}			60	100	150	kΩ
LCD Output Voltage Deviation (Common) [*1]	V_{ODC}	I_O = ±5 μA	V_{LCD0} = V_{LCD} V_{LCD1} = V_{LCD}×2/3 V_{LCD2} = V_{LCD}×1/3 2.7 V ≤ V_{LCD} ≤ V_{DD}	0		±0.2	V
LCD Output Voltage Deviation (Segment)	V_{ODS}	I_O = ±1 μA		0		±0.2	V

(to be cont'd)

(cont'd)

<table>
<tr><th>Parameter</th><th>Symbol</th><th colspan="3">Conditions</th><th>MIN.</th><th>TYP.</th><th>MAX.</th><th>Unit</th></tr>
<tr><td rowspan="9">Supply Current *2</td><td rowspan="2">I_{DD1}</td><td rowspan="4">4.19 MHz*3 crystal oscillator
C1 = C2 = 22pF</td><td colspan="2">V_{DD} = 5 V±10%*4</td><td></td><td>2.5</td><td>8</td><td>mA</td></tr>
<tr><td colspan="2">V_{DD} = 3 V±10%*5</td><td></td><td>0.35</td><td>1.2</td><td>mA</td></tr>
<tr><td rowspan="2">I_{DD2}</td><td rowspan="2">HALT mode</td><td>V_{DD} = 5 V±10%</td><td></td><td>500</td><td>1500</td><td>μA</td></tr>
<tr><td>V_{DD} = 3 V±10%</td><td></td><td>150</td><td>450</td><td>μA</td></tr>
<tr><td>I_{DD3}</td><td rowspan="2">32 kHz*6 crystal oscillato</td><td colspan="2">V_{DD} = 3 V±10%</td><td></td><td>30</td><td>90</td><td>μA</td></tr>
<tr><td>I_{DD4}</td><td>HALT mode</td><td>V_{DD} = 3 V±10%</td><td></td><td>5</td><td>15</td><td>μA</td></tr>
<tr><td rowspan="3">I_{DD5}</td><td rowspan="3">XT1 = 0 V
STOP mode</td><td colspan="2">V_{DD} = 5 V±10%</td><td></td><td>0.5</td><td>20</td><td>μA</td></tr>
<tr><td rowspan="2">V_{DD} = 3 V±10%</td><td></td><td></td><td>0.1</td><td>10</td><td>μA</td></tr>
<tr><td>T_a = 25°C</td><td></td><td>0.1</td><td>5</td><td>μA</td></tr>
</table>

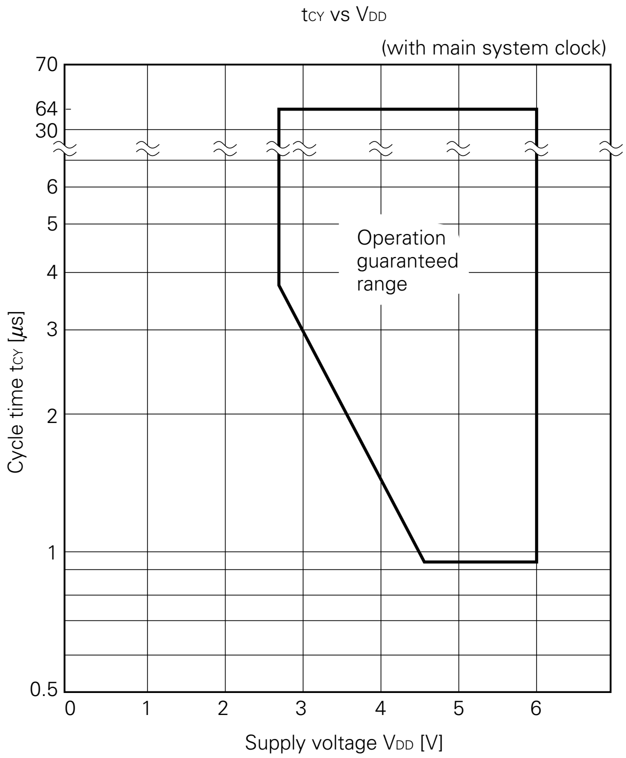
*1: "Voltage deviation" means the difference between the ideal segment or common output value (V_{LCDn}: n = 0, 1, 2) and output voltage.
2: Currents for the built-in pull-up resistor and the LCD step-down resistor are not included.
3: Including when the subsystem clock is operated.
4: When operand in the high-speed mode with the processor clock control register (PCC) set to 0011.
5: When operated in the low-speed mode with the PCC set to 0000.
6: When operated with the subsystem clock by setting the system clock control register (SCC) to 1001 to stop the main system clock operation.

AC CHARACTERISTICS (T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
CPU Clock Cycle Time (Minimum Instruction Execution Time = 1 Machine Cycle)*1	t_{CY}	w/main system clock	V_{DD} = 4.5 to 6.0 V	0.95		64	μs
				3.8		64	μs
		w/sub-system clock		114	122	125	μs
TI0 Input Frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		1	MHz
				0		275	kHz
TI0 Input High-, Low-Level Widths	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		0.48			μs
				1.8			μs
Interrupt Input High-, Low-Level Widths	t_{INTH}, t_{INTL}	INT0		*2			μs
		INT1, 2, 4		10			μs
		KR0-7		10			μs
$\overline{\text{RESET}}$ Low-Level Width	t_{RSL}			10			μs

*1: The CPU clock (Φ) cycle time is determined by the oscillation frequency of the connected oscillator, system clock control register (SCC), and processor clock control register (PCC).
The figure on the right is cycle time t_{CY} vs. supply voltage V_{DD} characteristics at the main system clock.

2: $2t_{CY}$ or $128/f_X$ depending on the setting of the interrupt mode register (IM0).



SERIAL TRANSFER OPERATION

Two-Line and Three-Line Serial I/O Modes ($\overline{SCK}$: internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ High-, Low-Level Widths	t_{KL1}	V_{DD} = 4.5 to 6.0 V		t_{KCY1}/2-50			ns
	t_{KH1}			t_{KCY1}/2-150			ns
SI Set-Up Time (vs. $\overline{SCK}$ ↑)	t_{SIK1}			150			ns
SI Hold Time (vs. $\overline{SCK}$ ↑)	t_{KSI1}			400			ns
$\overline{SCK}$ ↓→ SO Output Delay Time	t_{KSO1}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V			250	ns
						1000	ns

TWO-LINE AND THREE-LINE SERIAL I/O MODES ($\overline{SCK}$: external clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY2}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ High-, Low-Level Widths	t_{KL2}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KH2}			1600			ns
SI Set-Up Time (vs. $\overline{SCK}$ ↑)	t_{SIK2}			100			ns
SI Hold Time (vs. $\overline{SCK}$ ↑)	t_{KSI2}			400			ns
$\overline{SCK}$ ↓→ SO Output Delay Time	t_{KSO2}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns

*: R_L and C_L are load resistance and load capacitance of the SO output line.

SBI MODE ($\overline{SCK}$: internal clock output (master))

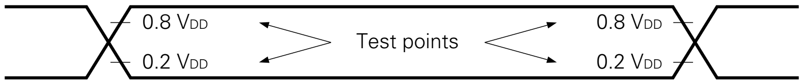
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ High-, Low-Level Widths	t_{KL3} t_{KH3}	V_{DD} = 4.5 to 6.0 V		t_{KCY3}/2-50			ns
				t_{KCY3}/2-150			ns
SB0, 1 Set-Up Time (vs. $\overline{SCK}$ ↑)	t_{SIK3}			150			ns
SB0, 1 Hold Time (vs. $\overline{SCK}$ ↑)	t_{KSI3}			t_{KCY3}/2			ns
$\overline{SCK}$ ↓→ SB0, 1 Output Delay Time	t_{KSO3}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
$\overline{SCK}$ ↑→ SB0, 1 ↓	t_{KSB}			t_{KCY3}			ns
SB0,1 ↓→ $\overline{SCK}$	t_{SBK}			t_{KCY3}			ns
SB0, 1 Low-Level Width	t_{SBL}			t_{KCY3}			ns
SB0, 1 High-Level Width	t_{SBH}			t_{KCY3}			ns

SBI MODE ($\overline{SCK}$: external clock input (slave))

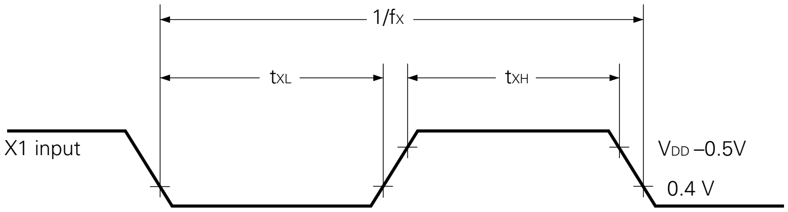
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ High-, Low-Level Widths	t_{KL4} t_{KH4}	V_{DD} = 4.5 to 6.0 V		400			ns
				1600			ns
SB0, 1 Set-Up Time (vs. $\overline{SCK}$ ↑)	t_{SIK4}			100			ns
SB0, 1 Hold Time (vs. $\overline{SCK}$ ↑)	t_{KSI4}			t_{KCY4}/2			ns
$\overline{SCK}$ ↓→ SB0, 1 Output Delay Time	t_{KSO4}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
$\overline{SCK}$ ↑→ SB0, 1 ↓	t_{KSB}			t_{KCY4}			ns
SB0,1 ↓→ $\overline{SCK}$ ↓	t_{SBK}			t_{KCY4}			ns
SB0, 1 Low-Level Width	t_{SBL}			t_{KCY4}			ns
SB0, 1 High-Level Width	t_{SBH}			t_{KCY4}			ns

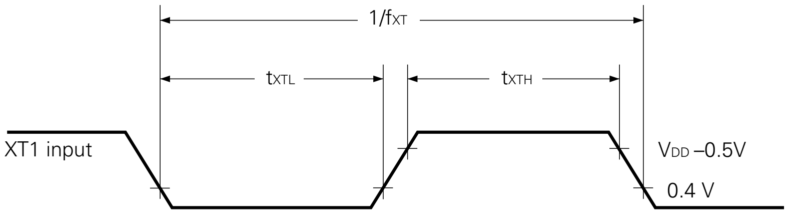
*: R_L and C_L are load resistance and load capacitance of the SB0 and SB1 output lines.

AC TIMING TEST POINT (excluding X1 and XT1 inputs)

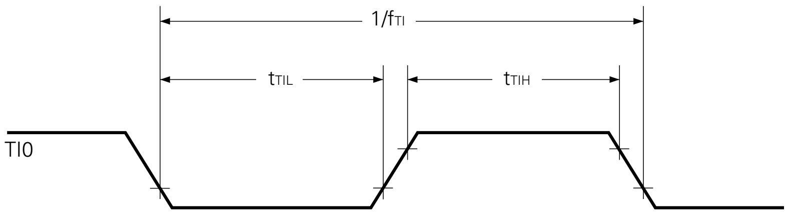


CLOCK TIMING



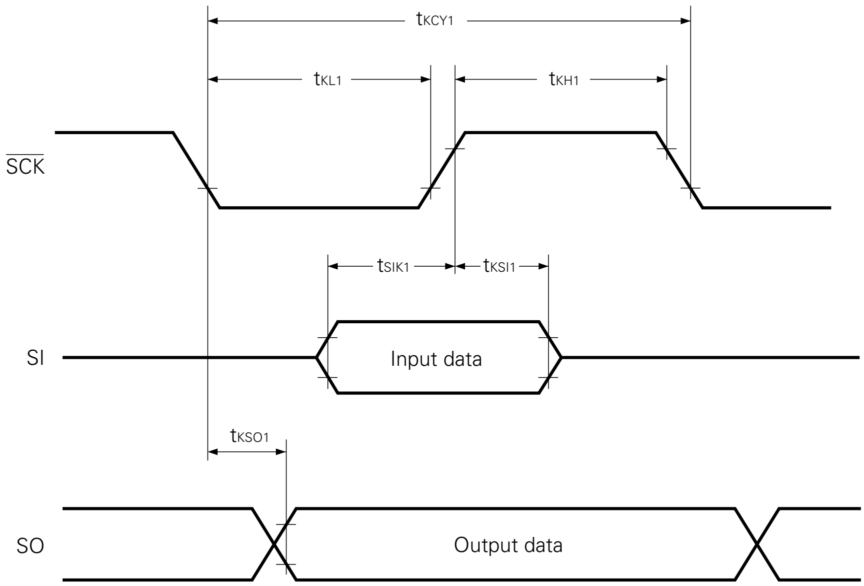


TI0 TIMING

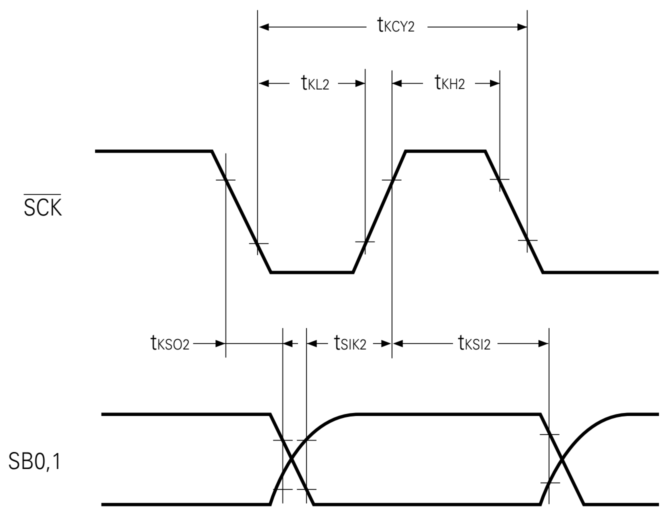


SERIAL TRANSFER TIMING

THREE-LINE SERIAL I/O MODE:

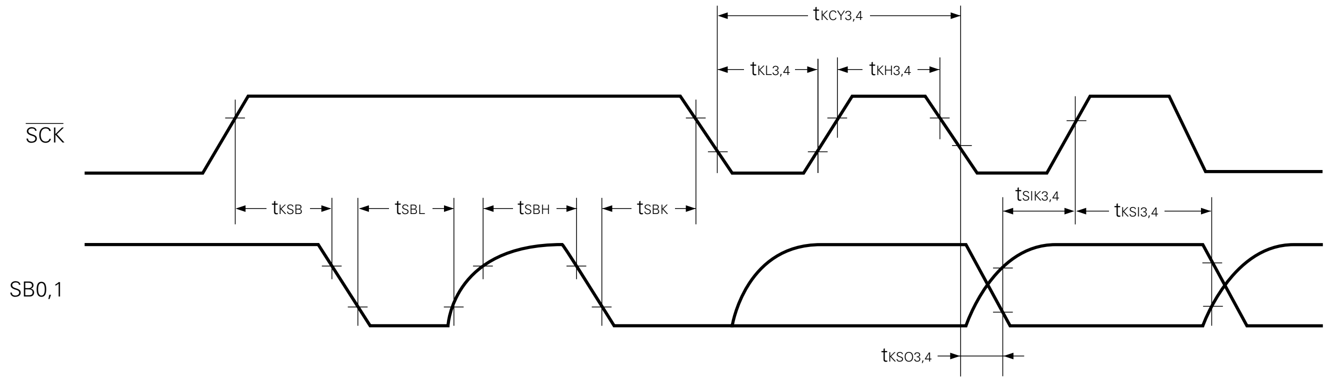


TWO-LINE SERIAL I/O MODE:

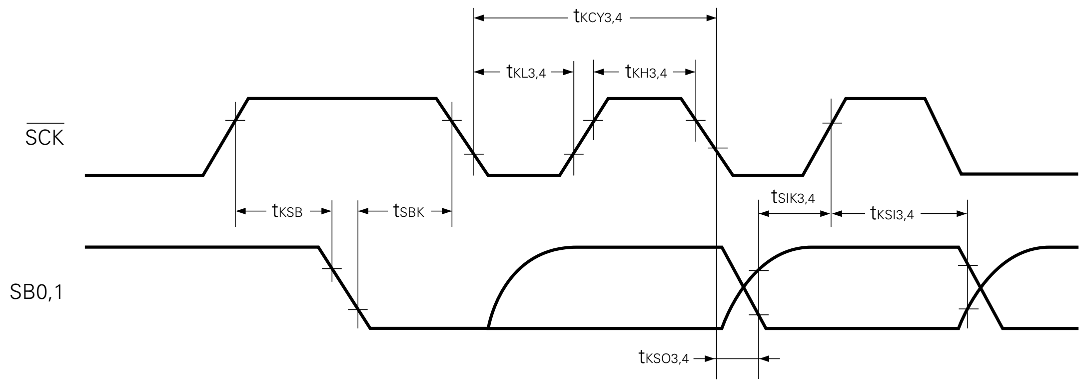


SERIAL TRANSFER TIMING

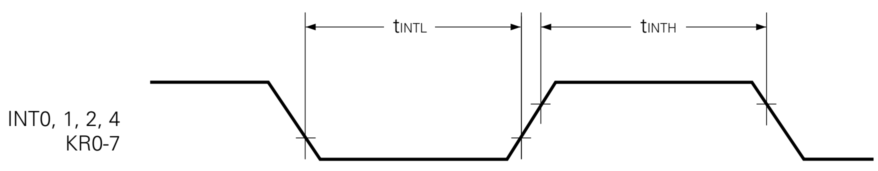
BUS RELEASE SIGNAL TRANSFER:



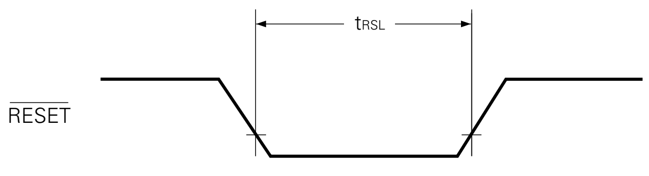
COMMAND SIGNAL TRANSFER:



INTERRUPT INPUT TIMING:



RESET INPUT TIMING:



LOW-VOLTAGE DATA RETENTION CHARACTERISTICS OF DATA MEMORY IN STOP MODE
(T_a = −40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data Retention Supply Voltage	V_{DDDR}		2.0		6.0	V
Data Retention Supply Current*1	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release Signal Set Time	t_{SREL}		0			μs
Oscillation Stabilization Wait Time*2	t_{WAIT}	Released by $\overline{RESET}$		$2^{17}/f_X$		ms
		Released by interrupt		*3		ms

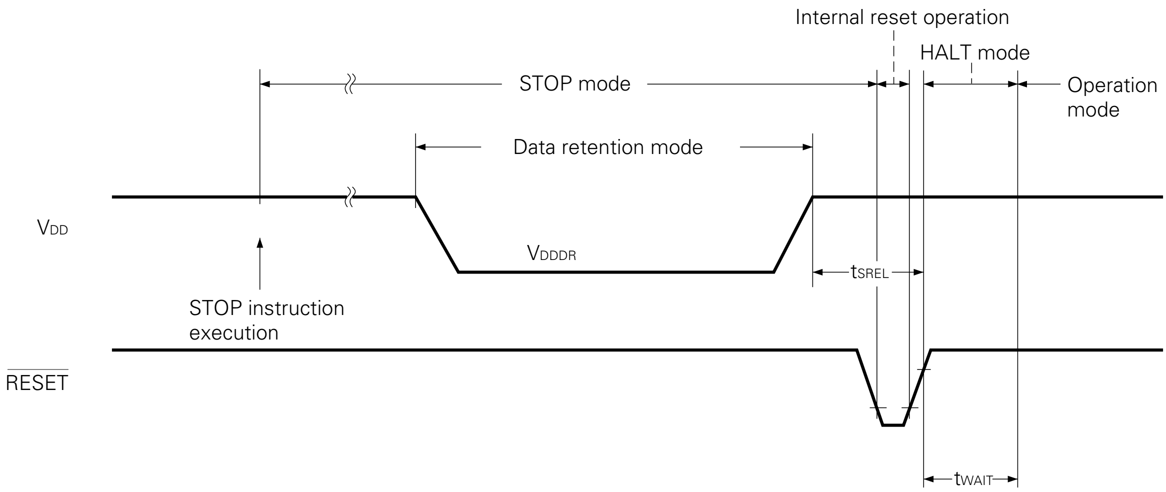
*1: Does not include current flowing through internal pull-up resistor

2: The oscillation stabilization wait time is the time during which the CPU is stopped to prevent unstable operation when oscillation is started.

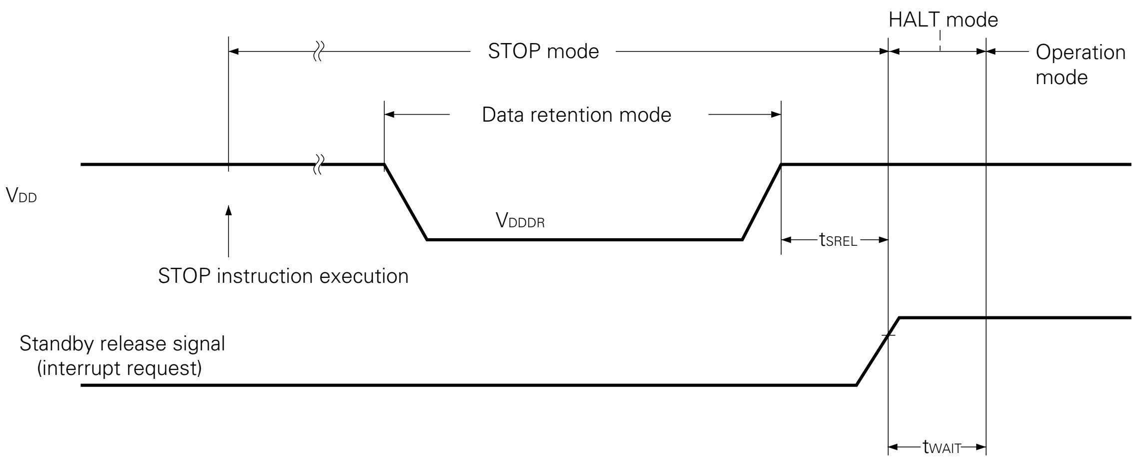
3: Depends on the setting of the basic interval timer mode register (BTM) as follows:

BTM3	BTM2	BTM1	BTM0	WAIT time ( ): f_X = 4.19 MHz
–	0	0	0	$2^{20}/f_X$ (approx. 250 ms)
–	0	1	1	$2^{17}/f_X$ (approx. 31.3 ms)
–	1	0	1	$2^{15}/f_X$ (approx. 7.82 ms)
–	1	1	1	$2^{13}/f_X$ (approx. 1.95 ms)

DATA RETENTION TIMING (releasing STOP mode by $\overline{RESET}$)

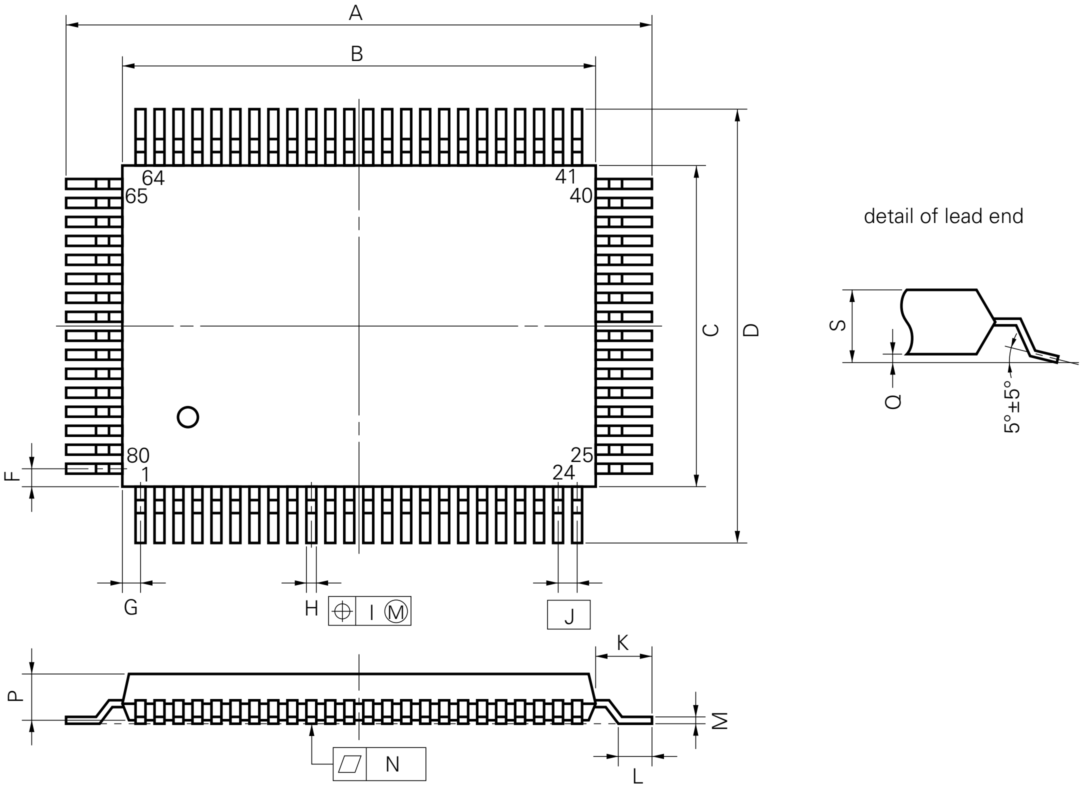


DATA RETENTION TIMING (standby release signal: releasing STOP mode by interrupt)



12. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (14×20)



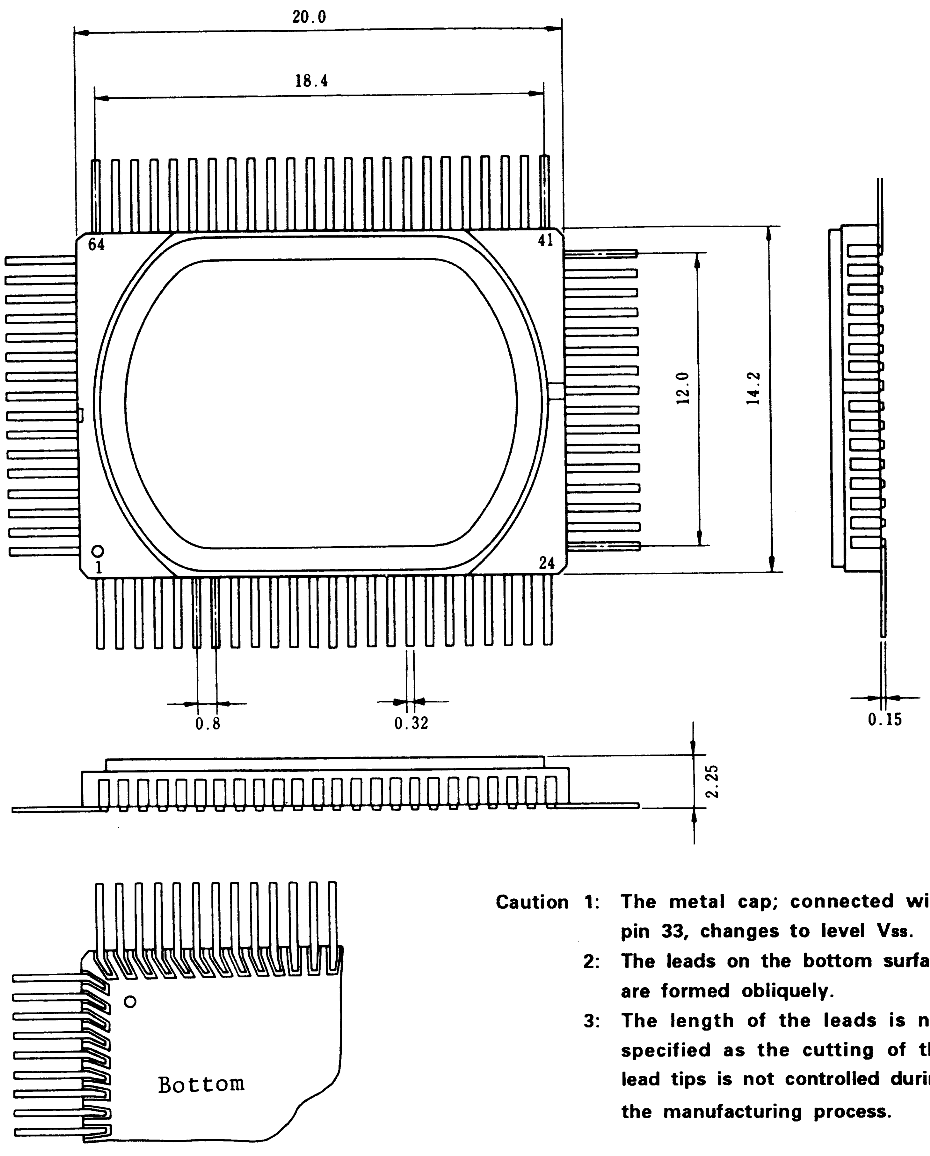
P80GF-80-3B9-2

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	0.8	0.031
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

80-PIN CERAMIC QFP FOR ES (REFERENCE) (UNITS IN mm)



Caution 1: The metal cap; connected with pin 33, changes to level V_{SS}.

2: The leads on the bottom surface are formed obliquely.

3: The length of the leads is not specified as the cutting of the lead tips is not controlled during the manufacturing process.

13. RECOMMENDED SOLDERING CONDITIONS

It is recommended that μPD75316(A) be soldered under the following conditions.

For details on the recommended soldering conditions, refer to Information Document "Semiconductor Devices Mounting Manual" (IEI-616).

The soldering methods and conditions are not listed here, consult NEC.

Table 13-1 Soldering Conditions

μPD75312GF(A) - xxx - 3B9: 80-pin plastic QFP (14×20 mm)
μPD75316GF(A) - xxx - 3B9: 80-pin plastic QFP (14×20 mm)

Soldering Method	Soldering Conditions	Symbol for Recommended Condition
Infrared Reflow	Package peak temperature: 230°C, time: 30 seconds max. (210°C min.), number of times: 1	IR30-00-1
VPS	Package peak temperature: 215°C, time: 40 seconds max. (200°C min.), number of times: 1	VP15-00-1
Wave Soldering	Soldering bath temperature: 260°C max., time: 10 seconds max., number of times: 1, pre-heating temperature: 120°C max. (package surface temperature)	WS60-00-1
Pin Partial Heating	Pin temperature: 300°C max., time: 3 seconds max. (per side)	—

Caution: Do not use two or more soldering methods in combination (except the pin partial heating method).

Notice

A model that can be soldered under the more stringent conditions (infrared reflow peak temperature: 235°C, number of times: 2, and an extended number of days) is also available. For details, consult NEC.

APPENDIX A. COMPARISION OF FEATURES AMONG THIS SERIES PRODUCTS

Item \ Product		μPD75304(A)	μPD75306(A)	μPD75308(A)	μPD75312(A)	μPD75316(A)	μPD75P308	μPD75P316	μPD75P316A
ROM Configuration		Mask ROM					EPROM/One-time PROM*1		
ROM (bits)		000H-FFFH 4096 × 8	0000H-177FH 6016 × 8	0000H-1F7FH 8064 × 8	0000H-2F7FH 12160 × 8	0000H-3F7FH 16256 × 8	0000H-1F7FH 8064 × 8	0000H-3F7FH 16256 × 8	0000H-3F7FH 16256 × 8
RAM (bits)		512 × 4 (bank 0, 1 : 256 × 4)							*2
Instruction Set	3-byte Branch Instruction	None	Provided						
	Others	Commonly provided							
Program Counter		12 bits	13 bits		14 bits		13 bits	14 bits	
Mask Option		• Pull-up resistor for Ports 4, 5 • Dividing resistor for LCD driving supply voltage					Not offered		
V_{PP}, PROM Programming Pin Connections		None					Offered		
Directly Driving LED		Not offered					Offered		
Electrical Characteristics	Operating Supply Voltage Range	2.7 to 6.0 V					5 V ± 5%	5 V ± 5%	2.7 to 6.0 V
	Absolute Maximum Ratings	Differ in high-level output current and low-level output current							
	DC Characteristics	Differ in low-level output voltage							
Quality Grade		Special					Standard		
Package		• 80-pin plastic QFP (14 × 20 mm)					• 80-pin plastic QFP (14 × 20 mm) • 80-pin ceramic LCC w/ window	• 80-pin plastic QFP (14 × 20 mm)	• 80-pin plastic QFP (14 × 20 mm) • 80-pin ceramic LCC w/ window

*1: For the μPD75P316, only the one-time PROM is provided.
2: 1024 × 4 (Banks 0, 1, 2, 3, 15 : 256 × 4)

APPENDIX B. DEVELOPMENT TOOLS ★

The following development support tools are readily available to support development of systems using μPD75312(A) and 75316(A):

Hardware	IE-75000-R *1 IE-75001-R	In-circuit emulator for 75X series
	IE-75000-R-EM *2	Emulation board for IE-75000-R and IE-75001-R
	EP-75308GF-R EV-9200G-80	Emulation prove for μPD75312GF(A) and 75316GF(A), provided with 80-pin conversion socket EV-9200G-80.
	PG-1500	PROM programmer
	PA-75P308GF	PROM programmer adapter solely used for μPD75P316GF and 75P316AGF. It is connected to PG-1500.
Software	IE Control Program	Host machine PC-9800 series (MS-DOS™ Ver.3.30 to Ver.5.00A*3) IBM PC/AT™ (PC DOS™ Ver.3.1)
	PG-1500 Controller	
	RA75X Relocatable Assembler	

*1: Maintenance product
2: Not provided with IE-75001-R.
3: Ver.5.00/5.00A has a task swap function, but this function cannot be used with this function.

Remarks: For development tools from other companies, refer to 75X Series Selection Guide (IF-151).

APPENDIX C. RELATED DOCUMENTS

GENERAL NOTES ON CMOS DEVICES

① STATIC ELECTRICITY (ALL MOS DEVICES)

Exercise care so that MOS devices are not adversely influenced by static electricity while being handled.

The insulation of the gates of the MOS device may be destroyed by a strong static charge. Therefore, when transporting or storing the MOS device, use a conductive tray, magazine case, or conductive buffer materials, or the metal case NEC uses for packaging and shipment, and use grounding when assembling the MOS device system. Do not leave the MOS device on a plastic plate and do not touch the pins of the device.

Handle boards on which MOS devices are mounted similarly .

② PROCESSING OF UNUSED PINS (CMOS DEVICES ONLY)

Fix the input level of CMOS devices.

Unlike bipolar or NMOS devices, if a CMOS device is operated with nothing connected to its input pin, intermediate level input may be generated due to noise, and an inrush current may flow through the device, causing the device to malfunction. Therefore, fix the input level of the device by using a pull-down or pull-up resistor. If there is a possibility that an unused pin serves as an output pin (whose timing is not specified), each pin should be connected to V_{DD} or GND through a resistor.

Refer to "Processing of Unused Pins" in the documents of each devices.

③ STATUS BEFORE INITIALIZATION (ALL MOS DEVICES)

The initial status of MOS devices is undefined upon power application.

Since the characteristics of an MOS device are determined by the quantity of injection at the molecular level, the initial status of the device is not controlled during the production process. The output status of pins, I/O setting, and register contents upon power application are not guaranteed. However, the items defined for reset operation and mode setting are subject to guarantee after the respective operations have been executed.

When using a device with a reset function, be sure to reset the device after power application.

[MEMO]