NEC

MOS INTEGRATED CIRCUIT

μPD77210, 77213

16-BIT FIXED-POINT DIGITAL SIGNAL PROCESSOR

The μPD77210 and 77213 are 16-bit fixed-point digital signal processors (DSP).

Compared with the existing members of the μPD77111 Family, the μPD77210 Family consumes less power and is ideal for battery-driven mobile terminal applications such as PDAs and cellular telephones. The μP77210 Family is DSP is also compatible with the μPD77111 Family at the binary level.

The μPD77210 Family consists of the μPD77210 and 77213. Unless otherwise specified, the μPD77210 Family refers to the entire family. If there are some differences in function or operation among family products, they are described under their respective names.

The functions of the μPD77210 Family are described in detail in the following user's manuals. Refer to these manuals when designing your system.

μPD77210 Family User's Manual - Architecture:	In preparation
μPD77016 Family User's Manual - Instructions:	U13116E

FEATURES

- Instruction cycle (operating clock):
  - μPD77210 6.25 ns MIN. (160 MHz MAX.)
  - μPD77213 8.33 ns MIN. (120 MHz MAX.)

- Memory
  - -Internal instruction memory:
    - μPD77210 :RAM 31.5 Kwords x 32 bits
    - μPD77213 :RAM 15.5 Kwords x 32 bits
      ROM 64 Kwords x 32 bits
  - -Data memory:
    - μPD77210 :RAM 30 Kwords x 16 bits x 2 planes (X and Y data memories)
      External memory space 1 Mwords x 16 bits (common to X and Y data memories)
    - μPD77213 :RAM 18 Kwords x 16 bits x 2 planes (X and Y data memories)
      ROM 32 Kwords x 16 bits x 2 planes (X and Y data memories)
      External memory space 1 Mwords x 16 bits (common to X and Y data memories)

- Peripheral
  - -Audio serial interface: 1 channel
  - -Time-division serial interface: 1 channel
  - -16-bit host interface: 1 channel
  - -16-bit general-purpose port
  - -16-bit timer: 2 channels
  - -Peripheral-memory DMA transfer function
  - -SD (Secure Digital) card interface
    :μPD77213 only

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The mark ★ shows major revised points.

• Supply voltage

-DSP core supply voltage: 1.425 to 1.65 V (MAX. operating speed 120 MHz),
1.55 to 1.65 V (MAX. operating speed 160 MHz) μPD77210 only

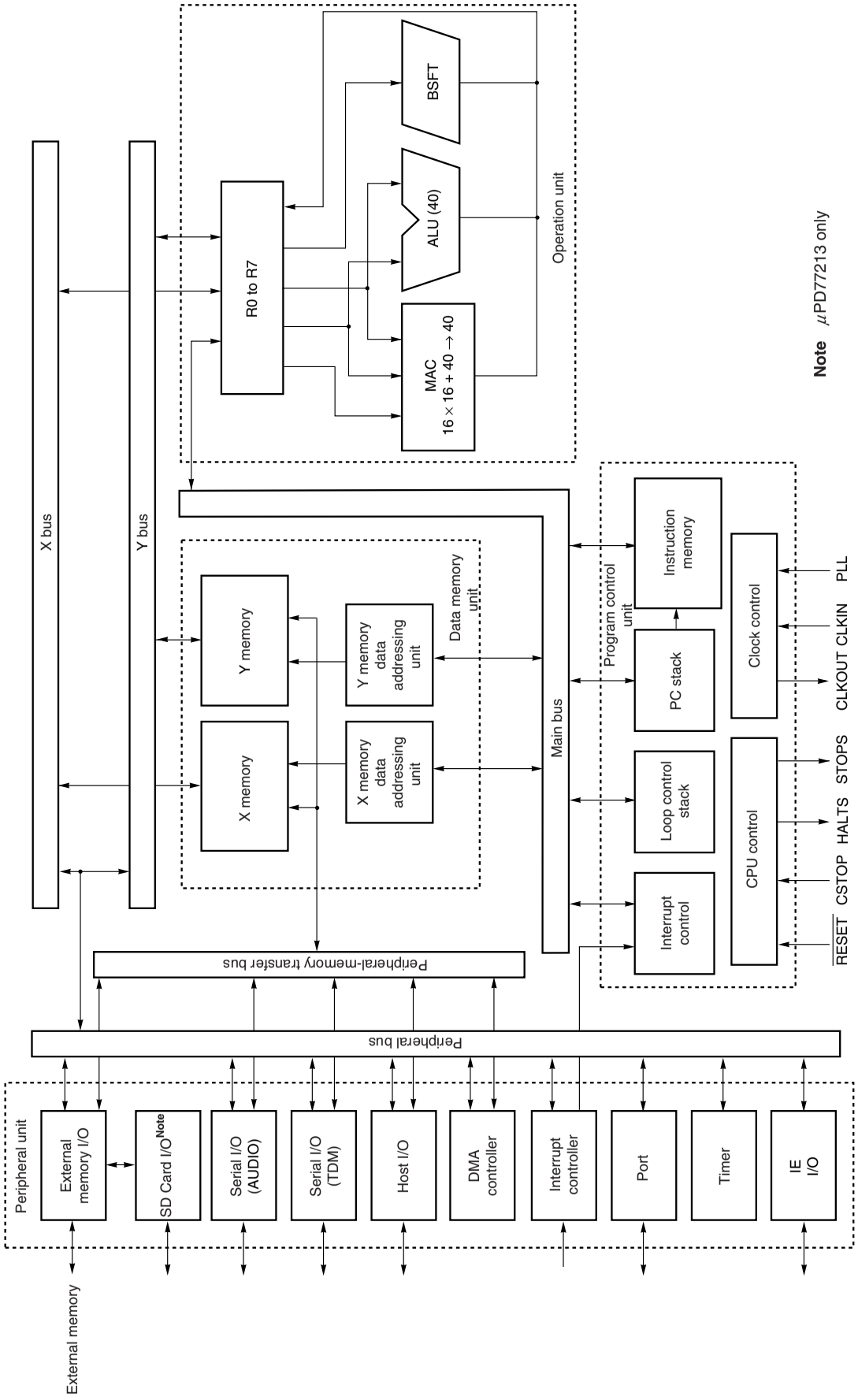
-I/O pin supply voltage: 2.7 to 3.6 V

ORDERING INFORMATION

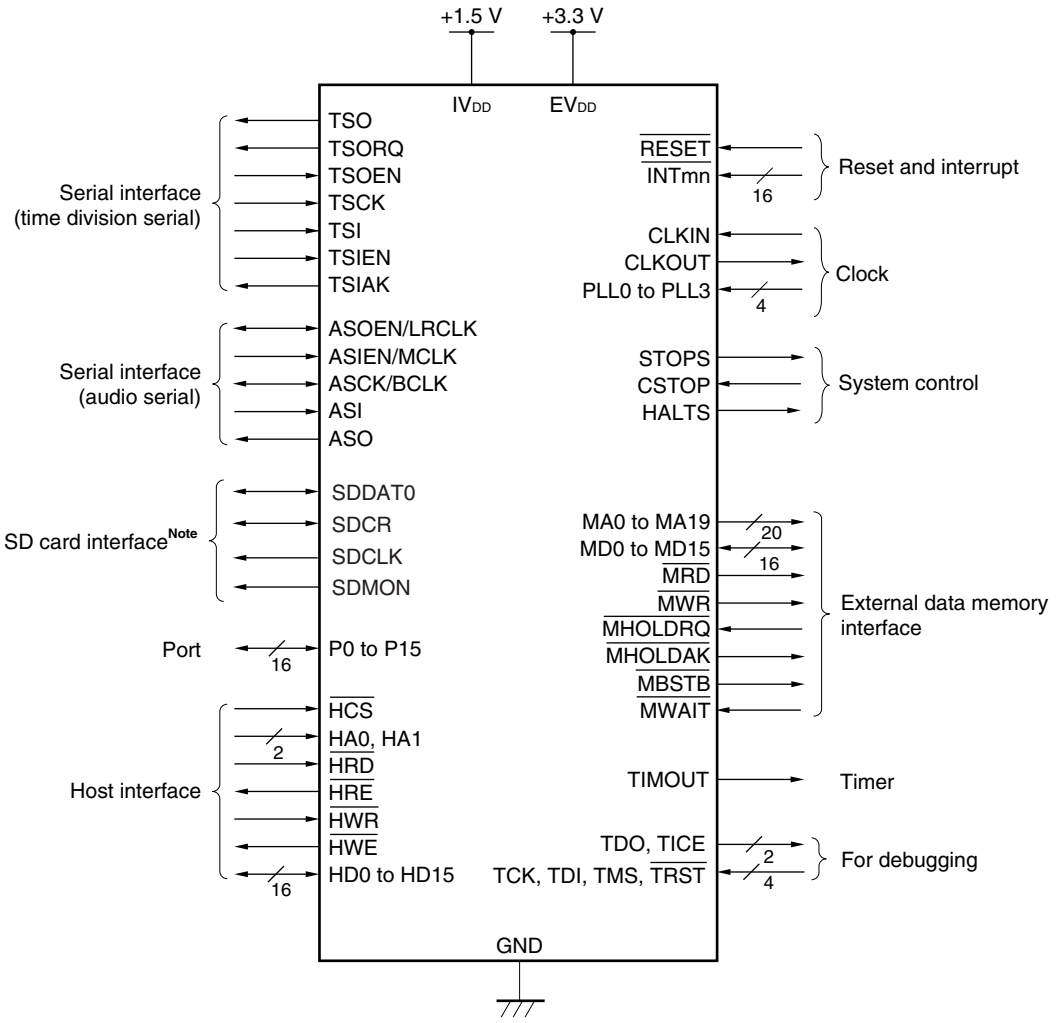
Parts Number	Package
μPD77210F1-DA2	161-pin plastic fine pitch BGA (10 x 10)
μPD77210GJ-8EN	144-pin plastic LQFP (fine pitch) (20 x 20)
μPD77213F1-xxx-DA2	161-pin plastic fine pitch BGA (10 x 10)
μPD77213GJ-xxx-8EN	144-pin plastic LQFP (fine pitch) (20 x 20)

Remark xxx indicates ROM code suffix.

BLOCK DIAGRAM



FUNCTIONAL PIN BLOCK



Note μPD77213 only

Caution Some port pins, host interface pins, serial interface pins, interrupt pins, and SD card interface pins are alternate function pins.

Remark m, n = 0 to 3

DSP FUNCTION LIST

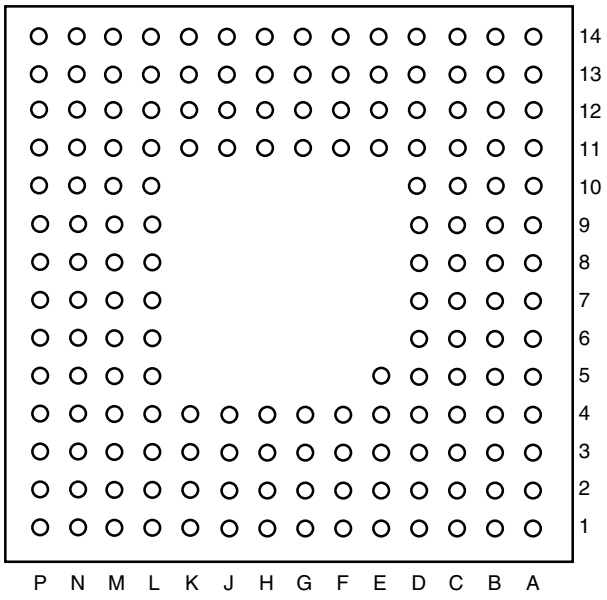
Item		μPD77110	μPD77111	μPD77112	μPD77113A	μPD77114	μPD77115	μPD77210	μPD77213
Memory space (words × bits)	Int. instruction RAM	35.5 K × 32	1 K × 32		3.5 K × 32		11.5 K × 32	31.5 K × 32	15.5 K × 32
	Int. instruction ROM	None	31.75 K × 32		48 K × 32		None		64K × 32
	Data RAM (X/Y memory)	24 K × 16 each	3 K × 16 each		16 K × 16 each		16 K × 16 each	30 K × 16 each	18 K × 16 each
	Data ROM (X/Y memory)	None	16 K × 16 each		32 K × 16 each		None		32 K × 16 each
	Ext. instruction memory	None							
	Ext. data memory (X/Y memory)	32 K × 16 each	None	16 K × 16 each	None	8 K × 16 each	None	1 M × 16	1 M × 16 (8 K × 16, using SD I/F)
Instruction cycle (at maximum operating speed)		15.3 ns (65 MHz)	13.3 ns (75 MHz)					6.25 ns (160 MHz)	8.33 ns (120 MHz)
Multiple		Integer multiple of ×1 to 8 (external pin)	Integer multiple of ×1 to 16 (mask option)				Integer multiple of ×1 to 16 (external pin)	Integer multiple of ×10 to 64 (external pin)	
Peripheral	Serial interface	2 channels (speech CODEC)					1 channel (audio CODEC)	2 channels (time-division, audio)	
	Host interface	8-bit bus					16-bit bus		
	General-purpose port (I/O programmable)	4 bits					8 bits	16 bits (some are alternative with host)	
	Timer	None					1 channel (16-bit resolution)	2 channels (16-bit resolution)	
	Others	–	–	–	–	–	SD card I/F	–	SD card I/F
Supply voltage		DSP core: 2.5 V I/O pins: 3 V						DSP core: 1.5 V I/O pins: 3.3 V	
Package		100-pin TQFP	80-pin TQFP 80-pin FBGA	100-pin TQFP	80-pin FBGA	100-pin TQFP	80-pin TQFP 80-pin FBGA	161-pin FBGA 144-pin LQFP	

PIN CONFIGURATIONS

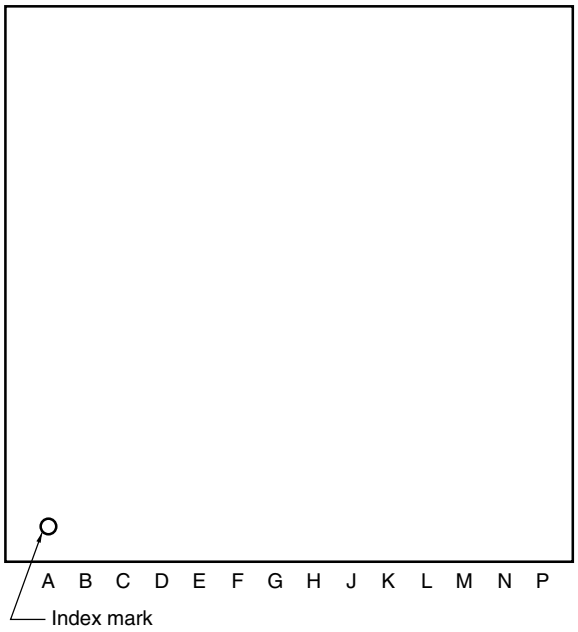
161-pin plastic fine pitch BGA (10 x 10)

- **μPD77210F1-DA2**
- **μPD77213F1-xxx-DA2**

(Bottom View)



(Top View)



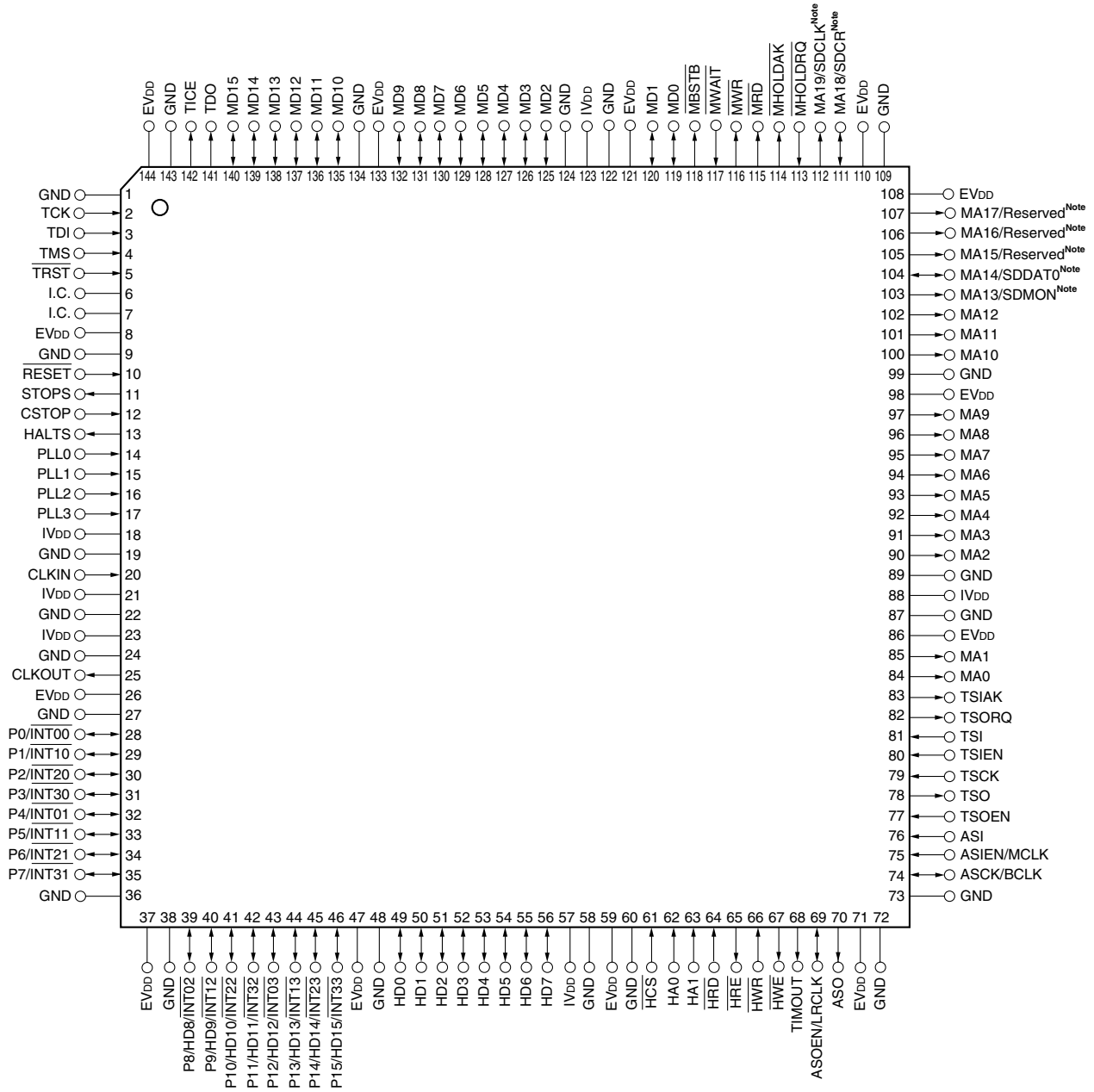
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A1	NC	C14	EV_{DD}	H2	HD7	M5	TSORQ
A2	NC	D1	P10/HD10/$\overline{INT22}$	H3	HD6	M6	MA0
A3	P5/$\overline{INT11}$	D2	P11/HD11/$\overline{INT32}$	H4	GND	M7	MA4
A4	P2/$\overline{INT20}$	D3	P12/HD12/$\overline{INT03}$	H11	MD5	M8	MA5
A5	GND	D4	GND	H12	MD4	M9	MA10
A6	EV_{DD}	D5	GND	H13	MD1	M10	MA12
A7	IV_{DD}	D6	P1/$\overline{INT10}$	H14	MD3	M11	MA15/Reserved[Note]
A8	IV_{DD}	D7	GND	J1	EV_{DD}	M12	MA19/SDCLK[Note]
A9	PLL0	D8	GND	J2	$\overline{HCS}$	M13	MA18/SDCR[Note]
A10	STOPS	D9	GND	J3	HA1	M14	EV_{DD}
A11	EV_{DD}	D10	GND	J4	$\overline{HWR}$	N1	NC
A12	$\overline{TRST}$	D11	TMS	J11	GND	N2	NC
A13	NC	D12	TICE	J12	MD0	N3	ASIEN/MCLK
A14	NC	D13	MD12	J13	$\overline{MBSTB}$	N4	TSCK
B1	NC	D14	MD15	J14	IV_{DD}	N5	TSIAK
B2	NC	E1	P14/HD14/$\overline{INT23}$	K1	HA0	N6	MA1
B3	P7/$\overline{INT31}$	E2	P15/HD15/$\overline{INT33}$	K2	$\overline{HRD}$	N7	MA2
B4	P6/$\overline{INT21}$	E3	P13/HD13/$\overline{INT13}$	K3	TIMOUT	N8	MA7
B5	P3/$\overline{INT30}$	E4	GND	K4	ASO	N9	MA9
B6	CLKOUT	E5	NC	K11	GND	N10	MA11
B7	IV_{DD}	E11	GND	K12	$\overline{MWR}$	N11	MA16/Reserved[Note]
B8	PLL3	E12	MD14	K13	$\overline{MWAIT}$	N12	MA17/Reserved[Note]
B9	PLL1	E13	MD9	K14	EV_{DD}	N13	NC
B10	CSTOP	E14	MD11	L1	$\overline{HWE}$	N14	NC
B11	I.C.	F1	EV_{DD}	L2	$\overline{HRE}$	P1	NC
B12	TCK	F2	HD1	L3	GND	P2	NC
B13	NC	F3	HD2	L4	GND	P3	ASI
B14	NC	F4	HD0	L5	TSIEN	P4	TSO
C1	EV_{DD}	F11	MD10	L6	GND	P5	TSI
C2	P8/HD8/$\overline{INT02}$	F12	MD13	L7	GND	P6	EV_{DD}
C3	P9/HD9/$\overline{INT12}$	F13	MD7	L8	MA8	P7	IV_{DD}
C4	P4/$\overline{INT01}$	F14	EV_{DD}	L9	GND	P8	MA3
C5	P0/$\overline{INT00}$	G1	HD3	L10	MA14/SDDAT0[Note]	P9	MA6
C6	CLKIN	G2	HD5	L11	GND	P10	EV_{DD}
C7	PLL2	G3	HD4	L12	$\overline{MHOLDRQ}$	P11	MA13/SDMON[Note]
C8	HALTS	G4	GND	L13	$\overline{MRD}$	P12	EV_{DD}
C9	$\overline{RESET}$	G11	GND	L14	$\overline{MHOLDAK}$	P13	NC
C10	I.C.	G12	MD8	M1	EV_{DD}	P14	NC
C11	TDI	G13	MD2	M2	ASCK/BCLK		
C12	TDO	G14	MD6	M3	ASOEN/LRCLK		
C13	GND	H1	IV_{DD}	M4	TSOEN		

Note MA13 to MA19 pins of the μPD77213 are alternate function pins.

144-pin plastic LQFP (fine pitch) (20 x 20) (Top View)

•μPD77210GJ-8EN

•μPD77213GJ-xxx-8EN



Note MA13 to MA19 pins of the μPD77213 are alternate function pins.

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	GND	37	EV_{DD}	73	GND	109	GND
2	TCK	38	GND	74	ASCK/BCLK	110	EV_{DD}
3	TDI	39	P8/HD8/$\overline{INT02}$	75	ASIEN/MCLK	111	MA18/SDCR[Note]
4	TMS	40	P9/HD9/$\overline{INT12}$	76	ASI	112	MA19/SDCLK[Note]
5	$\overline{TRST}$	41	P10/HD10/$\overline{INT22}$	77	TSOEN	113	$\overline{MHOLDRQ}$
6	I.C.	42	P11/HD11/$\overline{INT32}$	78	TSO	114	$\overline{MHOLDAK}$
7	I.C.	43	P12/HD12/$\overline{INT03}$	79	TSCK	115	$\overline{MRD}$
8	EV_{DD}	44	P13/HD13/$\overline{INT13}$	80	TSIEN	116	$\overline{MWR}$
9	GND	45	P14/HD14/$\overline{INT23}$	81	TSI	117	$\overline{MWAIT}$
10	$\overline{RESET}$	46	P15/HD15/$\overline{INT33}$	82	TSORQ	118	$\overline{MBSTB}$
11	STOPS	47	EV_{DD}	83	TSIAK	119	MD0
12	CSTOP	48	GND	84	MA0	120	MD1
13	HALTS	49	HD0	85	MA1	121	EV_{DD}
14	PLL0	50	HD1	86	EV_{DD}	122	GND
15	PLL1	51	HD2	87	GND	123	IV_{DD}
16	PLL2	52	HD3	88	IV_{DD}	124	GND
17	PLL3	53	HD4	89	GND	125	MD2
18	IV_{DD}	54	HD5	90	MA2	126	MD3
19	GND	55	HD6	91	MA3	127	MD4
20	CLKIN	56	HD7	92	MA4	128	MD5
21	IV_{DD}	57	IV_{DD}	93	MA5	129	MD6
22	GND	58	GND	94	MA6	130	MD7
23	IV_{DD}	59	EV_{DD}	95	MA7	131	MD8
24	GND	60	GND	96	MA8	132	MD9
25	CLKOUT	61	$\overline{HCS}$	97	MA9	133	EV_{DD}
26	EV_{DD}	62	HA0	98	EV_{DD}	134	GND
27	GND	63	HA1	99	GND	135	MD10
28	P0/$\overline{INT00}$	64	$\overline{HRD}$	100	MA10	136	MD11
29	P1/$\overline{INT10}$	65	$\overline{HRE}$	101	MA11	137	MD12
30	P2/$\overline{INT20}$	66	$\overline{HWR}$	102	MA12	138	MD13
31	P3/$\overline{INT30}$	67	$\overline{HWE}$	103	MA13/SDMON[Note]	139	MD14
32	P4/$\overline{INT01}$	68	TIMOUT	104	MA14/SDDAT0[Note]	140	MD15
33	P5/$\overline{INT11}$	69	ASOEN/LRCLK	105	MA15/Reserved[Note]	141	TDO
34	P6/$\overline{INT21}$	70	ASO	106	MA16/Reserved[Note]	142	TICE
35	P7/$\overline{INT31}$	71	EV_{DD}	107	MA17/Reserved[Note]	143	GND
36	GND	72	GND	108	EV_{DD}	144	EV_{DD}

Note MA13 to MA19 pins of the μPD77213 are alternate function pins.

Pin Name

ASCK :Audio Serial Clock Input/Output
ASI :Audio Serial Data Input
ASIEN :Audio Serial Input Enable
ASO :Audio Serial Data Output
ASOEN :Audio Serial Output Enable
BCLK :Bit Clock Input/Output
CLKIN :Clock Input
CLKOUT :Clock Output
CSTOP :Clear Stop Mode
EV_{DD} :Power Supply for I/O Pins
GND :Ground
HALTS :Halt Status Signal Output
HD0 to HD15 :Host Data Bus
$\overline{HCS}$:Host Chip Select
HA0, HA1 :Host Data Access
$\overline{HRD}$:Host Read
$\overline{HRE}$:Host Read Enable
$\overline{HWE}$:Host Write Enable
$\overline{HWR}$:Host Write
I.C. :Internal Connection
IV_{DD} :Power Supply for DSP Core
$\overline{INTmn}$:Interrupt (m,n=0 to 3)
LRCLK :Left Right Clock Input/Output
MA0 to MA19 :External Data Memory Address Bus
$\overline{MBSTB}$:External Data Memory Bus Strobe
MCLK :Master Clock Input
MD0 to MD15 :External Data Memory Bus
$\overline{MHOLDAK}$:External Data Memory Bus Hold Acknowledge
$\overline{MHOLDRQ}$:External Data Memory Bus Hold Request
$\overline{MRD}$:External Data Memory Read Output
$\overline{MWR}$:External Data Memory Write Output
$\overline{MWAIT}$:External Data Memory Access Wait Input
NC :Non-Connection
P0 to P15 :Port
PLL0-PLL3 :PLL Multiple Rate Set
Reserved :Reserved
$\overline{RESET}$:Reset
SDCLK :SD Card Clock Output
SDCR :SD Card Command Output/Response Input
SDDAT0 :SD Card Data Input/Output
SDMON :SD Card Access Monitor
STOPS :Stop Status Signal Output
TCK :Test Clock Input
TDI :Test Data Input
TDO :Test Data Output
TICE :Test In-Circuit Emulator
TIMOUT :Timer Time Out Monitor Output
$\overline{TMS}$:Test Mode Select
$\overline{TRST}$:Test Reset
TSCK :Time Division Multiplex Serial Clock Input
TSI :Time Division Multiplex Serial Data Input
TSIAK :Time Division Multiplex Serial Input Acknowledge
TSIEN :Time Division Multiplex Serial Input Enable
TSO :Time Division Multiplex Serial Data Output
TSOEN :Time Division Multiplex Serial Output Enable
TSORQ :Time Division Multiplex Serial Output Request

CONTENTS

1. PIN FUNCTIONS

Because the pin numbers differ depending on the package, see the column for the package to be used in the tables below.

1.1 Description of Pin Functions

• Power supply pins

Pin Name	Pin No.		I/O	Function	Alternate Pin
	144-pin LQFP	161-pin FBGA			
IV_{DD}	18,21,23,57, 88,123	A7,A8,B7,H1, J14, P7	–	Power supply for DSP core (+1.5 V) These pins supply power to the DSP core.	–
EV_{DD}	8,26,37,47,59, 71,86,98,108, 110,121,133, 144	A6,A11,C1, C14,F1,F14, J1,K14,M1, M14,P6,P10, P12	–	Power supply for I/O (+3.3 V) These pins supply power to the external interface pins.	–
GND	1,9,19,22,24, 27,36,38,48, 58,60,72,73, 87,89,99,109, 122,124,134, 143	A5,C13,D4,D5, D7,D8,D9,D10, E4,E11,G4, G11,H4,J11, K11,L3,L4,L6, L7,L9,L11	–	Ground These are ground pins.	–

Remark Please supply voltage to the IV_{DD} and EV_{DD} pins simultaneously.

• **Clock and system control pins**

Pin Name	Pin No.		I/O	Function	Alternate Pin
	144-pin LQFP	161-pin FBGA			
CLKIN	20	C6	Input	Clock input This pin inputs a clock to operate the μPD77210 Family.	–
CLKOUT	25	B6	Output	Internal system clock output This pin outputs the internal system clock that is the clock input from CLKIN and which is multiplied by the PLL circuit.	–
PLL0 to PLL3	14 to 17	A9,B9,C7,B8	Input	PLL multiple setting input These pins set a clock multiple of the PLL circuit. • PLL3: PLL2: PLL1: PLL0 0000: x10 0001: x12 0010: x14 0011: x16 0100: x18 0101: x20 0110: x22 0111: x24 1000: x26 1001: x28 1010: x30 1011: x32 1100: x40 1101: x48 1110: x56 1111: x64	–
HALTS	13	C8	Output	HALT mode status output This pin is asserted active in halt mode and stop mode.	–
STOPS	11	A10	Output	Stop mode status output This pin is asserted active in stop mode.	–
CSTOP	12	B10	Input	Stop mode clear signal input Stop mode is cleared when this pin is asserted active.	–

• **Reset and interrupt pins**

Pin Name	Pin No.		I/O	Function	Alternate Pin
	144-pin LQFP	161-pin FBGA			
$\overline{\text{RESET}}$	10	C9	Input	Internal system reset signal input This pin initializes the μPD77210 Family.	–
$\overline{\text{INT00}}$	28	C5	Input	Maskable external interrupt input These pins input external interrupts.	P0
$\overline{\text{INT01}}$	32	C4	Input		P4
$\overline{\text{INT02}}$	39	C2	Input		P8/HD8
$\overline{\text{INT03}}$	43	D3	Input		P12/HD12
$\overline{\text{INT10}}$	29	D6	Input		P1
$\overline{\text{INT11}}$	33	A3	Input		P5
$\overline{\text{INT12}}$	40	C3	Input		P9/HD9
$\overline{\text{INT13}}$	44	E3	Input		P13/HD13
$\overline{\text{INT20}}$	30	A4	Input		P2
$\overline{\text{INT21}}$	34	B4	Input		P6
$\overline{\text{INT22}}$	41	D1	Input		P10/HD10
$\overline{\text{INT23}}$	45	E1	Input		P14/HD14
$\overline{\text{INT30}}$	31	B5	Input		P3
$\overline{\text{INT31}}$	35	B3	Input		P7
$\overline{\text{INT32}}$	42	D2	Input		P11/HD11
$\overline{\text{INT33}}$	46	E2	Input		P15/HD15

• **External data memory interface**

Pin Name	Pin No.		I/O	Function	Alternate Pin
	144-pin LQFP	161-pin FBGA			
MA0 to MA19[Note]	84, 85, 90 to 97, 100 to 107, 111, 112	M6,N6,N7,P8, M7,M8,P9,N8, L8,N9,M9,N10, M10,P11,L10, M11,N11,N12, M13,M12	Output (3S)	Address bus of external data memory These pins output an address when the external data memory is accessed.	SDCLK, SDCR, SDDAT0, SDMON
MD0 to MD15	119,120, 125 to 132, 135 to 140	J12,H13,G13, H14,H12,H11, G14,F13,G12, E13,F11,E14, D13,F12,E12, D14	I/O (3S)	16-bit data bus These pins input/output data when the external data memory is accessed.	–
$\overline{\text{MWR}}$	116	K12	Output (3S)	Write output This pin outputs a write strobe signal for the external data memory.	–
$\overline{\text{MRD}}$	115	L13	Output (3S)	Read output This pin outputs a read strobe signal for the external data memory.	–
$\overline{\text{MHOLDAK}}$	114	L14	Output	Hold acknowledge signal This pin goes low when the external device is granted use of the external data memory bus of the μPD77210 Family.	–
$\overline{\text{MHOLDRQ}}$	113	L12	Input	Hold request signal The external device inputs a low level to this pin when it uses the external data memory bus of the μPD77210 Family.	–
$\overline{\text{MWAIT}}$	117	K13	Input	Wait signal input This pin inserts wait cycles when the μPD77210 Family accesses the external data memory. • 0: Inserts wait cycles. • 1: Does not insert wait cycles.	–
$\overline{\text{MBSTB}}$	118	J13	Output	Bus strobe signal This pin goes low while the μPD77210 Family uses the external data memory bus.	–

Note MA13 to MA19 pins of the μPD77213 are alternate function pins.

Remark Those pins marked "3S" in the above table enter the high-impedance state under the following conditions:

MA0 to MA19, $\overline{\text{MRD}}$, and $\overline{\text{MWR}}$: When the bus is released ($\overline{\text{MHOLDAK}}$ = low level)

MD0 to MD15: When the external data memory is not accessed and when the bus is released ($\overline{\text{MHOLDAK}}$ = low level)

• **Timer**

Pin Name	Pin No.		I/O	Function	Alternate Pin
	144-pin LQFP	161-pin FBGA			
TIMOUT	68	K3	Output	Time out monitor This pin is asserted active when the timer times out.	–

• **Serial interface**

Pin Name	Pin No.		I/O	Function	Alternate Pin
	144-pin LQFP	161-pin FBGA			
ASCK/ BCLK	74	M2	I/O	Audio serial clock input/output ASCK:Audio serial clock input BCLK:Serial clock I/O	–
ASO	70	K4	Output (3S)	Audio serial data output	–
ASI	76	P3	Input	Audio serial data input	–
ASOEN/ LRCLK	69	M3	I/O	Audio serial output enable/left right clock input output ASOEN:Audio serial output enable input LRCLK:Left right clock I/O	–
ASIEN/ MCLK	75	N3	Input	Audio serial input enable/master clock input output ASIEN:Audio serial input enable input MCLK:Master clock input (in master mode)	–
TSCK	79	N4	Input	Clock input for time division serial	–
TSO	78	P4	Output (3S)	Time-division serial data output	–
TSI	81	P5	Input	Time-division serial data input	–
TSORQ	82	M5	Output	Time-division serial output request	–
TSOEN	77	M4	Input	Time-division serial output enable	–
TSIEN	80	L5	Input	Time-division serial input enable	–
TSIAK	83	N5	Output	Time-division serial input acknowledge	–

Remark Those pins marked “3S” in the above table enter the high-impedance state when data transmission is completed and when the hardware reset ($\overline{\text{RESET}}$) signal is input.

• **Host interface**

Pin Name	Pin No.		I/O	Function	Alternate Pin
	144-pin LQFP	161-pin FBGA			
HA1	63	J3	Input	Host address 1 This pin specifies a register that is accessed by the host interface pins (HD7 to HD0, or HD15 to HD0). • 1: The host interface status register (HST) is accessed. • 0: The host transmit data register (HDT (out)) is accessed for read ($\overline{HRD}$ = 0) and the host receive data register (HDT (in)) is accessed for write ($\overline{HWR}$ = 0).	–
HA0	62	K1	Input	Host address 0 This pin specifies a register that is accessed by HD7 to HD0 in 8-bit mode. This pin is invalid in 16-bit mode. • 1: Bits 15 to 8 of HST, HDT (in), and HDT (out) are accessed. • 0: Bits 7 to 0 of HST, HDT (in), and HDT (out) are accessed.	–
$\overline{HCS}$	61	J2	Input	Chip select input	–
$\overline{HRD}$	64	K2	Input	Host read input	–
$\overline{HWR}$	66	J4	Input	Host write input	–
$\overline{HRE}$	65	L2	Output	Host read enable output	–
$\overline{HWE}$	67	L1	Output	Host write enable output	–
HD0 to HD7	49 to 56	F4,F2,F3,G1, G3,G2,H3,H2	I/O (3S)	8-bit host data bus These pins constitute a host data bus in 8-bit host mode. Access to 16-bit data for input/output is controlled by the HA0 pin, and the data is accessed two times such that it is divided into two blocks of 8-bit data. In 16-bit mode, the lower 8 bits of the data are input/output.	–
HD8 to HD15	39 to 46	C2,C3,D1,D2, D3,E3,E1,E2	I/O (3S)	Host data bus These pins constitute a host data bus in 16-bit host mode. They input/output 16-bit data with HD0 to HD7.	P8 to P15/ $\overline{INT02}$, $\overline{INT12}$, $\overline{INT22}$, $\overline{INT32}$, $\overline{INT03}$, $\overline{INT13}$, $\overline{INT23}$, $\overline{INT33}$

Remark Those pins marked “3S” in the above table enter the high-impedance state while the host interface is not being accessed.

• **I/O port**

Pin Name	Pin No.		I/O	Function	Alternate Pin
	144-pin LQFP	161-pin FBGA			
P0	28	C5	I/O	General-purpose I/O port	$\overline{\text{INT00}}$
P1	29	D6	I/O		$\overline{\text{INT10}}$
P2	30	A4	I/O		$\overline{\text{INT20}}$
P3	31	B5	I/O		$\overline{\text{INT30}}$
P4	32	C4	I/O		$\overline{\text{INT01}}$
P5	33	A3	I/O		$\overline{\text{INT11}}$
P6	34	B4	I/O		$\overline{\text{INT21}}$
P7	35	B3	I/O		$\overline{\text{INT31}}$
P8	39	C2	I/O		$\overline{\text{INT02}}$/HD8
P9	40	C3	I/O		$\overline{\text{INT12}}$/HD9
P10	41	D1	I/O		$\overline{\text{INT22}}$/HD10
P11	42	D2	I/O		$\overline{\text{INT32}}$/HD11
P12	43	D3	I/O		$\overline{\text{INT03}}$/HD12
P13	44	E3	I/O		$\overline{\text{INT13}}$/HD13
P14	45	E1	I/O		$\overline{\text{INT23}}$/HD14
P15	46	E2	I/O		$\overline{\text{INT33}}$/HD15

• **Debugging interface**

Pin Name	Pin No.		I/O	Function	Alternate Pin
	144-pin LQFP	161-pin FBGA			
TDO	141	C12	Output (3S)	For debugging This interface pins are used when a debugger is used.	–
TICE	142	D12	Output		–
TCK	2	B12	Input		–
TDI	3	C11	Input		–
TMS	4	D11	Input		–
$\overline{\text{TRST}}$	5	A12	Input		–

Remark Those pins marked “3S” in the above table enter the high-impedance state while the debugging interface is not being accessed.

•SD card interface (μPD77213 only)

Pin Name	Pin No.		I/O	Function	Alternate Pin
	144-pin LQFP	161-pin FBGA			
SDCLK	112	M12	Output	SD card clock output • Leave this pin open.	MA19
SDCR	111	M13	I/O (3S)	SD cord command/response Input: Response Output: Command • Leave pull-up.	MA18
SDDAT0	104	L10	I/O (3S)	SD card data input/output Input: Read data Output: Write data • Leave pull-up.	MA14
SDMON	103	P11	Output	SD card interface access monitor This pin outputs a high level when the SD card interface is being accessed. 1: SD card interface being accessed 0: SD card interface not being accessed	MA13
Reserved	105 to 107	M11, N11, N12	–	Reserved for future function expansion. This pin becomes high impedance when the SD card interface is being used.	MA15 to MA17

Remark Those pins marked “3S” in the above table enter the high-impedance state when the SD card interface is not being accessed.

• Others

Pin Name	Pin No.		I/O	Function	Alternate Pin
	144-pin LQFP	161-pin FBGA			
I.C.	6, 7	B11, C10	–	Internally connected. Leave these pins open.	–
NC	–	A1,A2,A13, A14,B1,B2, B13,B14,E5, N1,N2,N13, N14,P1,P2, P13,P14	–	No connection. Leave these pins open.	–

Caution If any signal is input to these pins or if these pins are read, the correct operation of the μPD77210 Family is not guaranteed.

1.2 Connection of Unused Pins

1.2.1 Connection of functional pins

Connect the unused pins as shown in the table below.

Pin Name	I/O	Recommended Connection
STOPS, HALTS	Output	Leave open.
CSTOP	Input	Connect to GND via a pull-down resistor.
CLKOUT	Output	Leave open.
P0 to P15	I/O	Connect to EV_{DD} via a pull-up resistor or to GND via a pull-down resistor.
HD0 to HD7[Note 1]	I/O	Connect to EV_{DD} via a pull-up resistor or to GND via a pull-down resistor.
HA0, HA1	Input	Connect to EV_{DD} via a pull-up resistor or to GND via a pull-down resistor.
$\overline{HCS}$, $\overline{HRD}$, $\overline{HWR}$	Input	Connect to EV_{DD} via a pull-up resistor.
$\overline{HRE}$, $\overline{HWE}$	Output	Leave open.
TIMOUT	Output	Leave open.
ASCK, TSCK	Input	Connect to EV_{DD} via a pull-up resistor or to GND via a pull-down resistor.
ASI, TSI	Input	
ASIEN, TSIEN	Input	Connect to GND via a pull-down resistor.
ASOEN, TSOEN, LRCLK	Input	
ASO, TSO	Output	Leave open.
TSORQ	Output	
TSIAK	Output	
MA0 to MA19	Output	Leave open.
MD0 to MD15[Note 2]	I/O	Connect to EV_{DD} via a pull-up resistor or to GND via a pull-down resistor.
$\overline{MRD}$, $\overline{MWR}$	Output	Leave open.
$\overline{MHOLDRQ}$	Input	Connect to EV_{DD} via a pull-up resistor.
$\overline{MBSTB}$, $\overline{MHOLDAK}$	Output	Leave open.
$\overline{MWAIT}$	Input	Connect to EV_{DD} via a pull-up resistor.
TCK	Input	Connect to GND via a pull-down resistor.
TDO, TICE	Output	Leave open.
TMS, TDI	Input	Leave open (this pin is internally pulled up).
$\overline{TRST}$	Input	Leave open (this pin is internally pulled down).

Notes 1. These pins may left opened if the $\overline{HCS}$, $\overline{HRD}$,and $\overline{HWR}$ are fixed to the high level. However, connect these pins as recommended in the HALT and STOP modes when the power consumption must be lowered.

2. These pins may leave opened if the external data memory is not accessed in the program. However, connect these pins as recommended in the HALT and STOP modes when the power consumption must be lowered.

Caution Unused alternate-function pins should be handled in accordance with the processing specified for the pin function of the initial setting.

1.2.2 Connection of non-functional pin

Pin name	I/O	Recommended Connection
I.C.	–	Leave open.
NC	–	Leave open.

2. FUNCTIONAL OUTLINE

2.1 Program Control Unit

This unit controls the execution of μPD77210 Family by executing instructions and controlling branching, loop, interrupts, clock, and standby mode.

2.1.1 CPU control

A three-stage pipeline architecture is employed so that all instructions, except branch instructions and some others, can be executed with one system clock.

2.1.2 Interrupt control

The interrupt control circuit services the interrupt requests input to the interrupt controller by an external pin ($\overline{\text{INTmn}}$) or internal peripherals (such as the serial interface, host interface, timer, and DMA controller). The interrupt of each interrupt source can be individually enabled or disabled. In addition, multiple interrupts are also supported.

2.1.3 Loop control stack

A loop function without any hardware overhead is realized. A 4-level loop stack is provided to support multiple loops.

2.1.4 PC stack

A 15-level PC stack that stacks the program counter supports multiple interrupts/subroutine calls.

2.1.5 Clock control

A PLL and a divider are internally provided as a clock generator so that an externally input clock is multiplied or divided and supplied as the operating clock to the μPD77210 Family. The multiple of the PLL can be set by using external pins (PLL0 to PLL3) within a range of ×10 to 64. The division ratio can be set by using a register in a range of ÷1 to 16.

The clock control register (CLKC) controls the power (ON/OFF) to the PLL, selects a clock source, controls the output divider, and controls the output of the CLKOUT pin.

Two types of standby modes are available so that the power consumption can be reduced when the μPD77210 Family is standing by.

- HALT mode: Current consumption falls to several mA upon execution of the HALT instruction.
  This mode is released by an interrupt or hardware reset.
- STOP mode: Current consumption falls to hundreds of μA[Note] upon execution of the STOP instruction.
  This mode is released by hardware reset or inputting a signal to CSTOP pin.

Note When the PLL is stopped

2.1.6 Instruction memory

Of the instruction RAM, 64 words are allocated as interrupt vectors.

The μPD77210 is provided with an instruction RAM of 31.5 Kwords. The μPD77213 is provided with an instruction RAM of 15.5 Kwords and instruction ROM of 64 Kwords.

A boot-up ROM that boots up the instruction RAM is also provided, and the instruction RAM can be initialized or rewritten by means of a memory boot (booting from an internal or external data space), host boot (booting via a host interface), or serial boot (booting via a serial interface).

2.2 Operation Unit

This unit performs multiplication, addition, logic, and shift operations, and consists of a 40-bit multiply accumulator, a 40-bit data ALU, a 40-bit barrel shifter, and eight 40-bit general-purpose registers.

2.2.1 General-purpose registers (R0 to R7)

These eight 40-bit registers input/output operands and load/store data to/from data memory.

Each register consists of three parts: R0L to R7L (bits 15 to 0), R0H to R7H (bits 31 to 16), and R0E to R7E (bits 39 to 32). Depending on the type of the operation, RnL, RnH, and RnE are used either as one register or in combination.

2.2.2 Multiply accumulator (MAC)

The multiply accumulator performs multiplication of two 16-bit data items and addition or subtraction between the result of the multiplication and one 40-bit data item, and then outputs 40-bit data.

A shifter (MSFT: MAC shifter) is provided at the preceding stage of the MAC, so that the 40-bit data that is to be added to or subtracted from the multiplication result can be arithmetically shifted 1 bit or 16 bits to the right before addition or subtraction.

2.2.3 Arithmetic logic unit (ALU)

The ALU accepts one or two 40-bit data items as input, performs an arithmetic or logical operation, and then outputs 40-bit data.

2.2.4 Barrel shifter (BSFT)

The BFST accepts 40-bit data items as input, shifts the data to the left or right by an arbitrary number of bits, and then outputs 40-bit data. The data can be shifted to the right arithmetically, in which case the sign of the data is extended, or logically in which case 0 is inserted starting from the MSB.

2.3 Data Memory Unit

The data memory unit consists of two planes of data memory spaces and two pairs of data addressing units.

2.3.1 Data memory

Two data memory planes (X data memory and Y data memory) are provided. The data memory space includes a 64-word peripheral area.

The μPD77210 has a data RAM consisting of 30 Kwords × 2 planes. The μPD77213 has a data RAM consisting of 18 Kwords × 2 planes, and has a data ROM consisting of 32 Kwords × 2 planes.

In addition, They also have an external data memory interface that is used to connect an external 1 Mword data memory to the device.

2.3.2 Data addressing unit

An independent data addressing unit is provided for each of the X and Y data memory spaces.

Each data addressing unit has four data pointers (DPn), four index registers (DNn), one module register (DMX or DMY), and an address ALU.

2.4 Peripheral Unit

The peripheral unit has serial interfaces, a host interface, general-purpose I/O ports, timers, an external memory interface, and SD card interface (μPD77213 only). All these internal peripherals are mapped to the X and Y data memory spaces and are accessed as memory-mapped I/Os by the program.

2.4.1 Serial interface (SIO)

Two serial interface channels, an audio serial interface (ASIO) and a time-division serial interface (TDMSIO), are provided.

The audio serial interface can be used in either of two modes: audio mode and standard mode. The standard mode is compatible with the existing μPD77111 Family. The audio mode is compatible with the μPD77115.

The features of the audio mode are as follows:

- Mode: Master mode and slave mode
  Master mode: Supports master clock input (MCLK), bit clock output (BCLK), LR clock output (LRCLK), 256 fs, 384 fs, and 512 fs.
  Slave mode: Bit clock input (BCLK) and LR clock input (LRCLK)
- Frame format: 32- or 64-bit audio formats (LRCLK format)
- Handshake: Handshaking with external devices by a dedicated frame signal (LRCLK) and with the internal circuitry by polling, wait, or interrupt

The standard mode has the following features:

- Serial clock: Supplied from an external source to each channel. The clock is shared for input and output by each channel.
- Frame length: 8 or 16 bits, with MSB or LSB first selected for each channel.
- Handshake: Handshaking with the external device by using a dedicated status signal and with the internal circuitry by polling, wait, or interrupt.

The time-division serial interface divides the serial input/output signal into 1 to 32 time slots and allows several devices to share the serial bus. Because the T1 and E1 frame signals are considered. The time slot can be extended from 1 to 128.

2.4.2 Host interface (HIO)

This is a parallel port that inputs/outputs data from/to an external host CPU and DMA controller. It can be used in either 8-bit parallel mode or 16-bit parallel mode. In the μPD77210 Family, 16-bit registers are mapped to memory for input data, output data, and status. Handshaking with an external device is performed by using a dedicated status signal, and the internal circuitry handshaking is done by means of polling, wait, or interrupts.

The 8-bit parallel mode is compatible with the existing members of the μPD77111 Family.

In 16-bit parallel mode, some port pins are used as host interface pins.

2.4.3 General-purpose I/O port (PIO)

This is a 16-bit I/O port that can be set to either input or output mode in 1-bit units.

The external pins alternate between interrupt pins and host interface pins. By setting the mode of 8 bits of the port to host interface pin mode, the host interface can be set in the 16-bit parallel mode.

2.4.4 External memory interface (MIO)

This interface accesses an external 1 Mwords data memory area in either of two modes: direct access and DMA access modes. In DMA access mode, access is made via a memory-mapped register.

In direct access mode, the data paging register (DPR) is set to 0x3F and a page area is accessed as an access window. An address of the external memory consists of 20 bits with the 8-bit value of the index register added as bits 12 to 19.

In DMA access mode, the address is automatically updated when a memory-mapped register is accessed. The address is updated in an increment addressing mode in which the address is simply incremented, or in two-dimensional addressing mode in which an offset is added to each line length.

The number of wait cycles to be inserted when the external memory is accessed can be specified by a register (MWAIT), within a range of 1 to 15. In addition, wait cycles can also be inserted by using the $\overline{\text{MWAIT}}$ pin.

2.4.5 Timers (TIM1 and TIM2)

The μPD77210 Family has two timer channels.

These timers can be used as interval timers, event counters, watchdog timers, and free-run timers.

The clock input to the timers is selected from the system clock, serial clock (ASCK or TSCK), external interrupt ($\overline{\text{INT00}}$, $\overline{\text{INT10}}$, $\overline{\text{INT20}}$, or $\overline{\text{INT30}}$), or output of each timer.

The count value is 16 bits and the clock input by the prescaler can be divided by 1, 2, 4, 8, 16, 32, 64, or 128.

2.4.6 Interrupt controller (INTC)

The interrupt controller has functions for selecting and masking interrupt signals. It controls the interrupt signal to be input to the DSP core.

2.4.7 DMA controller (PMT)

The DMA controller realizes data transfer between the peripherals and memory (peripheral-memory transfer) in the background. It mitigates the software overhead generated by interrupt processing of the data input/output via SIO, HIO, MIO, and SDCIF (μPD77213 only).

Data of 14 Kwords at addresses 0x0000 to 0x37FF of the internal data RAM can be transferred by means of DMA.

2.4.8 SD card interface (SDCIF)

The μPD77213 supports SD Card interface. This interface is for access of SD card. It supports the DMA transfer for input data to internal data RAM. The SD card is accessed by using a dedicated routine of system ROM.

2.4.9 Debug interface (IEIO)

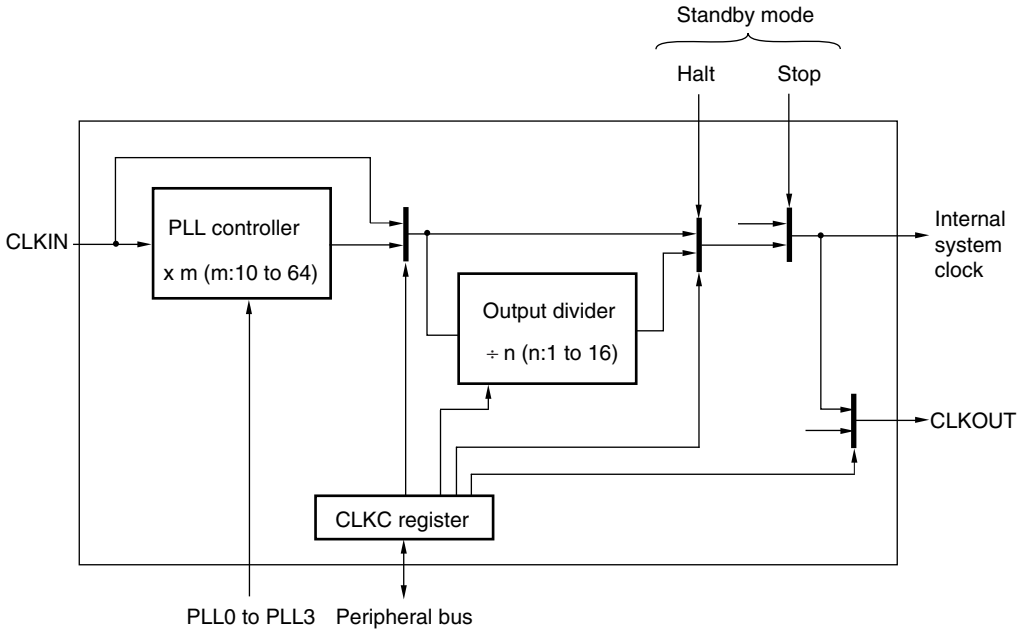
The μPD77210 Family has the following functions that conform to the JTAG (Joint Test Action Group) interface as a debug interface.

A device conforming to JTAG has an access port dedicated to testing and can be tested independently of the internal logic.

The μPD77210 Family has registers and a control circuit for in-circuit emulation, in addition to the instruction registers, bypass registers, and boundary scan registers that are required by the JTAG Recommendation.

3. CLOCK GENERATOR

The clock generator generates an internal system clock based on the external clock input from the CLKIN pin and supplies the clock to the μPD77210 Family. The configuration of the clock generator is as illustrated below.



The PLL is stopped immediately after reset. The clock input from the CLKIN pin is directly supplied to the μPD77210 Family internal circuitry and bootup commences. The PLL is started up in the boot routine and booting is carried out via the PLL output clock (except in the case of non-boot or external memory boot). In the case of non-boot or external memory boot, when booting has finished, after the PLL is started up by setting the CLKC register from the user program, the clock source must be switched to the PLL, in which case the PLL must be locked. Note that 300 μs are required between when the PLL is started up and when it is locked.

The PLL multiplication rate is specified by the external pins PLL0 to PLL3. The PLL also has two lock range modes: 80 to 120 MHz and 120 to 160 MHz. The mode to be used is specified by the P3 pin during booting. The CLKC register is used to control turning on/off the PLL, select the clock source (external clock/multiplied clock/divided or non-divided output), control resetting the output divider, set the division ratio, and enable/disable CLKOUT pin output.

When the output divider is selected, the high-level width of the clock output by the CLKOUT pin is equivalent to 1 cycle of the normal operation (which means that the clock does not have a duty factor of 50%).

In halt mode, output of the divider circuit is automatically selected as the clock source. When the divider circuit is selected, the clock is not changed even if halt mode is set.

In stop mode, the system clock supplied to the internal circuitry is masked. Because the PLL is not stopped automatically, it can recover from stop mode without PLL lock time. It is necessary to set the CLKC register by the program to stop the PLL.

4. RESET FUNCTION

The device is initialized when a low level of the specified width is input to the $\overline{\text{RESET}}$ pin.

4.1 Hardware Reset

The internal circuitry of the μPD77210 Family is initialized when the $\overline{\text{RESET}}$ pin is asserted active (low level) for a specific period. When the $\overline{\text{RESET}}$ pin is then deasserted inactive (high level), booting of the instruction RAM is performed in accordance with the status of the port pins (P0, P1, P2, and P3), and then processing is executed starting from the instruction at address 0x200 (reset entry) of the instruction memory.

5. FUNCTION OF BOOT-UP ROM

The instruction RAM is booted up by using the internal boot-up ROM when power is applied or when the contents of the instruction memory are to be rewritten by the program.

5.1 Boot at Reset

Immediately after release of a hardware reset, the boot program first reads general-purpose I/O port pins P0 to P3, and a boot mode (memory boot/host boot/serial boot) is determined by the bit patterns of these port pins. Once the booting processing has been completed, processing is executed starting from the instruction at address 0x200 (reset entry) of the instruction memory.

P2	P1	P0	Boot Mode
0	0	0	Non-boot[Note]
0	0	1	X memory initial boot
0	1	0	Y memory initial boot
0	1	1	XY memory initial boot
1	0	0	External memory initial boot
1	0	1	Host boot
1	1	0	Serial boot

Note This setting is used when the μPD77210 Family must be reset upon restoration from standby mode after a reset boot has been executed once.

P3	PLL lock range
0	120 to 160 MHz
1	80 to 120 MHz

5.1.1 Memory boot

The instruction code stored in data memory is transferred to the instruction RAM. Depending on the data memory from which the instruction code is to be transferred, X memory boot (booting from the X data memory), Y memory boot (booting from the Y data memory), XY memory boot (booting from the X and Y data memories), or external memory boot (booting from the external data memory space) may be performed.

5.1.2 Host boot

The boot parameter and instruction code are obtained via the host interface and transferred to the instruction RAM.

5.1.3 Serial boot

The boot parameter and instruction code are obtained via the serial interface and transferred to the instruction RAM.

5.2 Reboot

The contents of the instruction RAM can be rewritten by calling the following reboot entries by the program.

Reboot Mode		Entry Address	Parameter				
			Number of Instruction Steps	Transfer Source Start Address	Transfer Destination	Transfer Destination Start Address	Transfer Destination Page (DPR)
Memory reboot	X memory	0x1	R7L	DP3	R6L	DP2	R5L
	Y memory	0x2	R7L	DP7	R6L	DP6	R5L
	XY memories	0x3	R7L	DP3, DP7	R6L	DP2	R5L
	External memory	0x4	R7L	DP3	R6L	DP2	R5L
Host reboot		0x5	R7L	–	R6L	DP2	R5L
Serial reboot		0x6	R7L	–	R6L	DP2	R5L

5.2.1 Memory reboot

The instruction code stored into data memory is transferred to the instruction RAM. Depending on the data memory from which the instruction code is to be transferred, X memory reboot (rebooting from the X data memory), Y memory reboot (rebooting from the Y data memory), XY memory reboot (rebooting from the X and Y data memories), or external memory reboot (rebooting from the external data memory space) may be performed.

Perform memory rebooting by setting the following parameters and calling the entry address by the corresponding rebooting method.

- R7L: Number of instruction steps to be rebooted
- DP3: First address of X memory storing instruction code (to reboot from X, XY or external memories)
- DP7: First address of X memory storing instruction code (to reboot from Y or XY memories)
- R6L: Transfer source data page register (DPR) (Specify 0x00 in the case of the internal data RAM area.)
  Index register (for external memory rebooting)
- DP2: Transfer destination address of the instruction to be rebooted (to reboot from X, XY or external memories)
- DP6: Transfer destination address of the instruction to be rebooted (to reboot from Y memories)
- R5L: Transfer destination page register (DPR) (Specify 0x80 in the case of the internal instruction RAM area.)

5.2.2 Host reboot

The instruction code is obtained via the host interface and transferred to the instruction RAM.

The entry address is 0x5. Host rebooting is executed by setting the following parameters and then calling this address.

- R7L: Number of instruction steps to be rebooted
- R6L: Host status register (HST)
- DP2: Transfer destination address of instruction to be rebooted (offset 0x8000 in the case of internal instruction RAM area)
- R5L: Transfer destination data page register (DPR) (Specify 0x80 of the internal instruction RAM area.)

5.2.3 Serial reboot

The instruction code is obtained via the serial interface (TDMSIO) and then transferred to the instruction RAM.

The entry address is 0x6. Host rebooting is executed by setting the following parameters and then calling this address.

- R7L: Number of instruction steps to be rebooted
- R6L: Serial status register (SST) (Specify 0x0EC0.)
- DP2: Transfer destination address of instruction to be rebooted (offset 0x8000 in the case of internal instruction RAM area)
- R5L: Transfer destination data page register (DPR) (Specify 0x80 of the internal instruction RAM area.)

6. STANDBY MODE

The μPD77210 Family can be set to either of two standby modes. Each mode can be set by executing the corresponding instruction. The power consumption can be reduced in these modes.

6.1 Halt Mode

The halt mode can be set by executing the HALT instruction. In this mode, all the functions except the clock circuit and PLL are stopped and, therefore, the current consumption can be reduced.

The device can be released from this mode by an interrupt or hardware reset. To release the device from halt mode by issuing an interrupt, the contents of the internal registers and memories are retained. It takes 10 to 20 system clocks to release the μPD77210 Family from halt mode (if it is released by an interrupt).

When releasing the device from halt mode by using hardware reset, the external clock must be selected as the clock source in advance that the contents of memories are retain.

In halt mode, the clock circuit of the μPD77210 Family supplies the clock divided by the ratio specified by the CLKC register as the internal system clock. The same applies to the clock output by the CLKOUT pin.

6.2 Stop Mode

Stop mode is set when a STOP instruction is executed. In this mode, supply of the clock to the internal system is stopped.

If the PLL is stopped before stop mode is set, all the functions, including the clock circuit and PLL, are stopped. As a result, only a leakage current flows and, therefore, the current consumption can be minimized. In this case, the external clock must be selected as the clock source in advance.

The device is released from stop mode by a hardware reset or the CSTOP pin.

To release the device from stop mode by using the CSTOP pin, the contents of the internal registers and memories are retained. When releasing the device from stop mode by using hardware reset, the external clock must be selected as the clock source in advance that the contents of memories are retain.

7. MEMORY MAP

The μPD77210 Family employs a Harvard architecture that separates the instruction memory space from the data memory space.

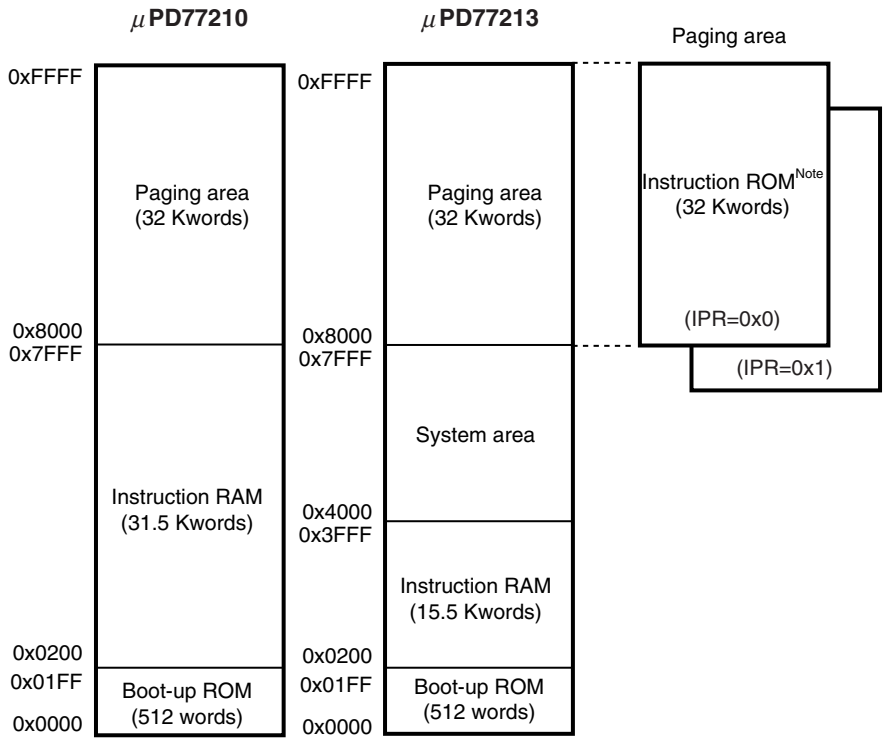
7.1 Instruction Memory

7.1.1 Instruction memory map

The instruction memory space consists of 64 Kwords × 32 bits. The area at addresses 0x8000 to 0xFFFF is a paging area that supports a memory space of 64 Kwords or more by specifying a page by using the instruction paging register (IPR).

The instruction ROM of the μPD77213 exists in the paging area and is accessed as IPR=0x0 or 0x1.

The paging area of the μPD77210 is reserved for future expansion.



Note The higher 8 words of the instruction ROM (0xFFF8 to 0xFFFF) constitute system area.

Caution Programs and data cannot be allocated to the system area, and neither can it be accessed. If these addresses are accessed, correct operation of the device is not guaranteed. A paging area in which no IPR page exists cannot be accessed. If this kind of paging area is accessed, correct operation of the device is not guaranteed.

7.1.2 Interrupt vector table

Addresses 0x200 to 0x23F of the instruction memory are assigned to entry points (vectors) of interrupts. Four instruction addresses are assigned to each interrupt source.

Four interrupt sources are assigned to each interrupt vector. There are 12 vectors. By identifying the source in the vector, the μPD77210 can use 38 interrupt sources and μPD77213 can use 42 interrupt sources.

Each of these interrupt sources can be masked by using the interrupt control register (ICR0 to ICR11).

Vector	Interrupt Source			
	0	1	2	3
0x200	Reset	Reserved	Reserved	Reserved
0x204	Reserved	Reserved	Reserved	Reserved
0x208	Reserved	Reserved	Reserved	Reserved
0x20C	Reserved	Reserved	Reserved	Reserved
0x210	$\overline{\text{INT00}}$	$\overline{\text{INT01}}$	$\overline{\text{INT02}}$	$\overline{\text{INT03}}$
0x214	$\overline{\text{INT10}}$	$\overline{\text{INT11}}$	$\overline{\text{INT12}}$	$\overline{\text{INT13}}$
0x218	$\overline{\text{INT20}}$	$\overline{\text{INT21}}$	$\overline{\text{INT22}}$	$\overline{\text{INT23}}$
0x21C	$\overline{\text{INT30}}$	$\overline{\text{INT31}}$	$\overline{\text{INT32}}$	$\overline{\text{INT33}}$
0x220	TSI input	TSIEN	PMT ch0 (TSI input)	SDCR input[Note]
0x224	TSO output	TSOEN	PMT ch1 (TSO output)	SDCR output[Note]
0x228	ASI input	ASIEN	PMT ch2 (ASI input)	SDDAT input[Note] (busy release)
0x22C	ASO output	ASOEN	PMT ch3 (ASO output)	SDDAT output[Note]
0x230	HI input	$\overline{\text{HWR}}$	PMT ch4 (HI input)	Reserved
0x234	HO output	$\overline{\text{HRD}}$	PMT ch5 (HO output)	Reserved
0x238	TIMER ch0	TIMER ch1	PMT ch6 (MI input)	Reserved
0x23C	TIMER ch1	TIMER ch0	PMT ch7 (MO output)	Reserved

Note These interrupt sources are for the μPD77213 only. When using the μPD77210, they are reserved.

Cautions 1. Reset is not an interrupt but is used as an entry of a vector.

2. It is recommended that the vector of an interrupt source that is not used branch to an abnormality processing routine.

7.2 Data Memory

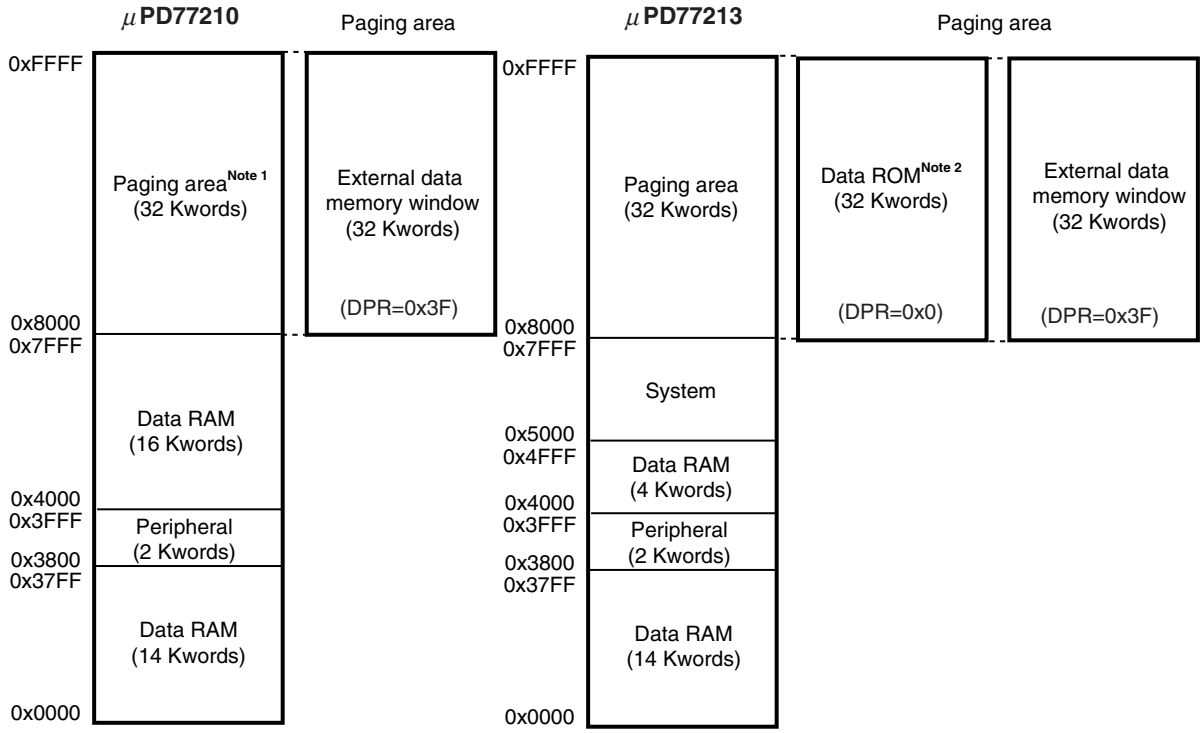
7.2.1 Data memory map

The data memory space consists of two planes: the X and Y memory spaces, each of which consists of 64 Kwords × 16 bits. The area of 0x8000 to 0xFFFF is a paging area that supports a memory space of 64 Kwords or more by specifying a page by using the data paging register (DPR). The DPR can be set in the same manner regardless of whether the X or Y memory space is accessed.

Page 0x3F of DPR is a window to the external data memory. The Data ROM of the μPD77213 exists in the paging area and is accessed as DPR=0x0.

Page 0x80 of the DPR is shared by 0x0000 to 0x7FFF of the internal instruction RAM. The lower 16 bits of the 32-bit instruction RAM constitute the X data memory, while the higher 16 bits are the Y data memory.

Because some pins of the μPD77213 are shared with the SD card interface, the area that can be accessed when the SD card interface is being used is restricted. The address pins MA13 to MA19 are shared with the SD card interface. When the SD card interface is being used, therefore, only the 13-bit address area of MA0 to MA12 (8 Kwords) can be accessed.



Notes 1. If the paging register is set to a value other than 0x3F (external data memory window) or 0x80 (internal instruction RAM area), programs and data cannot be stored to the addresses of the paging area, nor can these addresses be accessed.

2. The higher 8 words of the data ROM (0xFFF8 to 0xFFFF) constitute system area.

Caution Programs and data cannot be allocated to the system area, and neither can it be accessed. If these addresses are accessed, correct operation of the device is not guaranteed. A paging area in which no DPR page exists cannot be accessed. If this kind of paging area is accessed, correct operation of the device is not guaranteed.

7.2.2 Internal peripherals

The internal peripherals are mapped to the internal data memory space.

Cautions 1. The register names shown in the above table are not reserved words in either assembler or C. To use these names in assembler or C, therefore, the user must define them.

2. The same register is accessed regardless of whether the X memory space or Y memory space is accessed, provided that the address is the same.

3. Different registers cannot be accessed simultaneously from the X and Y memory spaces.

Memory-Mapped Peripherals (1/3)

X/Y Memory Address	Register Name	Function	Peripheral Name
0x3800	TSDT/SDT1	TDM serial data register/Serial data register 1	TSIO(SIO1)
0x3801	SST1	Serial status register 1	
0x3802	TSST	TDM serial status register	
0x3803	TFMT	TDM frame format register	
0x3804	TTXL	TDM transfer slot register (low)	
0x3805	TTXH	TDM transfer slot register (high)	
0x3806	TRXL	TDM receive slot register (low)	
0x3807	TRXH	TDM receive slot register (high)	
0x3808 to 0x380F	Reserved area	**Caution Do not access this area.**	–
0x3810	ASDT/SDT2	Audio serial data register/Serial data register 2	ASIO(SIO2)
0x3811	SST2	Serial status register 2	
0x3812	ASST	Audio serial status register	
0x3813 to 0x381F	Reserved area	**Caution Do not access this area.**	–
0x3820	HDT	Host interface data register	HIO
0x3821	HST	Host interface status register	
0x3822 to 0x383F	Reserved area	**Caution Do not access this area.**	–
0x3840	MDT	Memory data register	MIO
0x3841	MSHW	Memory I/F setup/hold width setting register	
0x3842	MCST	Memory I/F control/status register	
0x3843	MWAIT	Memory I/F wait register	
0x3844	MIDX	Direct access index register	
0x3845	MADRLI	Memory I/F input start address register (low)	
0x3846	MADRHI	Memory I/F input start address register (high)	
0x3847	MOFSI	Memory I/F input line offset register	
0x3848	MLENI	Memory I/F input line length register	
0x3849	MADRLO	Memory I/F output start address register (low)	
0x384A	MADRHO	Memory I/F output start address register (high)	
0x384B	MOFSO	Memory I/F output line offset register	
0x384C	MLENO	Memory I/F output line length register	
0x384D to 0x384F	Reserved area	**Caution Do not access this area.**	–
0x3850	PMSA0	PMT start address register 0	PMT ch0
0x3851	PMS0	PMT size register 0	
0x3852	PMC0	PMT control register 0	
0x3853	PMP0	PMT address pointer 0	

Memory-Mapped Peripherals (2/3)

X/Y Memory Address	Register Name	Function	Peripheral Name
0x3854	PMSA1	PMT start address register 1	PMT ch1
0x3855	PMS1	PMT size register 1	
0x3856	PMC1	PMT control register 1	
0x3857	PMP1	PMT address pointer 1	
0x3858	PMSA2	PMT start address register 2	PMT ch2
0x3859	PMS2	PMT size register 2	
0x385A	PMC2	PMT control register 2	
0x385B	PMP2	PMT address pointer 2	
0x385C	PMSA3	PMT start address register 3	PMT ch3
0x385D	PMS3	PMT size register 3	
0x385E	PMC3	PMT control register 3	
0x385F	PMP3	PMT address pointer 3	
0x3860	PMSA4	PMT start address register 4	PMT ch4
0x3861	PMS4	PMT size register 4	
0x3862	PMC4	PMT control register 4	
0x3863	PMP4	PMT address pointer 4	
0x3864	PMSA5	PMT start address register 5	PMT ch5
0x3865	PMS5	PMT size register 5	
0x3866	PMC5	PMT control register 5	
0x3867	PMP5	PMT address pointer 5	
0x3868	PMSA6	PMT start address register 6	PMT ch6
0x3869	PMS6	PMT size register 6	
0x386A	PMC6	PMT control register 6	
0x386B	PMP6	PMT address pointer 6	
0x386C	PMSA7	PMT start address register 7	PMT ch7
0x386D	PMS7	PMT size register 7	
0x386E	PMC7	PMT control register 7	
0x386F	PMP7	PMT address pointer 7	
0x3870	PDT0	Port data register 0	PIO
0x3871	PCD0	Port command register 0	
0x3872	PDT1	Port data register 1	
0x3873	PCD1	Port command register 1	
0x3874	PDT2	Port data register 2	
0x3875	PCD2	Port command register 2	
0x3876	PDT3	Port data register 3	
0x3877	PCD3	Port command register 3	
0x3878, 0x3879	Reserved area	**Caution Do not access this area.**	–
0x387A, 0x387B	POWC	Power control register	Peripheral STOP mode

Memory-Mapped Peripherals (3/3)

X/Y Memory Address	Register Name	Function	Peripheral Name
0x387C to 0x387F	Reserved area	**Caution Do not access this area.**	–
0x3880	ICR0	Interrupt control register 0	INTC
0x3881	ICR1	Interrupt control register 1	
0x3882	ICR2	Interrupt control register 2	
0x3883	ICR3	Interrupt control register 3	
0x3884	ICR4	Interrupt control register 4	
0x3885	ICR5	Interrupt control register 5	
0x3886	ICR6	Interrupt control register 6	
0x3887	ICR7	Interrupt control register 7	
0x3888	ICR8	Interrupt control register 8	
0x3889	ICR9	Interrupt control register 9	
0x388A	ICR10	Interrupt control register 10	
0x388B	ICR11	Interrupt control register 11	
0x388C to 0x388F	Reserved area	**Caution Do not access this area.**	–
0x3890	TIR0	Timer initial register 0	TIM0
0x3891	TCR0	Timer count register 0	
0x3892	TCSR0	Timer control/status register 0	
0x3893	Reserved area	**Caution Do not access this area.**	–
0x3894	TIR1	Timer initial register 1	TIM1
0x3895	TCR1	Timer count register 1	
0x3896	TCSR1	Timer control/status register 1	
0x3897 to 0x389F	Reserved area	**Caution Do not access this area.**	–
0x38A0	CEFR	Collect enable flag register	IMC
0x38A1	CPR0	Collect page register 0	
0x38A2	CAR0	Collect address register 0	
0x38A3	CLIR0	Collect instruction data register (high) 0	
0x38A4	CUIR0	Collect instruction data register (low) 0	
0x38A5	CPR1	Collect page register 1	
0x38A6	CAR1	Collect address register 1	
0x38A7	CLIR1	Collect instruction data register (high) 1	
0x38A8	CUIR1	Collection instruction data register (low) 1	
0x38A9 to 0x38AF	Reserved area	**Caution Do not access this area.**	–
0x38B0	CLKC	Clock control register	CLKC
0x38B1 to 0x38BF	Reserved area	**Caution Do not access this area.**	–
0x38C0	IPR	Instruction paging register	Page register
0x38C1	DPR	Data paging register	
0x38C2 to 0x38CF	Reserved area	**Caution Do not access this area.**	–
0x38D0	ADCR[Note]	Additional I/F control register	Additional IO
0x38D1-0x3FFF	Reserved area	**Caution Do not access this area.**	–

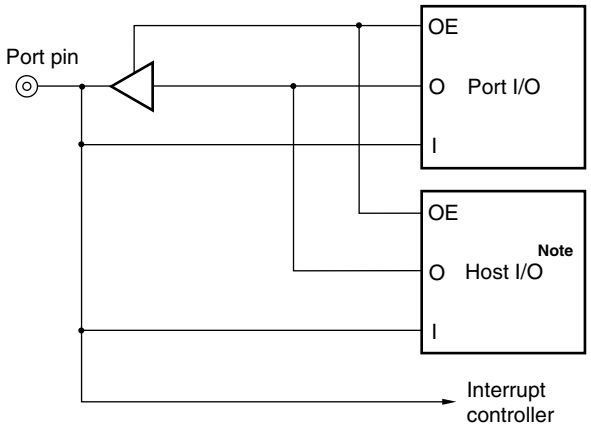
Note μPD77213 only. Do not access 0x38D0 of the μPD77210.

8. GENERAL-PURPOSE PORT AND INTERRUPT

8.1 General-purpose Port Pins

The general-purpose port pins alternate with the interrupt or host interface pins.

The configuration of the general-purpose port is illustrated below.



Note P0 to P7 do not alternate with the host interfave pins.

8.2 Interrupt Pin

The general-purpose port pin functions as an interrupt pin and the signal input to the port is always input to the interrupt controller. The interrupt controller recognizes the interrupt by detecting a falling edge.

The output of the general-purpose port or host interface pin can be also used as an interrupt input.

Pins $\overline{\text{HRD}}$, $\overline{\text{HWR}}$, ASOEN, ASIEN, TSOEN, and TSIEN are connected to the interrupt controller and can be used as interrupt pins.

9. INSTRUCTION

9.1 Outline of Instruction

One instruction consists of 32 bits. All the instructions, with some exceptions such as branch instructions, are executed with one system clock. The instruction cycle of the μPD77210 is up to 6.25 ns. The instruction cycle of the μPD77213 is up to 8.33 ns. The following nine types of instructions are available.

(1) Trinomial instructions

These instructions specify an operation by the MAC. As the operands, three general-purpose registers can be specified.

(2) Binomial instructions

These instructions specify an operation by the MAC, ALU, or BSFT. As the operands, two general-purpose registers can be specified. Some of these instructions allow one immediate value to be specified instead of a general-purpose register.

(3) Monomial instructions

These instructions specify an operation by the ALU. As the operand, a general-purpose register can be specified.

(4) Load/store instructions

These instructions specify 16-bit data transfer between memory and a general-purpose register. As the operand, any general-purpose register can be specified.

(5) Register-to-register transfer instructions

These instructions specify transfer between a general-purpose register and another register.

(6) Immediate value setting instructions

These instructions set an immediate value in the general-purpose registers and each register of the address operation unit.

(7) Branch instructions

These instructions specify branching of the program.

(8) Hardware loop instructions

These instructions specify the repetitive execution of an instruction.

(9) Control instructions

These instructions specify program control.

9.2 Instruction Set and Its Operation

Describe an operation in the operation field of each instruction in accordance with the description method of the operation representation format of the instruction. If two or more elements are available, select one of them.

(a) Correspondence between representation format and selectable register

The representation format and selectable register are as follows:

Representation Format	Selectable Register
ro, ro', ro"	R0 to R7
rl, rl'	R0L to R7L
rh, rh'	R0H to R7H
re	R0E to R7E
reh	R0EH to R7EH
dp	DP0 to DP7
dn	DN0 to DN7
dm	DMX, DMY
dpx	DP0 to DP3
dpy	DP4 to DP7
dpx_mod	DPn, DPn++, DPn—, DPn##, DPn%%, !DPn## (n = 0 to 3)
dpy_mod	DPn, DPn++, DPn—, DPn##, DPn%%, !DPn## (n = 4 to 7)
dp_imm	DPn## imm (n = 0 to 7)
*xxx	Contents of memory at address ××× (Example) If the contents of the DP0 register are 1000, *DP0 indicates the contents of memory address 1000.

(b) Modifying data pointer

The data pointer is modified only after memory access. The result of the modification becomes valid starting from the instruction that is executed immediately after. The data pointer cannot be modified without the memory access.

Example	Operation
DPn	Nothing is executed (value of DPn is not changed).
DPn++	DPn ← DPn + 1
DPn––	DPn ← DPn – 1
DPn##	DPn ← DPn + DNn (Value of DN0 to DN7 corresponding to DP0 to DP7 is added.) Example: DP0 ← DP0 + DN0
DPn%%	(n = 0 to 3) DPn = ((DP$_L$ + DNn) mod (DMX + 1)) + DP$_H$
	(n = 4 to 7) DPn = ((DP$_L$ + DNn) mod (DMY + 1)) + DP$_H$
!DPn##	Reverses bits of DPn and then accesses DPn. After memory access, DPn ← DPn + DNn
DPn## imm	DPn ← DPn + imm

(c) Instructions that can be described simultaneously

Those instructions that can be described simultaneously are indicated by √.

(d) Status of overflow flag (OV)

The status of the overflow flag is indicated by the following symbols:

●: No change

↕: Set to 1 if an overflow occurs.

Caution If an overflow does not occur after an operation, the overflow flag is not reset and its status remains the same as before the operation.

Instruction Set

Instruction Group	Instruction Name	Mnemonic	Operation	Instructions That Can Be Described Simultaneously									Flag
				Trinomial	Binomial	Monomial	Load/Store	Transfer	Immediate Value	Branch	Loop	Control	OV
Trinomial operation	Multiply add	ro = ro + rh*rh'	ro ← ro + rh*rh'				√						↕
	Multiply sub	ro = ro – rh*rh'	ro ← ro – rh*rh'				√						↕
	Signed/unsigned multiply add	ro = ro + rh*rl (rl is in positive integer format.)	ro ← ro + rh*rl				√						↕
	Unsigned/unsigned multiply add	ro = ro + rl*rl' (rl and rl' are in positive integer format.)	ro ← ro + rl*rl'				√						↕
	1-bit shift multiply add	ro = (ro >> 1) + rh*rh'	ro ← ro/2 + rh*rh'				√						↕
	16-bit shift multiply add	ro = (ro >> 16) + rh*rh'	ro ← ro/2 + rh*rh'				√						●
Binomial operation	Multiply	ro = rh*rh'	ro ← rh*rh'				√						●
	Add	ro" = ro + ro'	ro" ← ro + ro'				√						↕
	Immediate add	ro' = ro + imm	ro' ← ro + imm (where imm ≠ 1)										↕
	Sub	ro" = ro – ro'	ro" ← ro – ro'				√						↕
	Immediate sub	ro' = ro – imm	ro' ← ro – imm (where imm ≠ 1)										↕
	Arithmetic right shift	ro' = ro SRA rl	ro' ← ro >> rl				√						●
	Immediate arithmetic right shift	ro' = ro SRA imm	ro' ← ro >> imm										●
	Logical right shift	ro' = ro SRL rl	ro' ← ro >> rl				√						●
	Immediate logical right shift	ro' = ro SRL imm	ro' ← ro >> imm										●
	Logical left shift	ro' = ro SLL rl	ro' ← ro << rl				√						●
	Immediate logical left shift	ro' = ro SLL imm	ro' ← ro << imm										●
	And	ro" = ro & ro'	ro" ← ro & ro'				√						●
	Immediate and	ro' = ro & imm	ro' ← ro & imm										●
	Or	ro" = ro | ro'	ro" ← ro | ro'				√						●
	Immediate or	ro' = ro | imm	ro' ← ro | imm										●
	Exclusive or	ro" = ro^ro'	ro" ← ro^ro'				√						●
	Immediate exclusive or	ro‘ = ro^imm	ro' ← ro^imm										●
	Less than	ro" = LT (ro, ro')	if (ro < ro') {ro" ← 0x0000000001} else {ro" ← 0x0000000000}				√						●

Instruction Group	Instruction Name	Mnemonic	Operation	Instructions That Can Be Described Simultaneously									Flag
				Trinomial	Binomial	Monomial	Load/Store	Transfer	Immediate Value	Branch	Loop	Control	OV
Monomial operation	Clear	CLR (ro)	ro ← 0x0000000000				√					√	●
	Increment	ro' = ro + 1	ro' ← ro + 1				√					√	↕
	Decrement	ro' = ro – 1	ro' ← ro – 1				√					√	↕
	Absolute value	ro' = ABS (ro)	if (ro < 0) {ro' ← –ro} else {ro' ← ro}				√					√	↕
	1's complement	ro' = ~ro	ro' ← ~ro				√					√	●
	2's complement	ro' = –ro	ro' ← –ro				√					√	↕
	Clip	ro' = CLIP (ro)	if (ro > 0x007FFFFFFF) {ro' ← 0x007FFFFFFF} elseif (ro < 0xFF80000000) {ro' ← 0xFF80000000} else {ro' ← ro}				√					√	●
	Round	ro' = ROUND (ro)	if (ro > 0x007FFF0000) {ro' ← 0x007FFF0000} elseif (ro < 0xFF80000000) {ro' ← 0xFF80000000} else {ro' ← (ro + 0x8000) & 0xFFFFFF0000}				√					√	●
	Exponent	ro' = EXP (ro)	ro' ← $\log_2$ (1/ro)				√					√	●
	Substitution	ro' = ro	ro' ← ro				√					√	●
	Accumulated add	ro' + = ro	ro' ← ro' + ro				√					√	↕
	Accumulated sub	ro' – = ro	ro' ← ro' – ro				√					√	↕
	Division	ro' / = ro	if (sign (ro') = = sign (ro)) {ro' ← (ro' – ro) << 1} else {ro' ← (ro' + ro) << 1} if (sign (ro') = = 0) {ro' ← ro' + 1}				√					√	↕

Instruction Group	Instruction Name	Mnemonic	Operation	Instructions That Can Be Described Simultaneously									Flag
				Trinomial	Binomial	Monomial	Load/Store	Transfer	Immediate Value	Branch	Loop	Control	OV
Load/store	Parallel load/store Notes 1, 2	ro = *dpx_mod ro' = *dpy_mod	ro ← *dpx, ro' ← *dpy	√	√	√							●
		ro = *dpx_mod *dpy_mod = rh	ro ← *dpx, *dpy ← rh										
		*dpx_mod = rh ro = *dpy_mod	*dpx ← rh, ro ← *dpy										
		*dpx_mod = rh *dpy_mod = rh'	*dpx ← rh, *dpy ← rh'										
	Partial load/store Notes 1, 2, 3	dest = *dpx_mod dest' = *dpy_mod	dest ← *dpx, dest' ← *dpy										●
		dest = *dpx_mod *dpy_mod = source	dest ← *dpx, *dpy ← source										
		*dpx_mod = source dest = *dpy_mod	*dpx ← source, dest ← *dpy										
		*dpx_mod = source *dpy_mod = source'	*dpx ← source, *dpy ← source'										
	Direct addressing load/store Note 4	dest = *addr	dest ← *addr										●
		*addr = source	*addr ← source										
	Immediate index load/store Note 5	dest = *dp_imm	dest ← *dp										●
		*dp_imm = source	*dp ← source										
Register-to-register transfer	Register-to-register transfer Note 6	dest = rl	dest ← rl									√	●
		rl = source	rl ← source										
Immediate value setting	Immediate value setting	rl = imm (where imm = 0 to 0xFFFF)	rl ← mm										●
		dp = imm (where imm = 0 to 0xFFFF)	dp ← imm										
		dn = imm (where imm = 0 to 0xFFFF)	dn ← imm										
		dm = imm (where imm = 1 to 0xFFFF)	dm ← imm										

Notes 1. Of the two mnemonics, either or both can be described.

2. After transfer, modification specified by mod is performed.

3. dest, dest' = {ro, reh, re, rh, rl}, source, source' = {re, rh, rl}

4. dest = {ro, reh, re, rh, rl}, source = {re, rh, rl}, addr = {0: X-0xFFFF: X (X memory), or 0: Y-0xFFFF: Y (Y memory)}

5. dest = {ro, reh, re, rh, rl}, source = {re, rh, rl}

6. Select any of the registers (except the general-purpose registers) as dest and source.

Instruction Group	Instruction Name	Mnemonic	Operation	Instructions That Can Be Described Simultaneously									Flag
				Trinomial	Binomial	Monomial	Load/Store	Transfer	Immediate Value	Branch	Loop	Control	OV
Branch	Jump	JMP imm	PC ← imm									√	●
	Register-to-register jump	JMP dp	PC ← dp									√	●
	Subroutine call	CALL imm	SP ← SP + 1 STK ← PC + 1 PC ← imm									√	●
	Register-to-register subroutine call	CALL dp	SP ← SP + 1 STK ← PC + 1 PC ← dp									√	●
	Return	RET	PC ← STK SP ← SP – 1									√	●
	Interrupt return	RETI	PC ← STK STK ← SP – 1 Restores interrupt enable flag.									√	●
Hardware loop	Repeat	REP count	Start RC ← count RF ← 0 During repeat PC ← PC RC ← RC – 1 End PC ← PC + 1 RF ← 1										●
★	Loop	LOOP count (Instruction of 2 lines or more)	Start LC ← count LF ← 0 During loop PC ← PC + 1 (while PC < LEA) if (PC = LEA) PC ← LSA LC ← LC – 1 End PC ← PC + 1 LF ← 1										●
	Loop pop	LPOP	LC ← LSR3 LE ← LSR2 LS ← LSR1 LSP ← LSP – 1										●
Control	No operation	NOP	PC ← PC + 1										●
	Halt	HALT	CPU stops.										●
★	Stop	STOP	CPU stops, PLL, and OSC can be stopped by a user										●
	Condition	IF (ro cond)	Condition judgment			√		√		√			●
	Forget interrupt	FINT	Discards interrupt request.										●

10. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = +25°C)

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	IV_{DD}	For DSP core	− 0.5 to + 2.0	V
	EV_{DD}	For I/O pins	− 0.5 to + 4.6	V
Input voltage	V_I	$V_I < EV_{DD}$ + 0.5 V	− 0.5 to + 4.6	V
Output voltage	V_O		− 0.5 to + 4.6	V
Storage temperature	T_{stg}		− 65 to + 150	°C
Operating ambient temperature	T_A		− 20 to + 70	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operating voltage	IV_{DD}	For DSP core (operating speed 120 MHz Max.)	1.425	1.50	1.65	V
		For DSP core (operating speed 160 MHz Max.)[Note]	1.55	1.60	1.65	V
	EV_{DD}	For I/O pins	2.7	3.3	3.6	V
Input voltage	V_I		0		EV_{DD}	V

Note μPD77210 only

Capacitance (T_A = +25°C, IV_{DD} = 0 V, EV_{DD} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz, Pins other than those tested: 0 V		10		pF
Output capacitance	C_O			10		pF
I/O capacitance	C_{IO}			10		pF

DC Characteristics (Unless otherwise specified, T_A = – 20 to + 70°C, with IV_{DD} and EV_{DD} within recommended operating condition range)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IHN}	Pins other than below		0.7 EV_{DD}		EV_{DD}	V
	V_{IHC}	CLKIN		0.7 EV_{DD}		EV_{DD}	V
	V_{IHS}	$\overline{RESET}$, P0 to P15, TSCK, TSIEN,TSOEN, ASCK, ASIEN, ASOEN		0.8 EV_{DD}		EV_{DD}	V
Low level input voltage	V_{ILN}	Pins other than below		0		0.2 EV_{DD}	V
	V_{ILC}	CLKIN		0		0.2 EV_{DD}	V
	V_{ILS}	$\overline{RESET}$, P0 to P15, TSCK, TSIEN,TSOEN, ASCK, ASIEN, ASOEN		0		0.2 EV_{DD}	V
High level output voltage	V_{OH}	I_{OH} = –100 μA		0.8 EV_{DD}			V
Low level output voltage	V_{OL}	I_{OL} = 2.0 mA				0.2 EV_{DD}	V
High level input leakage current	I_{LHN}	$V_I = EV_{DD}$		0		10	μA
Low level input leakage current	I_{LLN}	V_I = 0 V		–10		0	μA
High impedance leakage current	I_{LZ}	0 V ≤ V_I ≤ EV_{DD}		0		–10	μA
Pull-up pin current	I_{PUI}	TDI, TMS, 0 V ≤ V_I ≤ EV_{DD}		20	70	200	μA
Pull-down pin current	I_{PDI}	$\overline{TRST}$, 0 V ≤ V_I ≤ EV_{DD}		–20	–70	–200	μA
Internal supply current [fclkin = 10 MHz, IV_{DD} = 1.5 V, $V_{IHN} = V_{IHC} = V_{IHS} = EV_{DD}$, V_{IL} = 0 V, no load, T_A = 25°C]	I_{DD}	During operating, fclk = 100 MHz, PLL multiple rate x10			35[Note 1]	70[Note 2]	mA
	I_{DDH}	In halt mode, fclk = 100 MHz, PLL multiple rate x 10, division rate 1/1			20[Note 3]		mA
	I_{DDS}	In stop mode[Note 4], fclk = 0 Hz, PLL stop	μPD77210		240		μA
			μPD77213		120		

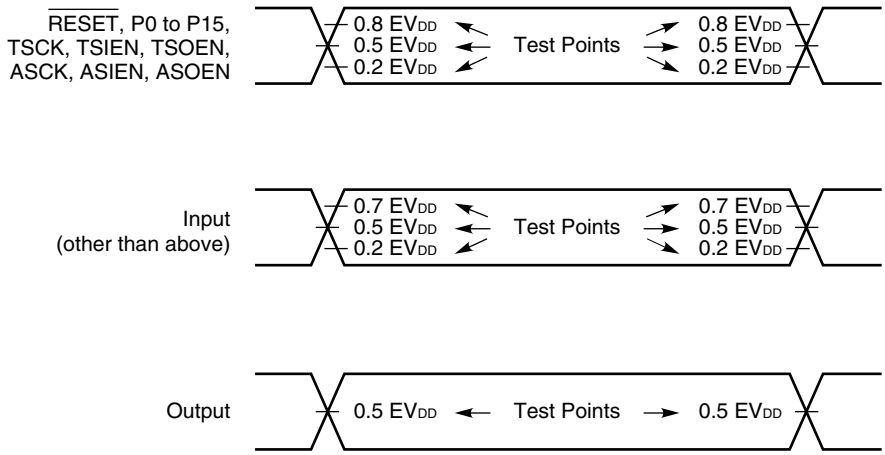
Notes 1. The value is when MAC with Dual Load instruction 50% + nop instruction 50% are executed. It is roughly estimated at 0.35 mA/MHz.

2. The value is when a special program that brings about frequent switching inside the device is executed.
It is roughly estimated at 0.7 mA/MHz.

3. The value is when the division rate is 1/1. It is roughly estimated at 0.2 mA/MHz + I_{DDS} using the divided clock.

4. The value in stop mode is the value when PLL is stopped.

Common Test Criteria of Switching Characteristics



AC Characteristics (T_A = – 20 to + 70°C, with IV_{DD} and EV_{DD} within recommended operating condition range)

Clock

Timing requirements

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CLKIN cycle time[Note 1]	t_{cCX}		62.5			ns
CLKIN high level width	t_{wCXH}		12.5			ns
CLKIN low level width	t_{wCXL}		12.5			ns
CLKIN rise/fall time	t_{rfCX}				5	ns
Internal clock cycle time	t_{cC}	Over 120 MHz(μPD77210 only)	6.25			ns
requirements		Under 120 MHz	8.33			ns
PLL lock-up time	t_{LPLL}				300	μs
PLL lock frequency[Note 1]	t_{cPLL}	When boot:P3 = 0[Note 2]	120		160	MHz
		When boot:P3 = 1	80		120	MHz

Notes 1. The CLKIN cycle time must accord with the PLL lock frequency. It is therefore necessary to satisfy both the CLKIN cycle time condition of 62.5 ns (MIN.) and the PLL lock frequency condition of a multiplied frequency in the range of 80 to 160 MHz.

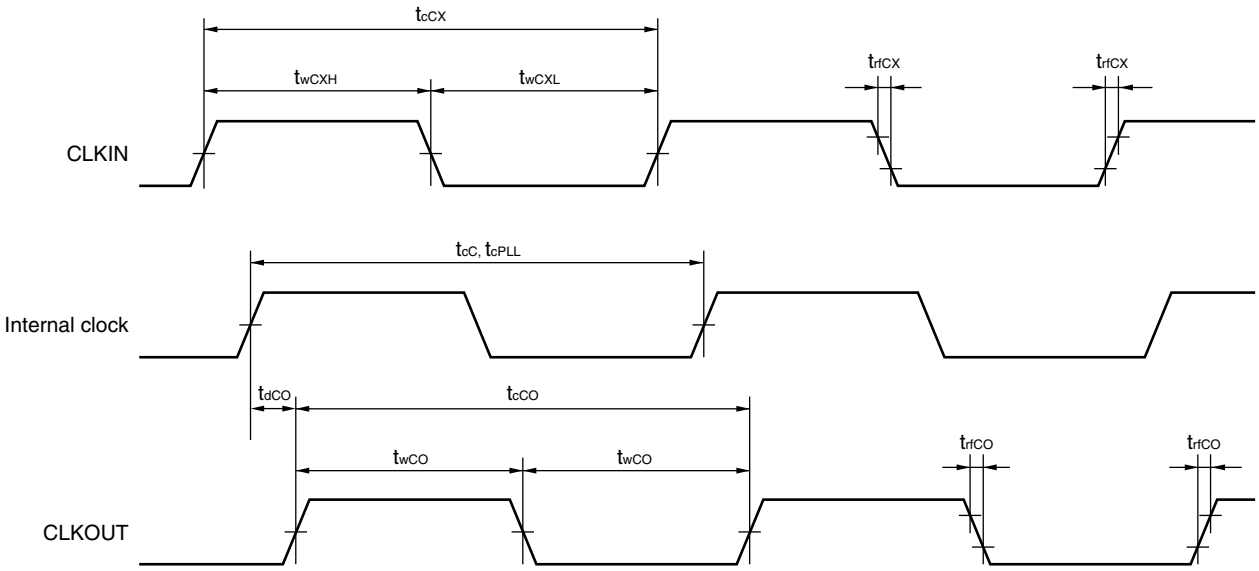
2. In the μPD77213, it can be set only when an external memory boot is being used.

Switching characteristics

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Internal clock cycle[Note]	t_{cC}				$t_{cCX} \div m \times n$		ns
CLKOUT cycle time	t_{cCO}				t_{cC}		ns
CLKOUT width	t_{wCO}	n = 1			$t_{cC} \div 2$		ns
		$n \geq 2$	High level width		$t_{cC} \div n$		ns
			Low level width		$t_{cC} - t_{cC} \div n$		ns
CLKOUT rise/fall time	t_{rfCO}					5	ns
CLKOUT delay time	t_{dCO}					6.25	ns

Note m: Multiple ratio, n: Division ratio (PLL, divider)

Clock I/O timing



Reset, Interrupt, System Control, Timer

Timing requirements

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ low level width	$t_{w(RL)}$		6 t_{cCX} Note 1			ns
CSTOP high level width	$t_{w(CSTOPH)}$		12 t_{cC} Note 2			ns
CSTOP recovery time	$t_{rec(CSTOP)}$		12 t_{cC} Note 2			ns
$\overline{\text{INTmn}}$ low level width	$t_{w\ (INTL)}$		6 t_{cC} Note 3			ns
$\overline{\text{INTmn}}$ recovery time	$t_{rec\ (INT)}$		6 t_{cC} Note 3			ns

Notes 1. When reset timing, it is specified by input clock.

2. When STOP or HALT mode, it is specified by divided clock.

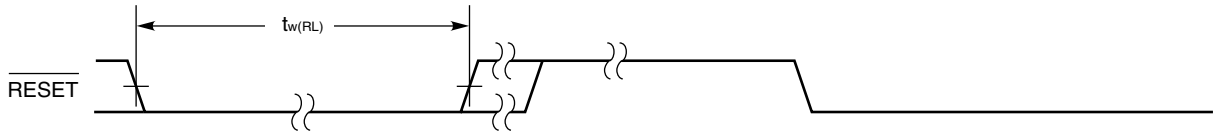
3. Interrupt can input by TSIEN, TSOEN, ASIEN, and ASOEN pins other than interrupt pins. The interrupt pins function alternately as pins P0 to P15.

Remark $\overline{\text{INTmn}}$ m, n = 0 to 3

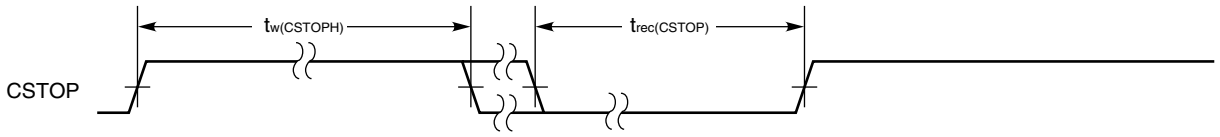
Switching characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
STOPS output delay time	t_{dSTP}		0		6.25	ns
HALTS output delay time	t_{dHLT}		0		6.25	ns
TIMOUT output delay time	t_{dTIM}		0		6.25	ns
TIMOUT output width	t_{wTIM}			4 t_{cC}		ns

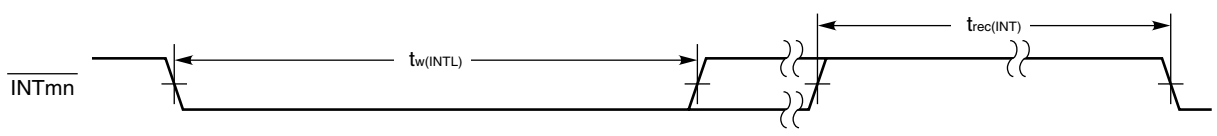
Reset timing



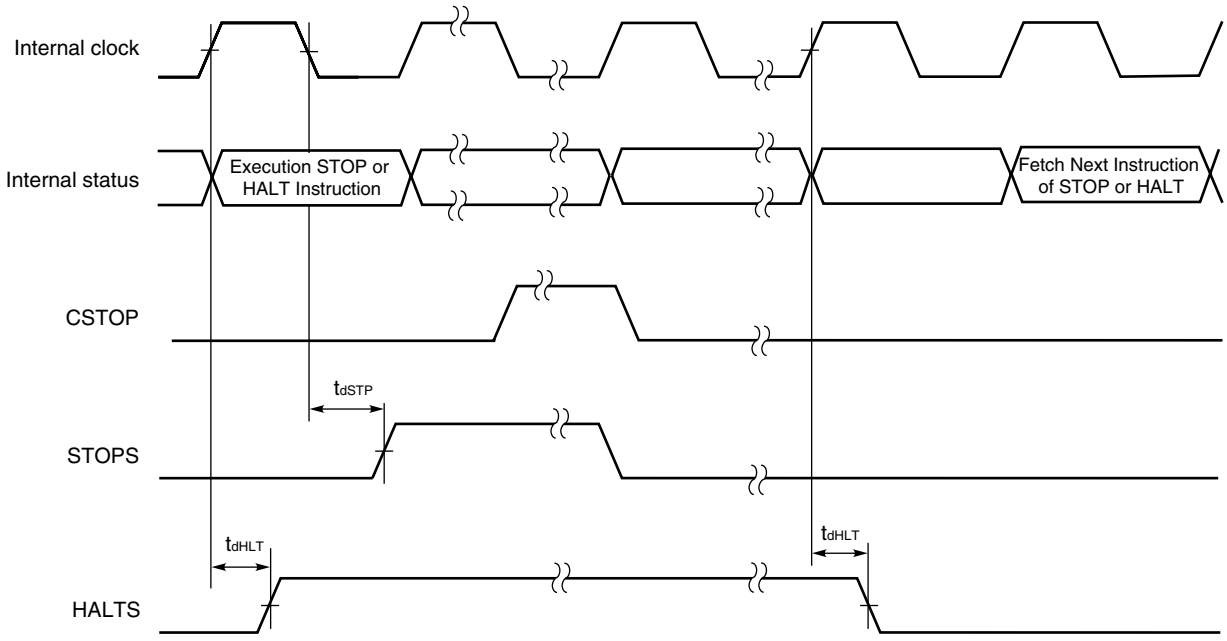
WAKEUP timing



Interrupt timing



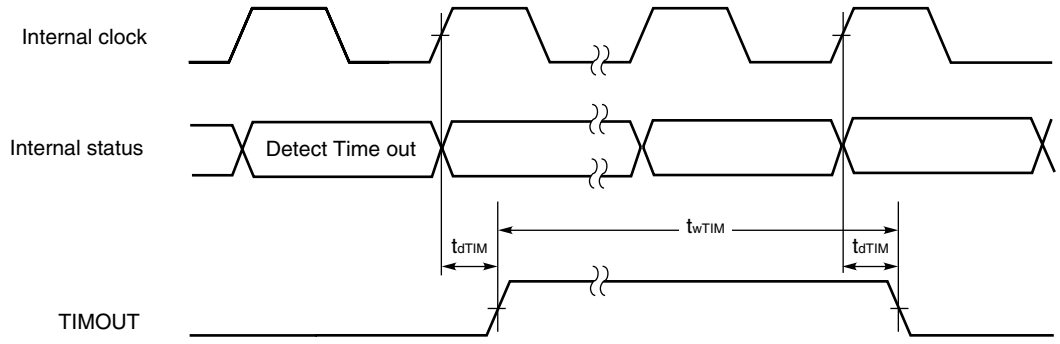
Standby mode status output timing



Remarks 1. Internal clock cycle is changed or stopped to be fixed to low level when STOP or HALT mode.

2. STOPS pin is become low level asynchronously by CSTOP pin rising edge.

Timer time out status output timing



External Data Memory Access

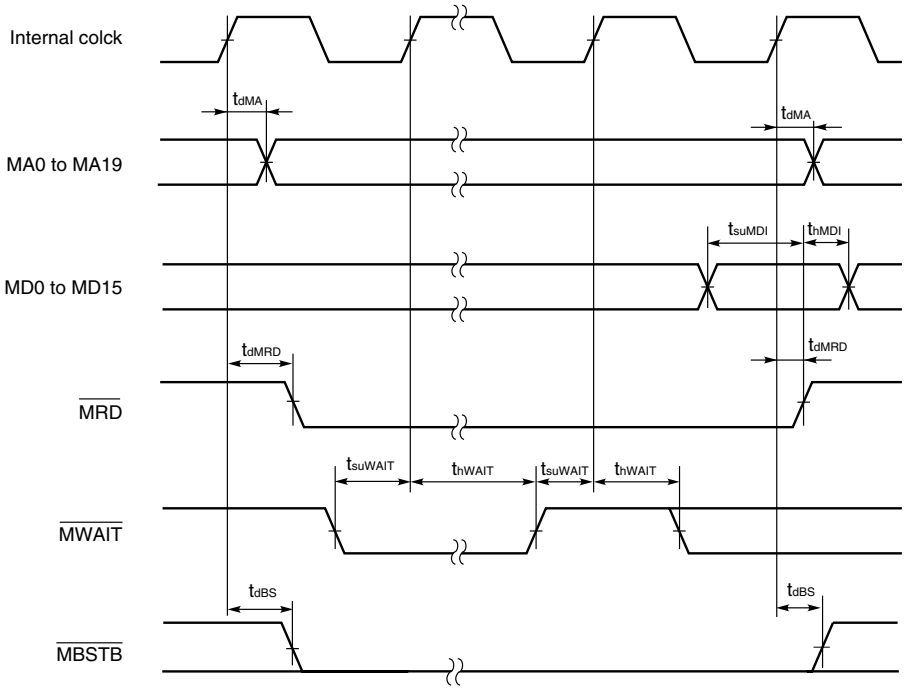
Timing requirements

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MD setup time	t_{suMDI}		17.5			ns
MD hold time	t_{hMDI}		0			ns
$\overline{\text{MHOLDRQ}}$ setup time	t_{suHRQ}		11.25			ns
$\overline{\text{MHOLDRQ}}$ hold time	t_{hHRQ}		0			ns
$\overline{\text{MWAIT}}$ setup time	t_{suWAIT}		11.25			ns
$\overline{\text{MWAIT}}$ hold time	t_{hWAIT}		0			ns

Switching characteristics

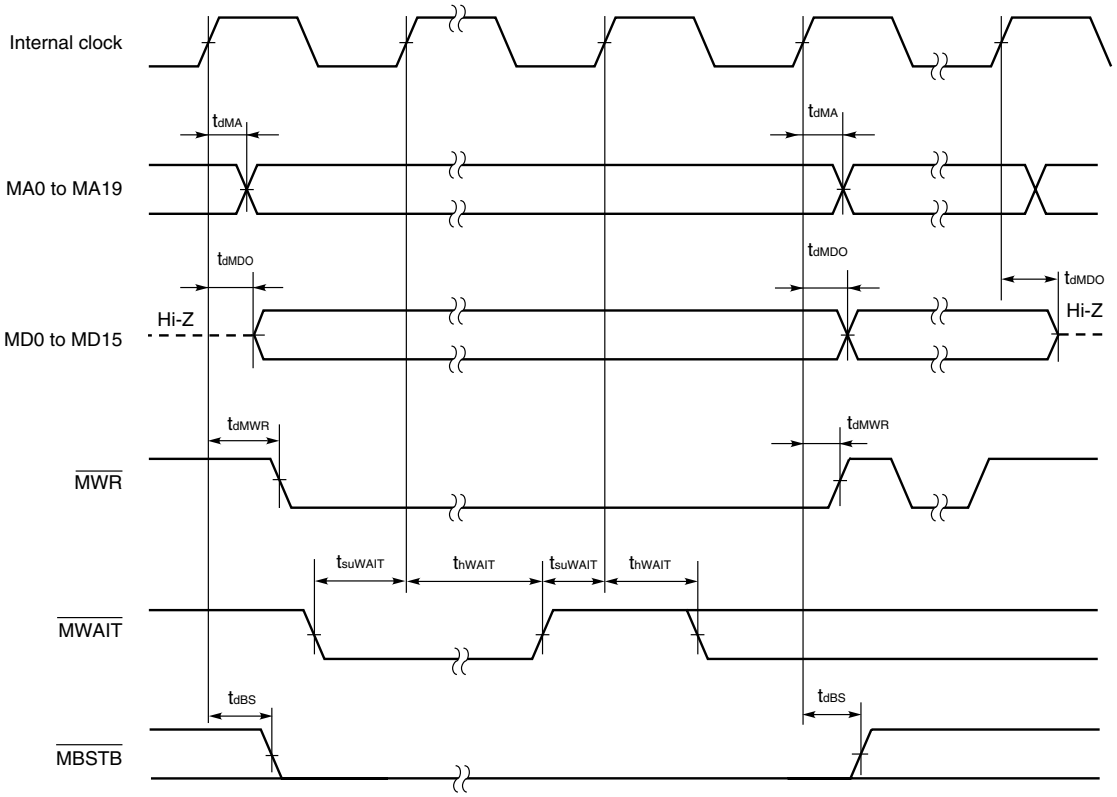
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MA output delay time	t_{dMA}		0		6.25	ns
$\overline{\text{MRD}}$ output delay time	t_{dMRD}		0		6.25	ns
$\overline{\text{MWR}}$ output delay time	t_{dMWR}		0		6.25	ns
MD output delay time	t_{dMDO}		0		6.25	ns
$\overline{\text{MBSTB}}$ output delay time	t_{dBS}		0		6.25	ns
$\overline{\text{MHOLDAK}}$ output delay time	t_{dHAK}		0		6.25	ns

External data memory access timing (Read)



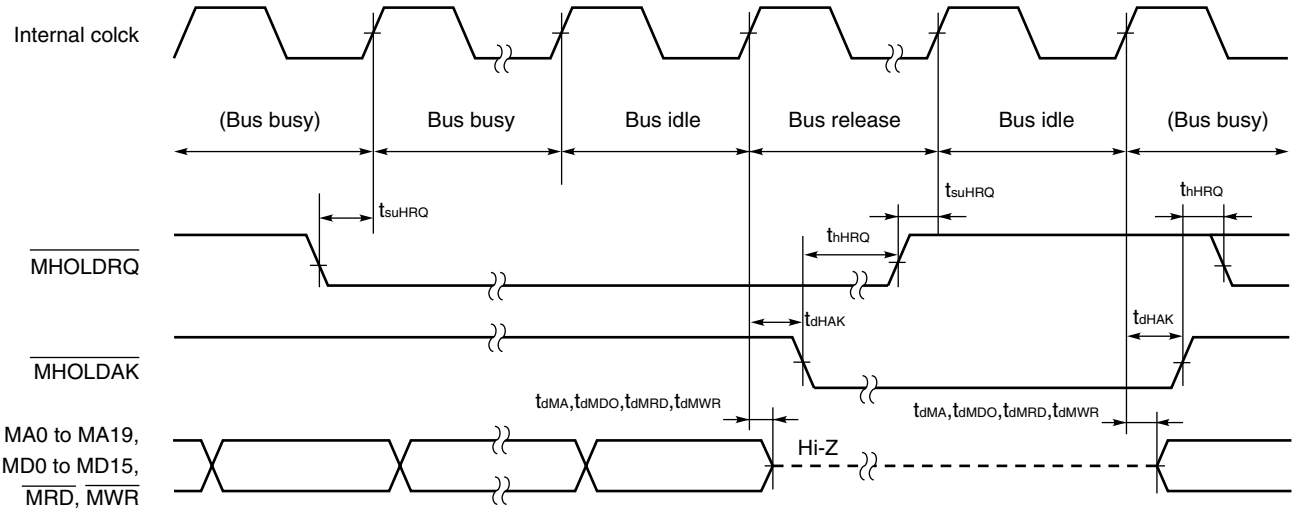
Remark In the μPD77213, it is possible to shift fall timing of $\overline{\text{MRD}}$ pin by cycle unit, by setting of MSHW register.

External data memory access timing (Write)



Remark It is possible to shift rise/fall timing of $\overline{\text{MWR}}$ pin by cycle unit, by setting of MSHW register.

Bus arbitration timing



General-purpose I/O Port

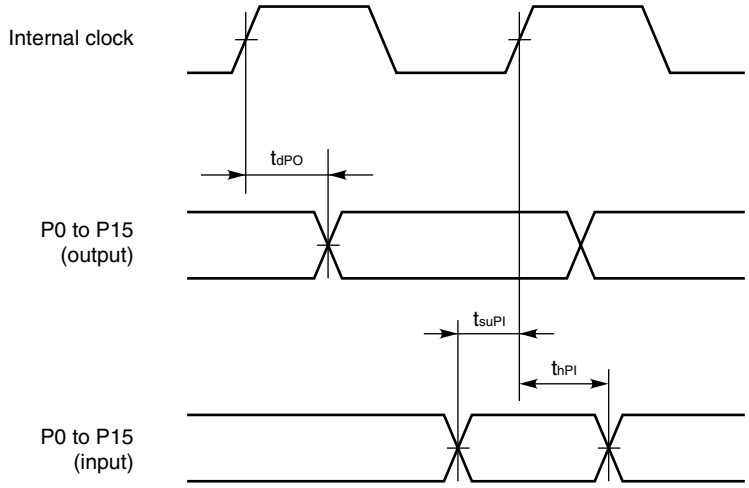
Timing requirements

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Port input setup time	t_{suPI}		11.25			ns
Port input hold time	t_{hPI}		6.25			ns

Switching characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Port output delay time	t_{dPO}		0		6.25	ns

General-purpose I/O port timing



Host Interface

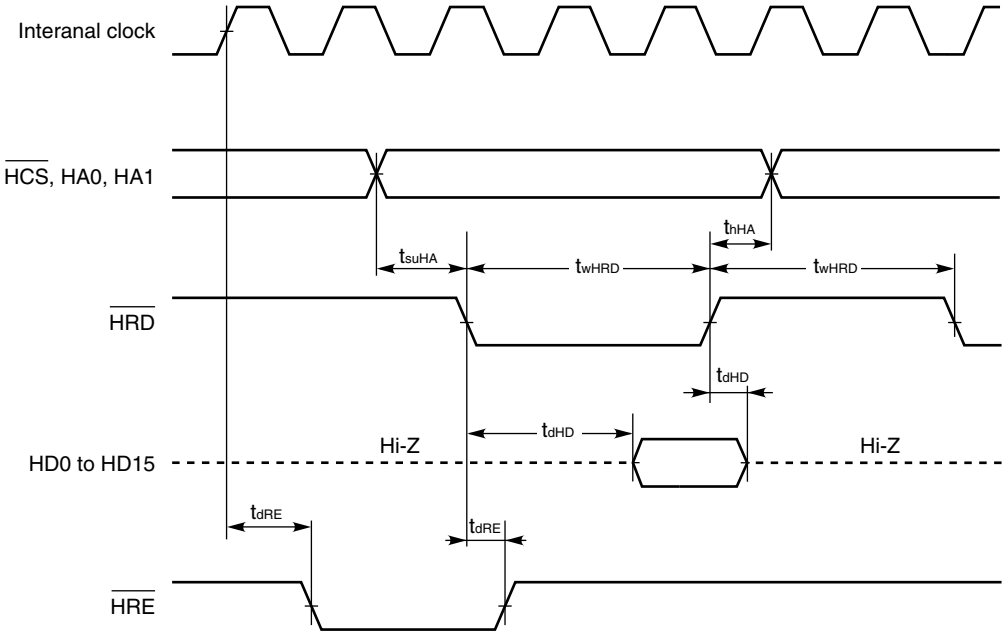
Timing requirements

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{HRD}$ low level width, recovery time	t_{wHRD}		3 t_{cC}			ns
$\overline{HWR}$ low level width, recovery time	t_{wHWR}		3 t_{cC}			ns
HD setup time	t_{suHDI}		6.25			ns
HD hold time	t_{hHDI}		6.25			ns
HA, $\overline{HCS}$ setup time	t_{suHA}		3			ns
HA,$\overline{HCS}$ hold time	t_{hHA}		0			ns

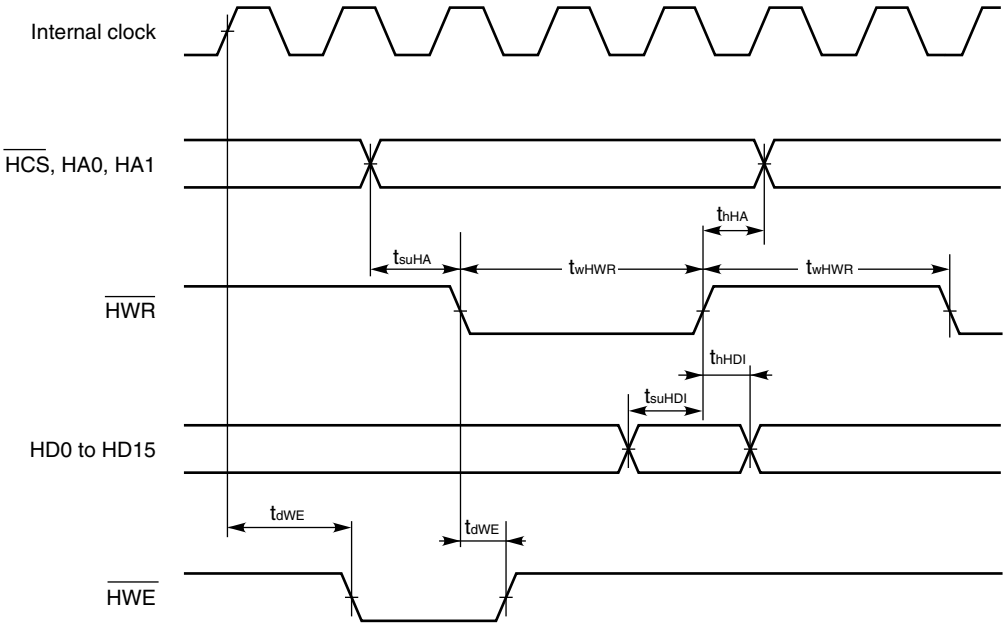
Switching characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{HRE}$ output delay time	t_{dRE}		0		11.25	ns
$\overline{HWE}$ output delay time	t_{dWE}		0		11.25	ns
HD output delay time	t_{dHD}		0		11.25	ns

Host read interface timing



Host write interface timing



Serial Interface (Standard Serial mode/ TDM serial mode)

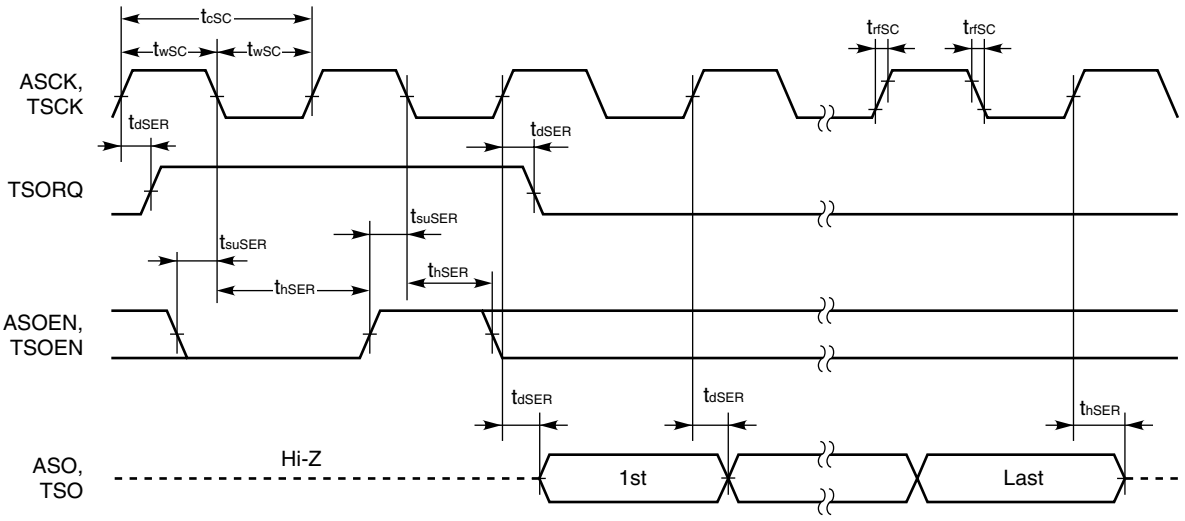
Timing requirements

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{cSC}		50 and 2 t_{cC}			ns
ASCK high /low level width	t_{wSC}		25			ns
ASCK rise/fall time	t_{rfSC}				20	ns
Serial input setup time	t_{suSER}		12.5			ns
Serial input hold time	t_{hSER}		12.5			ns

Switching characteristics

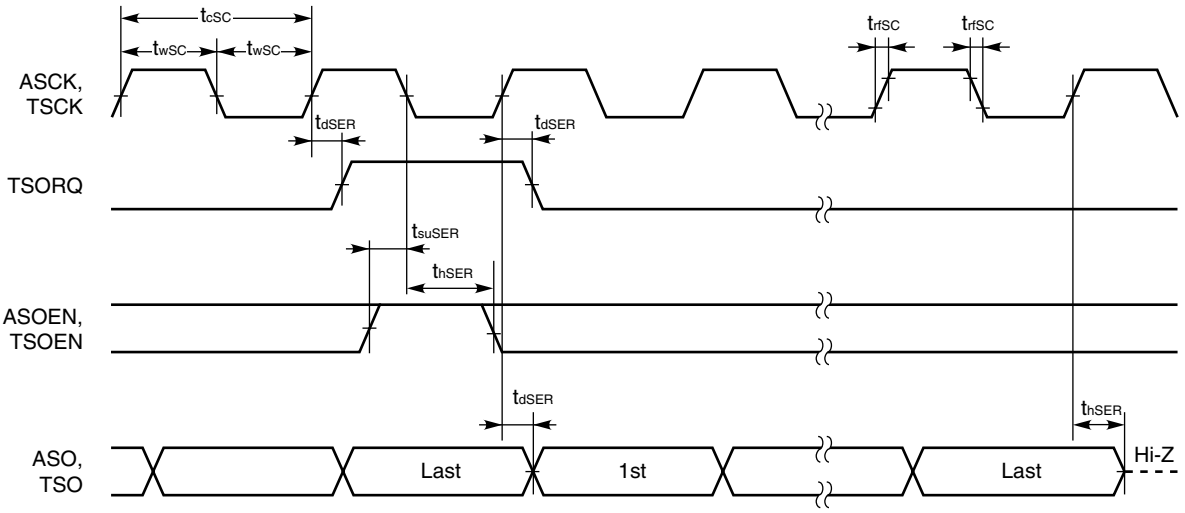
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Serial output delay time	t_{dSER}		0		17.5	ns

Serial output timing 1



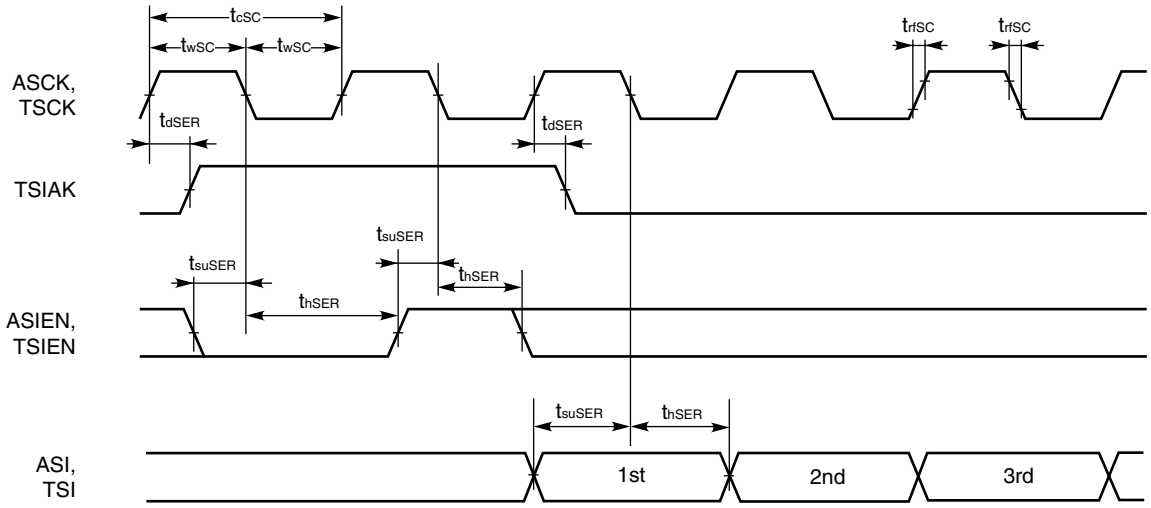
Note When TDM mode, TSO output value is delay for a bit according to TDM setting value.

Serial output timing 2 (during successive output)



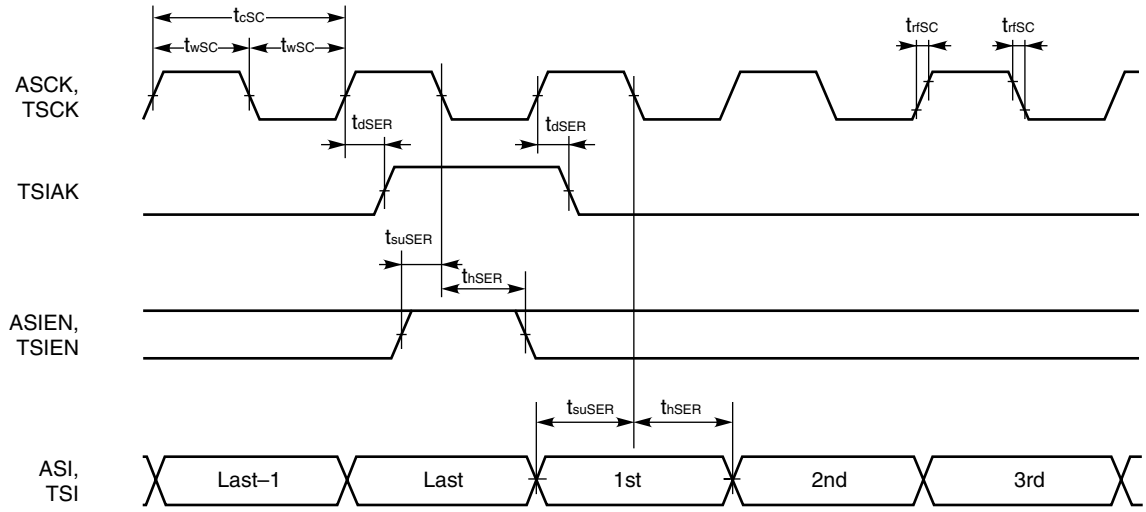
Note When TDM mode, TSO output value is delay for a bit or dummy cycle (high impedance) is inserted, according to TDM setting value.

Serial input timing 1



Note When TDM mode, TSI input value is delay for a bit according to TDM setting value.

Serial input timing 2 (during successive input)



Note When TDM mode, TSI input value is delay for a bit or skip cycle is input, according to TDM setting value.

Serial Interface (Audio Serial mode)

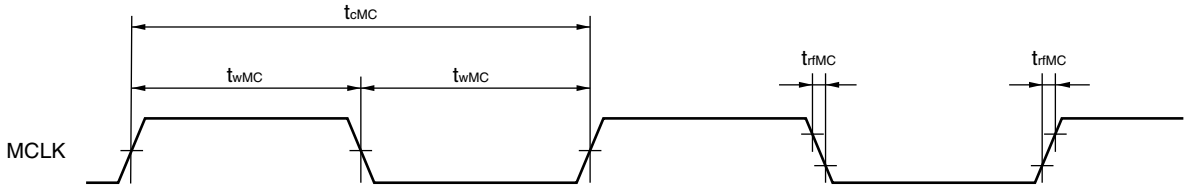
Timing requirements

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MCLK cycle time	t_{cMC}	Master mode	50 and 2 t_{cC}			ns
MCLK high/low level width	t_{wMC}	Master mode	25			ns
MCLK rise/fall time	t_{rfMC}	Master mode			20	ns
BCLK cycle time	t_{cBC}	Slave mode	50 and 8 t_{cC}			ns
BCLK high/low level width	t_{wBC}	Slave mode	25			ns
BCLK rise/fall time	t_{rfBC}	Slave mode			20	ns
Serial input setup time	t_{suASER}	Slave mode	12.5			ns
		Master mode	25.0			ns
Serial input hold time	t_{hASER}	Slave mode	12.5			ns
		Master mode	25.0			ns

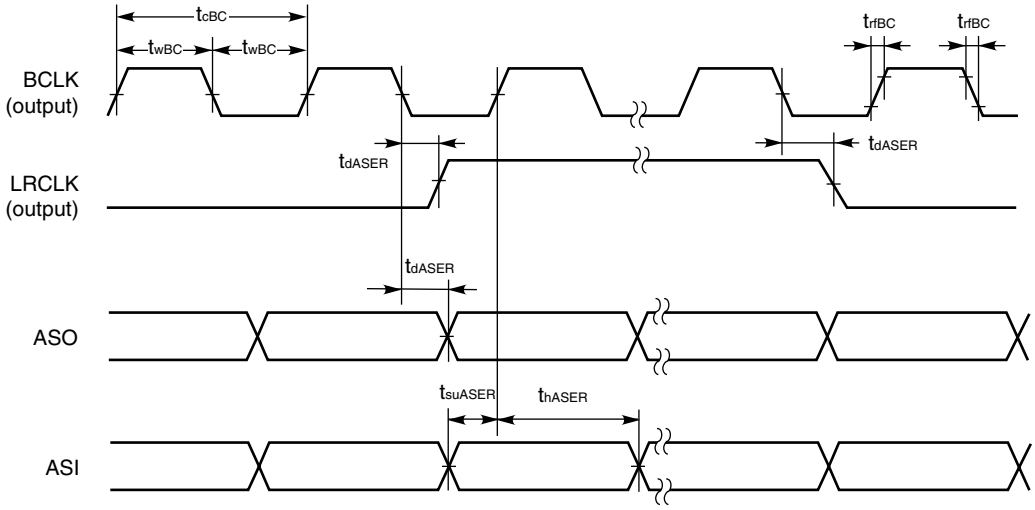
Switching characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
BCLK cycle time	t_{cBC}	Master mode	50 and 8 t_{cC}			ns
BCLK high/low level width	t_{wBC}	Master mode	25			ns
BCLK rise/fall time	t_{rfBC}	Master mode			5	ns
Serial output delay time	t_{dASER}	Master mode	−12.5		+25.0	ns
		Slave mode	0		17.5	ns

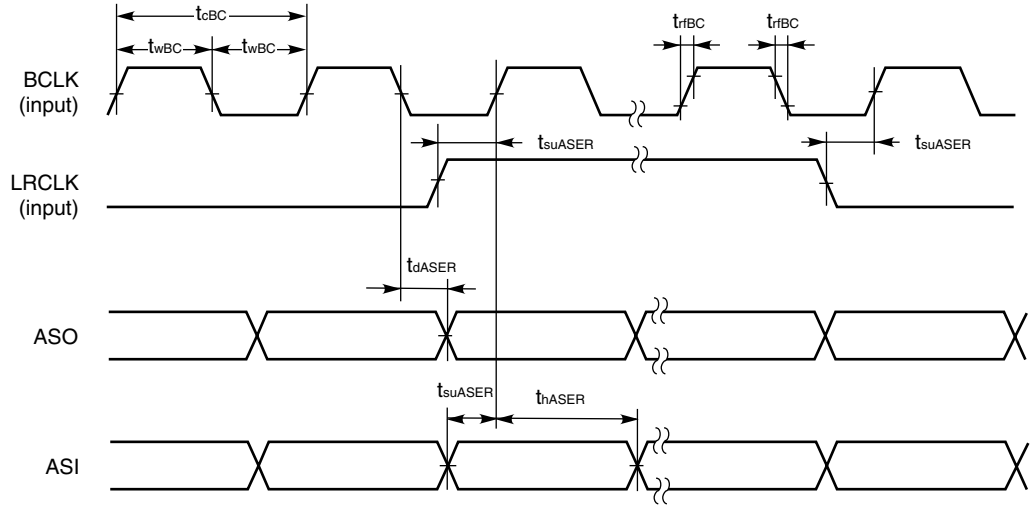
Audio serial clock timing



Audio serial master mode timing

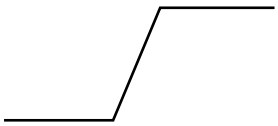


Audio serial slave mode timing



Caution If noise is superimposed on the serial clock, the serial interface may be deadlocked. Bear in mind the following points when designing your system:

- **Reinforce the wiring for power supply and ground (if noise is superimposed on the power and ground lines, it has the same effect as if noise were superimposed on the serial clock).**
- **Shorten the wiring between the device's ASCK, TSCK, BCLK pins, and clock supply source.**
- **Do not cross the signal lines of the serial clock with any other signal lines. Do not route the serial clock line in the vicinity of a line through which a high alternating current flows.**
- **Supply the clock to the ASCK, TSCK, BCLK pins of the device from the clock source on a one-to-one basis. Do not supply clock to several devices from one clock source.**
- **Exercise care that the serial clock does not overshoot or undershoot. In particular, make sure that the rising and falling of the serial clock waveform are clear.**



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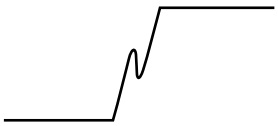
Make sure that the serial clock rises and falls linearly.



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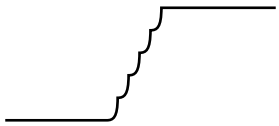
The serial clock must not bound. Noise must not be superimposed on the serial clock.



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The serial clock must not rise or fall step-wise.

SD card Interface (μPD77213 only)

Timing requirements

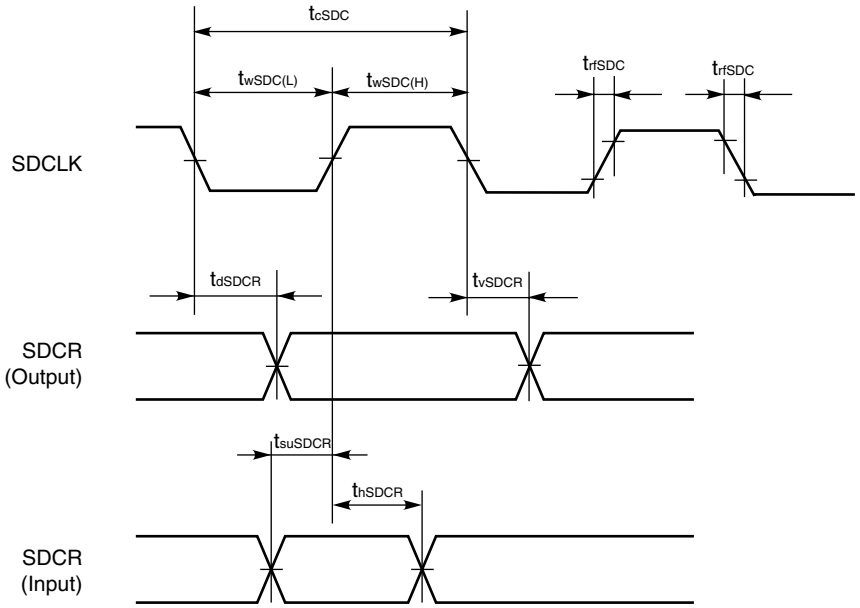
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SDCR input setup time	t_{suSDCR}	Input response	10			ns
SDCR input hold time	t_{hSDCR}	Input response	0			ns
SDDAT input setup time	t_{suSDD}	Input data	10			ns
SDDAT input hold time	t_{hSDD}	Input data	0			ns

Switching characteristics

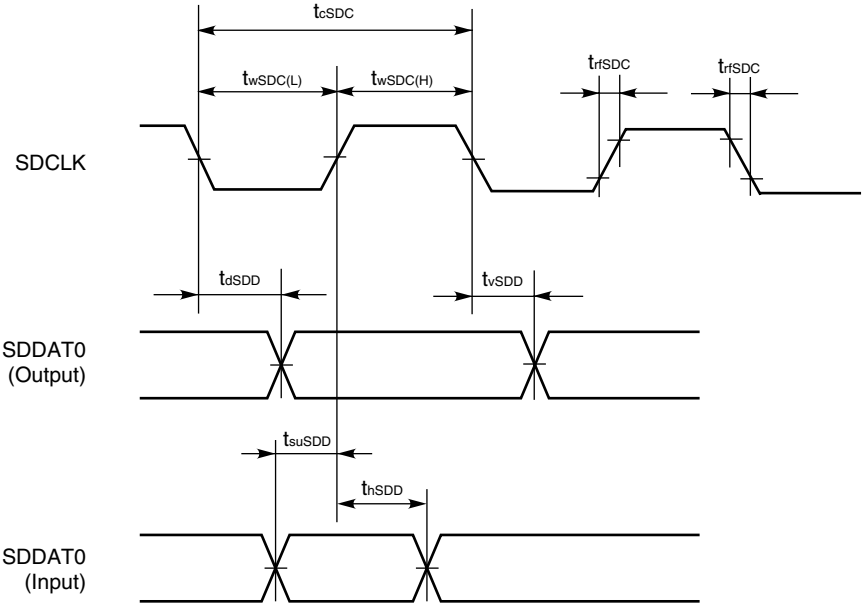
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SDCLK cycle time	t_{cSDC}			n x t_{cC} Note		ns
SDCLK high level width	$t_{wSDC(H)}$			2 t_{cC}		ns
SDCLK low level width	$t_{wSDC(L)}$			t_{cSDC} − $t_{wSDC(H)}$		ns
SDCLK rise/fall time	t_{rfSDC}				5	ns
SDCR output delay time	t_{dSDCR}	Output command			10	ns
SDCR output valid time	t_{vSDCR}	Output command	0			ns
SDDAT output delay time	t_{dSDD}	Output data			10	ns
SDDAT output valid time	t_{vSDD}	Output data	0			ns

Note n:SD card clock division ratio

SDCR timing



SDDAT timing



Remark The SDMON pin functions alternately as the external data memory interface pin MA13. When accessing a peripheral register related to the SD card interface, the SDMON (MA13) pin becomes high level, and the MA0 to MA12 pins become low level. For the timing of these pins, refer to **External Data Memory Access**.

Debugging Interface (JTAG)

Timing requirements

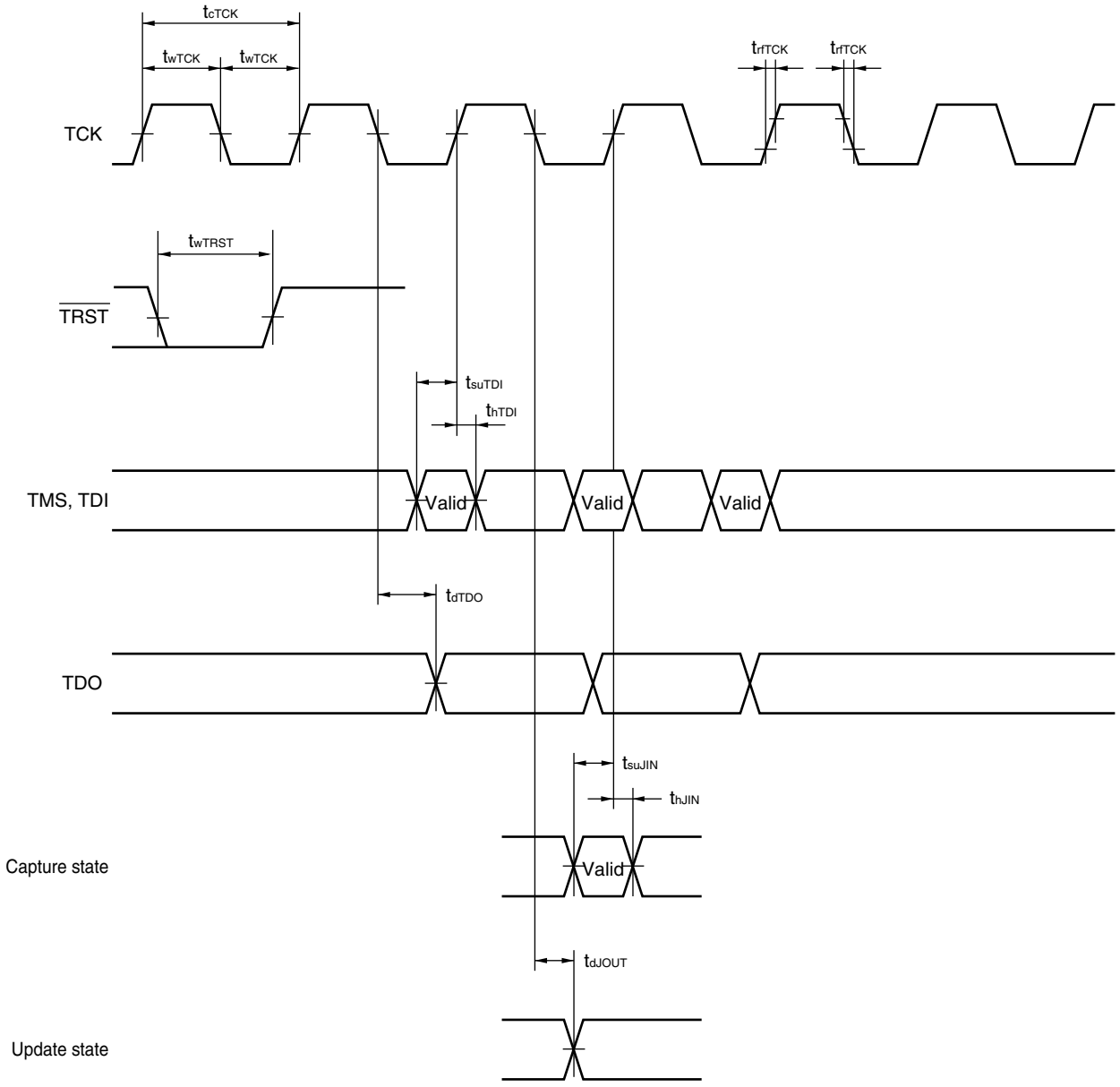
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TCK cycle time	t_{cTCK}		50 and 2 t_{cC} Note			ns
TCK high/low level width	t_{wTCK}		25			ns
TCK rise/fall time	t_{rfTCK}				20	ns
TDI input setup time	t_{suTDI}		12.5			ns
TDI input hold time	t_{hTDI}		12.5			ns
Input pin setup time	t_{suJIN}		12.5			ns
Input pin hold time	t_{hJIN}		12.5			ns
$\overline{\text{TRST}}$ low level width	t_{wTRST}		100			ns

Note When using debugger, the value is 50 and 2 t_{cCX} (MIN.).

Switching characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TDO output delay time	t_{dTDO}		0		17.5	ns
Output pin output delay time	t_{dJOUT}				17.5	ns

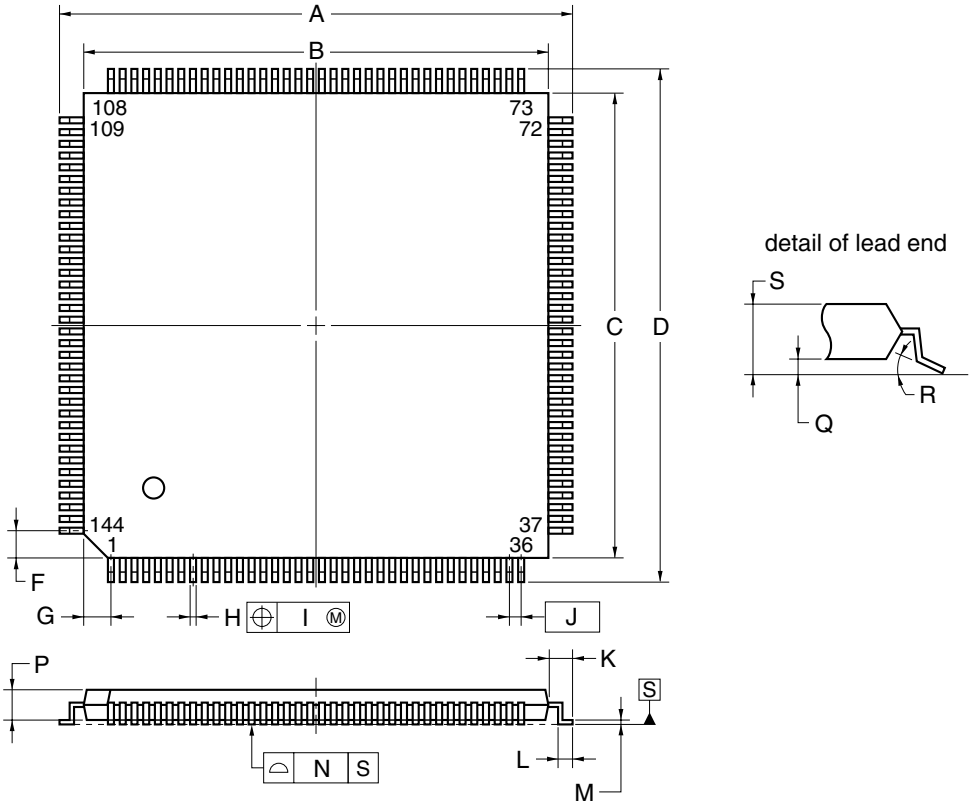
Debugging interface timing



Remark For details of JTAG, refer to **IEEE1149.1**.

11. PACKAGE DRAWINGS

144-PIN PLASTIC LQFP (FINE PITCH) (20x20)



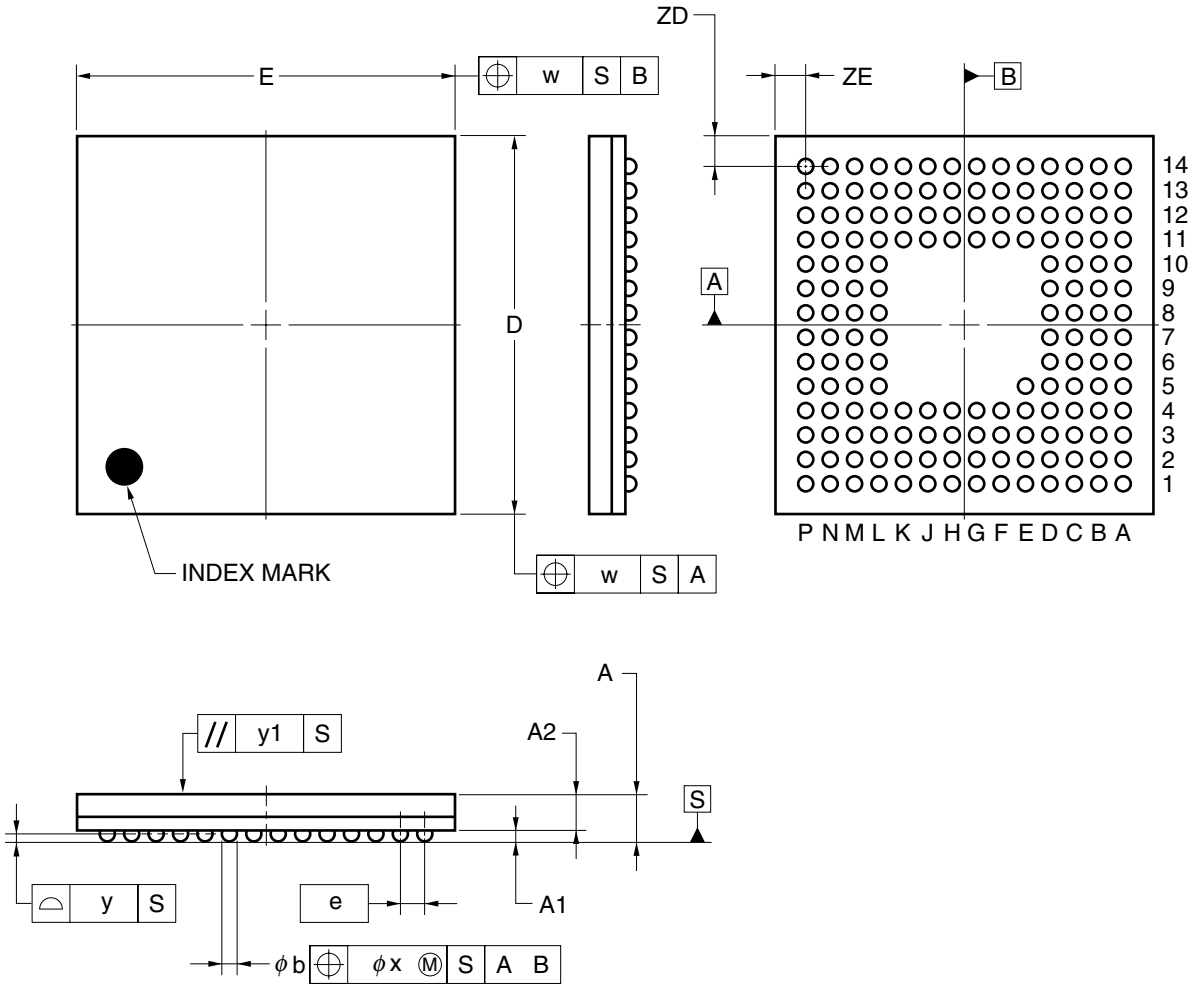
NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	22.0±0.2
B	20.0±0.2
C	20.0±0.2
D	22.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.4±0.05
Q	0.10±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.6 MAX.

S144GJ-50-8EN-1

161-PIN PLASTIC FBGA (10x10)



ITEM	MILLIMETERS
D	10.00±0.10
E	10.00±0.10
w	0.20
A	1.23±0.10
A1	0.30±0.05
A2	0.93
e	0.65
b	0.40±0.05
x	0.08
y	0.10
y1	0.20
ZD	0.775
ZE	0.775

P161F1-65-DA2

★ 12. RECOMMENDED SOLDERING CONDITIONS

The μPD77210 Family should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Surface Mounting Type Soldering Conditions

μPD77210F1-DA2:161-pin plastic fine pitch BGA (10 x 10)
μPD77213F1-xxx-DA2:161-pin plastic fine pitch BGA (10 x 10)

Soldering method	Soldering conditions	Recommended condition symbol
Infrared reflow	Package peak temperature: 235 °C, Time: 30 sec. Max. (at 210 °C or higher). Count: two times or less Exposure limit: 7 days [Note] (after that prebaking is necessary at 125 °C for 10 to 72 hours)	IR35-107-2

μPD77210GJ-8EN:144-pin plastic LQFP (fine pitch) (20 x 20)
μPD77213GJ-xxx-8EN:144-pin plastic LQFP (fine pitch) (20 x 20)

Soldering method	Soldering conditions	Recommended condition symbol
Infrared reflow	Package peak temperature: 235 °C, Time: 30 sec. Max. (at 210 °C or higher). Count: two times or less Exposure limit: 3 days [Note] (after that prebaking is necessary at 125 °C for 10 to 72 hours)	IR35-103-2
Partial heating	Pin temperature: 300 °C Max. , Time: 3 sec. Max. (per pin row)	–

Note After opening the dry pack, store it at 25 °C or less and 65 % RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for the partial heating).

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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J01.2

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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License not needed: μPD77210F1-DA2, μPD77210GJ-8EN

The customer must judge the μPD77213F1-xxx-DA2, μPD77213GJ-xxx-8EN

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