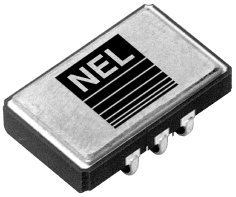
CRYSTAL CLOCK OSCILLATORS

Data Sheet 0208E

Rev. B



LVDS with Tri-State
PJ-A2D00 Series

PRELIMINARY

Description

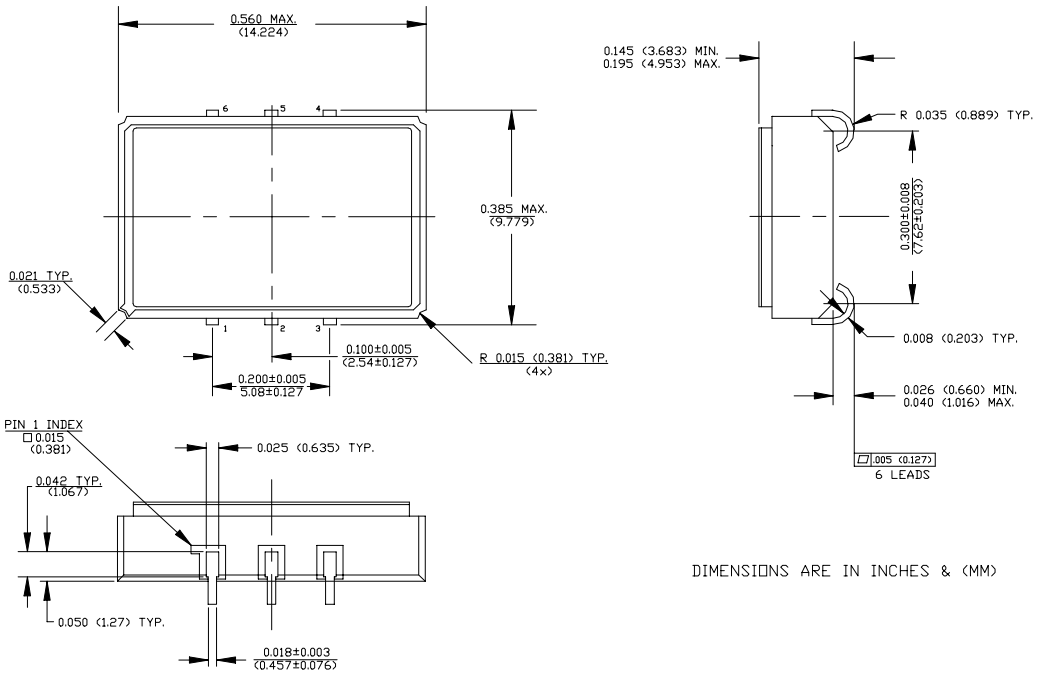
The **PJ-A2D00 Series** of quartz crystal oscillators provide LVDS compatible signals in a ceramic SMD package. Systems designers may now specify space-saving, cost-effective packaged LVDS oscillators to meet their timing requirements.

Features

- Wide frequency range–50.0MHz to 250.0MHz
- User specified tolerance available
- Will withstand vapor phase temperatures of 253°C for 4 minutes maximum
- Space-saving alternative to discrete component oscillators
- High shock resistance, to 3000g
- 3.3 volt operation (other voltages available upon request)
- Metal lid electrically connected to ground to reduce EMI
- Enable/Disable (Tri-state)
- LVDS output on pin 4, complement on Pin 5
- Low Jitter - Wavecrest jitter characterization available
- High Reliability - NEL HALT/HASS qualified for crystal oscillator start-up conditions
- Overtone technology
- High Q Crystal actively tuned oscillator circuit
- Power supply decoupling internal
- No internal PLL avoids cascading PLL problems
- High frequencies due to proprietary design
- Gold plated leads - Solder dipped leads available upon request

Electrical Connection

Pin	Connection
1	N.C.
2	Enable/Disable
3	Ground
4	Output
5	Output Complement
6	V_{CC}



NEL FREQUENCY CONTROLS, INC.

357 Beloit Street, P.O. Box 457, Burlington, WI 53105-0457 U.S.A. Phone 262/763-3591 FAX 262/763-2881
Email: nelsales@nelfc.com www.nelfc.com

PJ-A2D00 Series Continued
LVDS

Rev. B

Operating Conditions and Output Characteristics

Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typical	Max
Frequency	-----	-----	50.0MHz	-----	250.0MHz
Duty Cycle(2)	-----	@ V_O /2	45/55%	-----	55/45%
Logic 0 (2)	V_{OL}	-----	0.80V	-----	1.10V
Logic 1 (2)	V_{OH}	-----	1.25V	-----	1.55V
Differential Voltage (2)	V_{OD}	-----	250 mV	-----	450 mV
Disable Voltage	V_{IL}	-----	GND	-----	0.8V
Enable Voltage	V_{IH}	(or open)	2.0V	-----	V_{CC}
Rise & Fall Time (2)	tr,tf	20-80%V_O	-----	0.8 ns	1.0 ns
Tpd (4)	-----	-----	-0.5 ns	-----	+0.5 ns
Jitter, RMS(3)	-----	-----	-----	-----	3 psec
Enable (Low) voltage	-----	-----	-----	-----	800mV
Disable (High) voltage	-----	-----	2.00V	-----	-----
Frequency Stability (1)	dF/F	Overall conditions including: voltage, calibration, temp., 10 yr aging, shock, vibration	-100ppm	-----	+100ppm

General Characteristics

Parameter	Symbol	Conditions	Min	Typical	Max
Supply Voltage	V_{CC}	-----	3.15V	3.3V	3.45V
Supply Current	I_{CC}	-----	0.0 mA	-----	80 mA
Output current	I_O	Continuous Output Current	0.0 mA	-----	±50.0 mA
Operating temperature	T_A	------	0°C	-----	70°C
Storage temperature	T_S	-----	-55°C	-----	125°C
Power Dissipation	P_D	-----	-----	-----	345 mW
Lead temperature	T_L	Soldering, 10 sec.	-----	-----	300°C
Load	100 ohms across differential outputs				
Start-up time	t_S	-----	-----	2 ms	10 ms

Environmental and Mechanical Characteristics

Mechanical Shock	Per MIL-STD-202, Method 213, Condition E
Thermal Shock	Per MIL-STD-833, Method 1011, Condition A
Vibration	0.060" double amplitude 10 Hz to 55 Hz, 35g's 55Hz to 2000 Hz
Soldering Condition	300°C for 10 seconds
Hermetic Seal	Leak rate less than 1 x 10^{-8} atm.cc/sec of helium

Footnotes:
1) Standard frequency stability (±20,±25,±50ppm & others available)
2) With Load of 100 ohms across differential outputs.
3) Jitter performance is frequency dependent. Please contact factory for full Wavecrest characterization.
4) Tpd is phase shift between the falling edge of pin 4 and the rising edge of pin 5.

Creating a Part Number

PJ - A2D0X - FREQ

Package Code
PJ 6 J Lead SMD

Input Voltage

Code	Specification
A	3.3V
	5V

Tolerance/Performance

0	±100ppm 0-70°C
1	±50ppm 0-70°C
7	±25ppm 0-70°C
9	Customer Specific
A	±20ppm 0-70°C
B	±50ppm -40 to +85°C
C	±100ppm -40 to +85°C

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