DUAL LOW VOLTAGE POWER AMPLIFIER

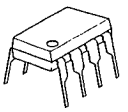
■ GENERAL DESCRIPTION

The NJM2076 is a dual power amplifier, which operates with 1.0V minimum supply voltage. The NJM2076 is suitable to small radio and head-phone of stereo and single BTL application.

■ FEATURES

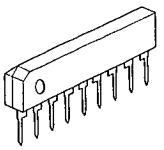
- BTL operation P_O=90mW type.
- Minimum external components
- Headphone stereo Amp. with external transistors
- Low Operation Voltage (1.0V MIN.)
- Low Operating Current (4.7mA TYP.)
- Package Outline DIP8, DMP8, SIP9
- Bipolar Technology

■ PACKAGE OUTLINE



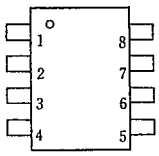
NJM2076D

NJM2076M



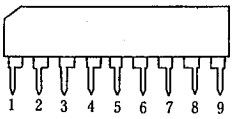
NJM2076S

■ PIN CONFIGURATION



NJM2076D
NJM2076M

PIN FUNCTION
1. Inverting Amp. Input (A)
2. Non-Inverting Amp. Input(B)
3. V^+
4. Base(B)
5. (B) Output
6. GND
7. (A) Output
8. Base (A)



NJM2076S

PIN FUNCTION
1. V^+
2. Base (B)
3. (B) Output
4. Power GND
5. GND
6. (A) Output
7. Base (A)
8. Inverting Amp Input (A)
9. Non-Inverting Amp Input (B)

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■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	4.5	V
Maximum Input Signal	V_{IN}	200	mVrms
Power Dissipation	P_D	(DIP 8) 500 (SIP 9) 500 (DMP 8) 500	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(Ta=25℃, V^+=1.5V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{cc}	Input: Open	—	4.7	7.0	mA
(I) Stereo Configuration (Test Circuit 1. R_L=16Ω)						
Voltage Gain	Av	V_{IN}=10mVrms	26.5	28.0	29.5	dB
Max. Output Power	P_{O1}	THD=10%(S-Type)	15	20.0	—	mW
		THD=10%(D, M-Type)	15	17.5	—	mW
	P_{O2}	THD=10%, V^+=1.0V	—	3	—	mW
Total Harmonic Distortion	THD_1	P_O=1mW (126mVrms/16Ω)	—	0.4	0.8	%
Output Noise Voltage	V_{NO1}	Rg=0, A Curve	—	50	150	μV
Ripple Rejection Ratio	RR_1	Rg=0.f$_R$=1kHz, V_R=30mvrms	25	35	—	dB
Input Resistance	R_{IN}		25	33	43	kΩ
Output Pin Voltage	V_O (DC)		0.62	0.70	0.77	V
(II) BTL Configuration (Test Circuit 2. R_L=8Ω)						
Max. Output power	P_{O3}	THD=10% (S-Type)	75	100	—	mW
		THD=10% (D,M-Type)	75	90	—	mW
	P_{O4}	THD=10%, V^+=1.0V (S-Type)	—	30	—	mW
		THD=10%. V^+=1.0V(D, M-Type)	—	20	—	mW
Total Harmonic Distortion	THD_2	P_O=10mW(283mVrms/8Ω	—	1.5	4.5	%
Output Noise Voltage	V_{NO2}	Rg=0, A Curve	—	85	250	μV
Ripple Rejection Ratio	RR_2	Rg=0, f_R=1kHz, V_R=30mVrms	20	25	—	dB
Voltage Difference between Two Output Pins	ΔV_O(DC)		—	—	50	mV

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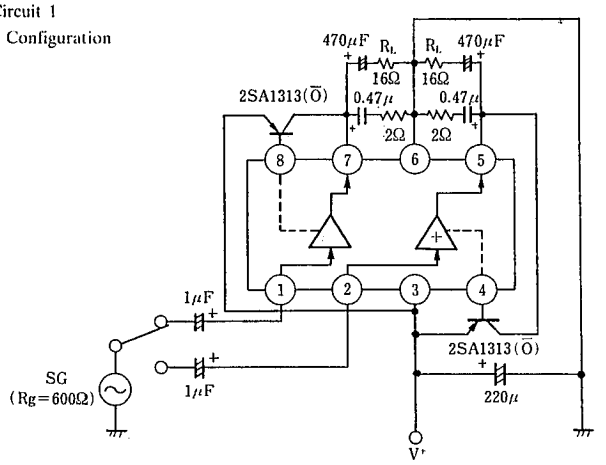
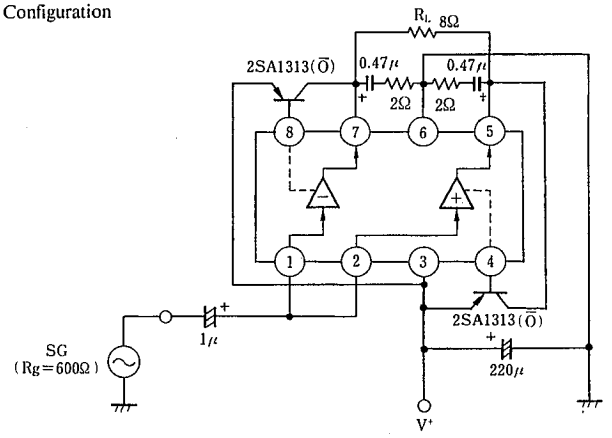
■ TEST CIRCUIT

· Test Circuit 1
Stereo Configuration



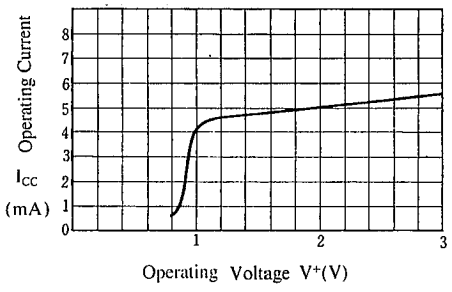
2SA1313(Ō): h_{FE}=115~125
(Ic=100mA)

· Test Circuit 2
BTL Configuration

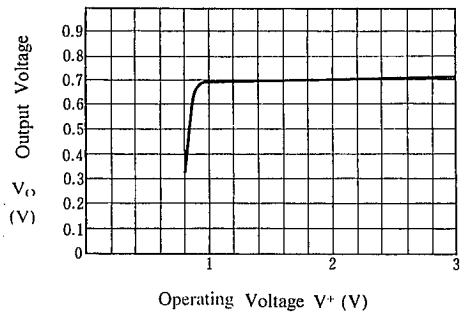


■ TYPICAL CHARACTERISTICS

Operating Current (Test Circuit 1)

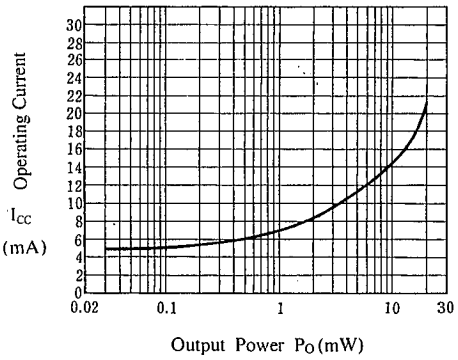


Output Voltage (Test Circuit 1)



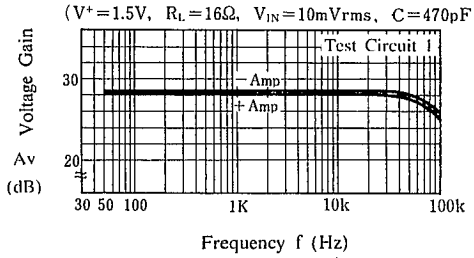
Operating Current (Stereo)

(V^+=1.5V, f=1kHz)



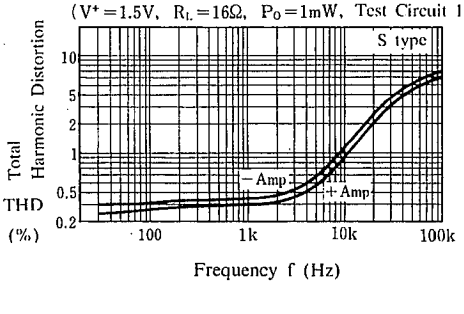
Voltage Gain

(V^+=1.5V, R_L=16Ω, V_{IN}=10mVrms, C=470pF)



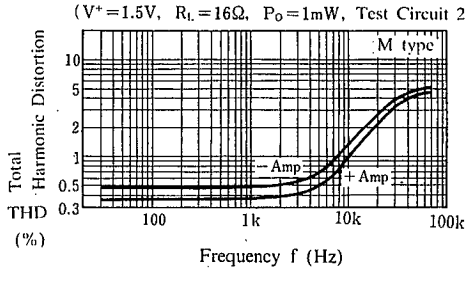
Total Harmonic Distortion (Stereo)

(V^+=1.5V, R_L=16Ω, P_O=1mW, Test Circuit 1



Total Harmonic Distortion (Stereo)

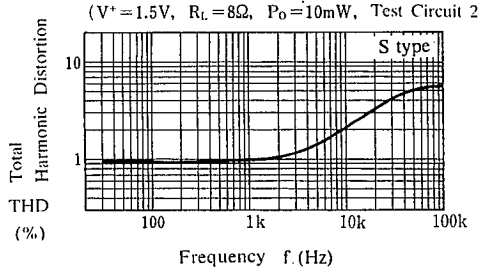
(V^+=1.5V, R_L=16Ω, P_O=1mW, Test Circuit 2



■ TYPICAL CHARACTERISTICS

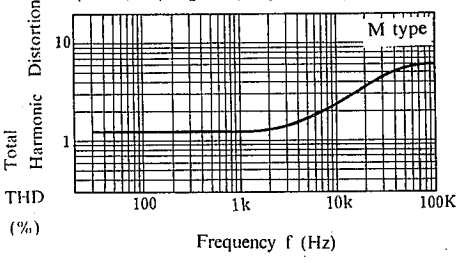
Total Harmonic Distortion (BTL)

(V^+=1.5V, R_L=8Ω, P_O=10mW, Test Circuit 2)



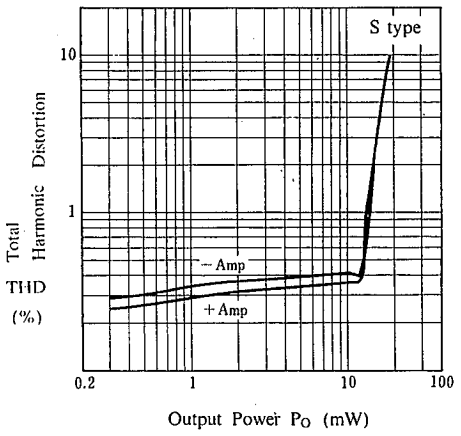
Total Harmonic Distortion (BTL)

(V^+=1.5V, R_L=8Ω, P_O=10mW, Test Circuit 2



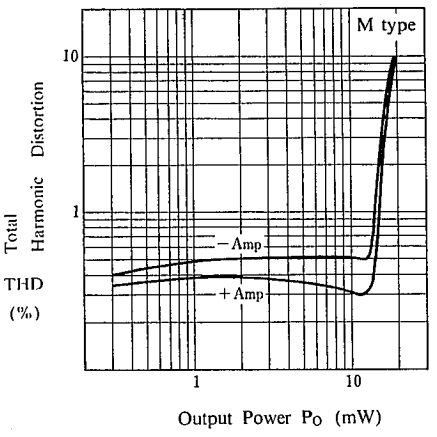
Total Harmonic Distortion (Stereo)

(V^+=1.5V, R_L=16Ω, f=1kHz, Test Circuit 1)



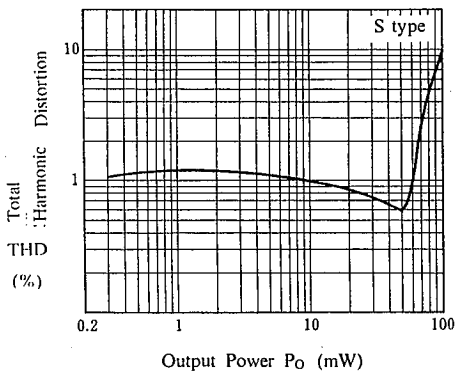
Total Harmonic Distortion (Stereo)

(V^+=1.5V, R_L=16Ω, f=1kHz, Test Circuit 1)



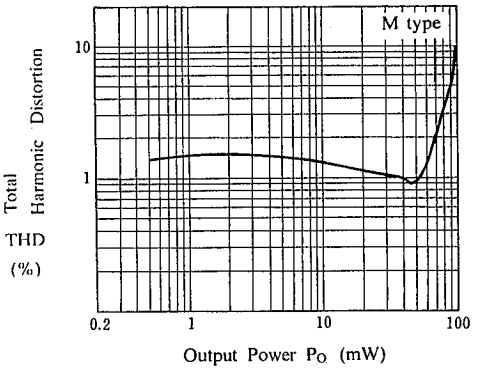
Total Harmonic Distortion (BTL)

(V^+=1.5V, R_L=8Ω, f=1kHz, Test Circuit 2)



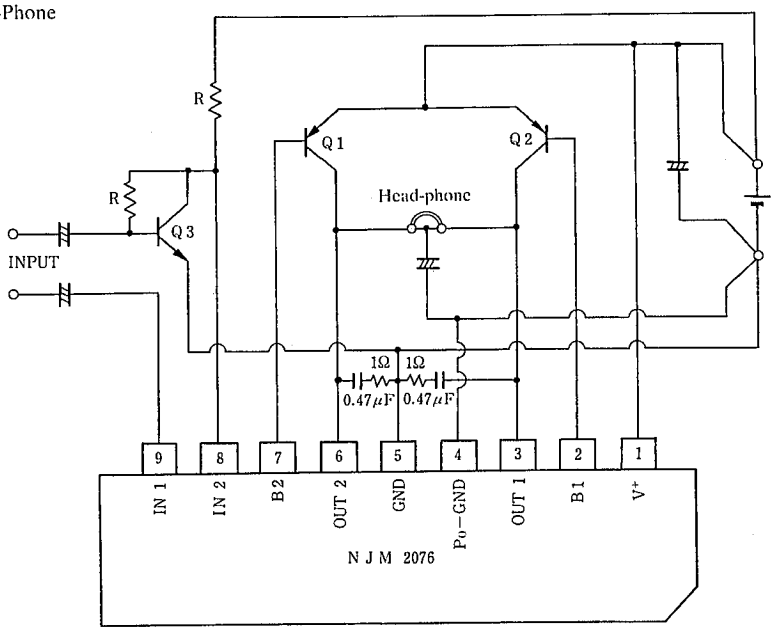
Total Harmonic Distortion (BTL)

(V^+=1.5V, R_L=8Ω, f=1kHz, Test Circuit 2)

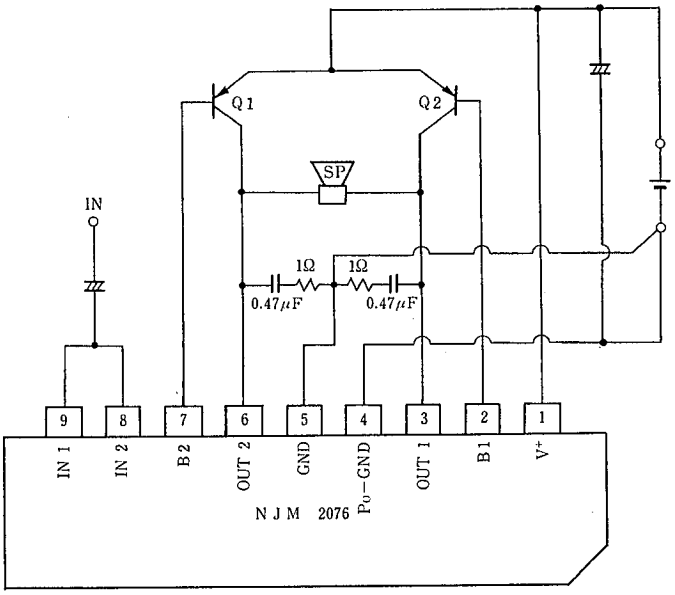


■ TYPICAL APPLICATION

1. For Stereo Head-Phone



2. BTL Amp. for Speaker



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■ NOTICE

(1) External PNP Transistor

Maximum output power becomes large with low saturation voltage transistor, and so select transistor of low saturation.
Saturation Voltage: less than 0.1V (Ic=100mA. I_B=10mA). h_{FE}: 120

(2) External Frequency Compensation

Recommend tantalum capacitor with low tanδ (less than 0.25 at f=10kHz) and 1Ω resistor. Stable with large capacitor of less high frequency distortion and worse tanδ. For example: 1μF, tanδ ≦ 0.6

(3) Layout on PCB

Be careful to get maximum output power and low distortion set.
DIP/DMP: Signal ground has to be close to IC ground pin. Impedance of ground line must be low.
SIP: Two terminals (Power GND, GND) are connected at one point on PCB.

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MEMO

[CAUTION]
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