

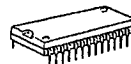
## 4-BIT SINGLE CHIP MICRO CONTROLLER

### ■ GENERAL DESCRIPTION

The **NJU3503** is the C-MOS 4-bit Single Chip Micro Controller consisting of the 4-bit CPU Core, Input / Output Selectable I/O ports, Program ROM, Data RAM, Dual Timer/Counter, 8-bit Serial Interface, 8-bit A/D Converter, and Oscillator Circuit (CR or Ceramic or X'tal). It realizes the control for home appliances or toys by only few external components.

The **NJU3503** is suitable for battery operated appliances because of low operating current, wide operating voltage range, and STANDBY function (HALT mode).

### ■ PACKAGE OUTLINE



NJU3503L



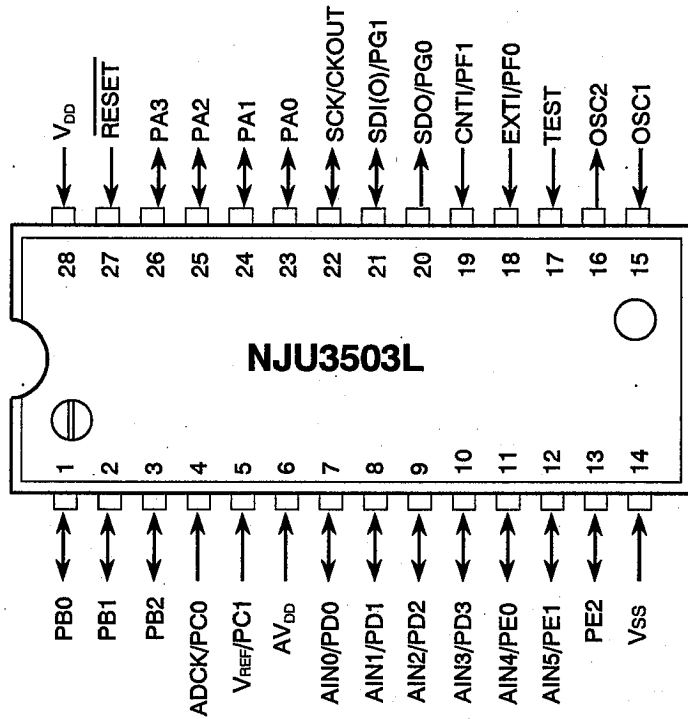
NJU3503M

### ■ FEATURES

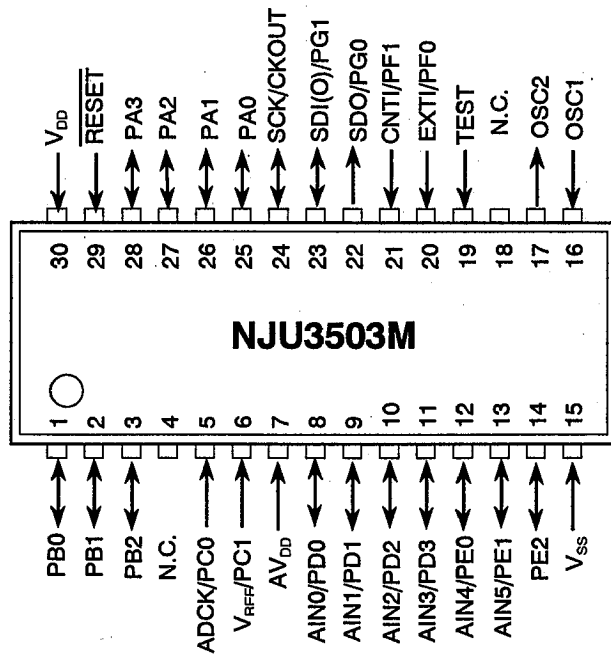
- Internal Program ROM 2048 X 8 bits
- Internal Data RAM 128 X 4 bits
- Input / Output Port 20 lines(MAX) / NJU3503L
- 12 lines ··· Input / Output direction of each bit is selected by the mask option.
  - 8 lines ··· Input / Output direction of each bit can be changed by the program.
- Additional functions by the mask option.
  - External Interrupt Terminal : EXTI/PF0
  - External Clock Input Terminal for Timer2 : CNTI/PF1
  - Serial Interface Terminals : SDO/PL0, SDI(O)/PG1
  - A/D Converter Interface Terminals : ADCK/PC0, VREF/PC1, AIN0~3/PD0~3, AIN4~5/PE0~1
- High Output-Current terminal (11 lines) : PA0~PA3, PD0~PD3, PE0~PE2
- N-Channel FET Open Drain Type (IoL) 15mA at V<sub>DD</sub>=5V
- Instruction Set 59 instructions
- Subroutine Nesting 8 levels
- Pulse Edge Detector
  - The rising or falling edge of a pulse is selected by the mask option.
- Instruction Executing Time 6/f<sub>osc</sub> sec (1.5 μ sec at 4MHz)
- Operating Frequency Range 30kHz to 4MHz
- Internal Oscillator
  - CR, or Ceramic, or X'tal oscillation and External clock input
- STANDBY function (HALT mode)
- Wide operating voltage range 2.4V to 5.5V
- 8-bit Serial Input / Output port
- Timer/Counter
  - (Timer1 : 8-bit re-load type timer,
  - Timer2 : 8-bit re-load type timer event counter )
  - (Count clock : Timer1's clock is an internal one.
  - Timer2's clock is an internal or external one.)
- 8-bit A/D converter (Multiplexed 6-channel input )
- Interrupt factor 4 (external, timer1, timer2, serial Input / Output)
- C-MOS technology
- Package outline SDIP28 / SDMP30

## ■ PIN CONFIGURATION

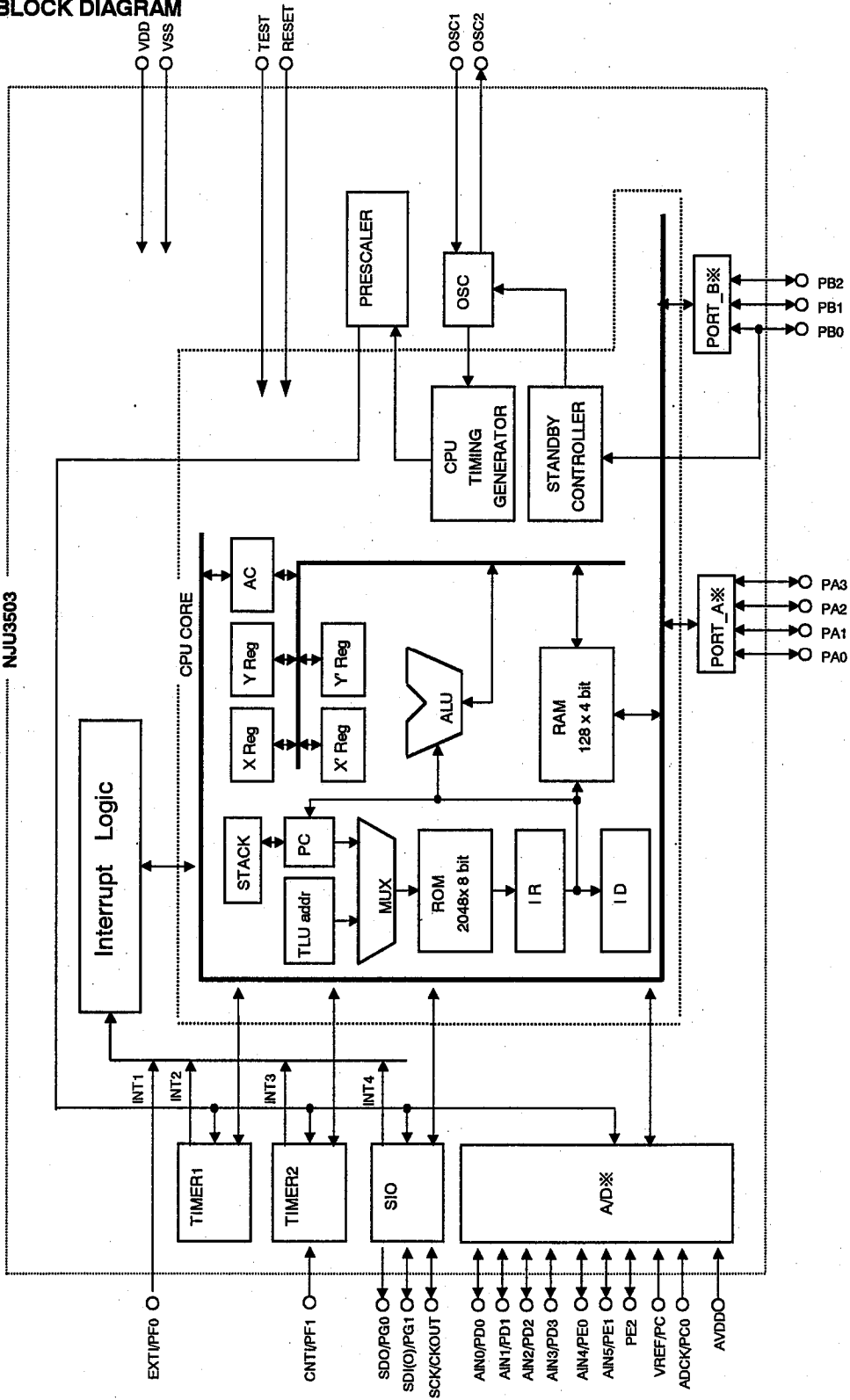
SDIP28



SDMP30



## ■ BLOCK DIAGRAM



※ Refer ■ INPUT/OUTPUT TERMINAL TYPE

## ■ TERMINAL DESCRIPTION 1

No.		SYMBOLS	INPUT/OUTPUT	FUNCTIONS
NJU 3503M	NJU 3503L			
1	1	PB0	INPUT/OUTPUT	3-bit Input / Output PORTB. Selects a terminal circuit for each port from follows by the mask option. <ul style="list-style-type: none"> <li>•C-MOS Schmitt Trigger Input Terminal with Pull-up Resistance (ISP)</li> <li>•C-MOS Schmitt Trigger Input Terminal (IS)</li> <li>•C-MOS Output Terminal (OC)</li> </ul> When the ports are selected as the input terminal, PB0 operates also as RESTART signal input terminal to return from STANDBY mode, and PB1 operates also as the Edge Detector Terminal.
2	2	PB1	INPUT/OUTPUT	
3	3	PB2	INPUT/OUTPUT	
5	4	ADCK / PC0	INPUT	2-bit Input PORTC. Selects a function of either of 1) or 2) for PORTC by the mask option. 1) Input terminal for A/D Converter. External Clock Input Terminal : ADCK (ACP,AC) Reference Voltage Input Terminal : V <sub>REF</sub> (AD)  2) 2-bit Input Terminals as PORTC. Selects a terminal circuit for each port from follows by the mask option. <ul style="list-style-type: none"> <li>•C-MOS Schmitt Trigger Input Terminal with Pull-up Resistance (ISP)</li> <li>•C-MOS Schmitt Trigger Input Terminal (IS)</li> </ul>
6	5	V <sub>REF</sub> / PC1	INPUT	
7	6	AV <sub>DD</sub>	—	Analog Block Power source Connect to V <sub>DD</sub> terminal when A/D converter is not used.
8	7	AIN0 / PD0	AIN0 to AIN3: INPUT  PD0 to PD3: INPUT/OUTPUT	4-bit Input PORTD. Selects a function of either of 1) or 2) for PORTD by the mask option. 1) 4-bit Analog Input to A/D Converter. (AD)  2) 4-bit Input / Output Terminals as PORTD. Selects a terminal circuit for each port from follows by the mask option. <ul style="list-style-type: none"> <li>•C-MOS Input Terminal with Pull-up Resistance (ICP)</li> <li>•C-MOS Input Terminal (IC)</li> <li>•Nch-FET Open-Drain Output Terminal with Pull-up Resistance (ONP)</li> <li>•Nch-FET Open-Drain Output Terminal (ON)</li> </ul>
9	8	AIN1 / PD1		
10	9	AIN2 / PD2		
11	10	AIN3 / PD3		

Note )      INPUT/OUTPUT : Input or Output is selected by the mask option.  
               INOUT                : Input or Output is changed by the program.

## ■ TERMINAL DESCRIPTION 2

No.		SYMBOL	INPUT/OUTPUT	FUNCTIONS
NJU 3503M	NJU 3503L			
12 13 14	11 12 13	AIN4 / PE0 AIN5 / PE1 PE2	AIN4, AIN5: INPUT  PE0 to PE2: INPUT/OUTPUT	3-bit Input / Output PORTE. Selects a function of either of 1) or 2) for PORTE by the mask option. 1) 2bit Analog Input to A/D Converter. : AIN4,AIN5 (AD) 2) 3-bit Input / Output Terminals as PORTE. Selects a terminal circuit for each port from follows by the mask option. <ul style="list-style-type: none"> <li>•C-MOS Input Terminal with Pull-up Resistance (ICP)</li> <li>•C-MOS Input Terminal (IC)</li> <li>•Nch-FET Open-Drain Output Terminal with Pull-up Resistance (ONP)</li> <li>•Nch-FET Open-Drain Output Terminal (ON)</li> </ul>
15	14	V <sub>SS</sub>	–	Power Source ( 0V )
16 17	15 16	OSC1 OSC2	INPUT OUTPUT	Internal Oscillator Terminals. Connects a device selected from the ceramic or the crystal resonator, or the resistor, to these terminals for the internal oscillator. In the external clock operation, OSC1 is the external clock input terminal and OSC2 is normally open terminal.
19	17	TEST	INPUT	Maker Testing Terminal with Pull-down Resistance The terminal is recommended to connect to GND.
20 21	18 19	EXTI / PF0 CNT1 / PF1	INPUT INPUT	2-bit Input PORTF. Selects a function of either of 1) or 2) for PORTF by the mask option. 1) External Interrupt Input Terminal with Pull up resistance :EXTI ( IIP,II, P / F ) External Clock Input Terminal with Pull up resistance for Timer2 :CNT1 (IIP,II) 2) 2-bit Input Terminals as PORTF. Selects a terminal circuit for each port from follows by the mask option. <ul style="list-style-type: none"> <li>•C-MOS Schmitt Trigger Input Terminal with Pull-up Resistance (ISP)</li> <li>•C-MOS Schmitt Trigger Input Terminal (IS)</li> </ul>
22 23	20 21	SDO / PG0 SDI(O)/ PG1	SDO :OUTPUT PG0 :OUTPUT  SDI(O) :INOUT PG1 : INPUT/OUTPUT	2-bit Input / Output PORTG. Selects a function of either of 1) or 2) for PORTG by the mask option. 1) Serial Interface Function Serial Data Output Terminal : SDO (SO) Serial Data Input-Output Terminal with Pull-up Resistance : SDI(O) (SDP) 2) 2-bit Input / Output Terminals as PORTG. Selects a terminal circuit for each port from follows by the mask option. <ul style="list-style-type: none"> <li>•C-MOS Input Terminal with Pull-up Resistance (ICP):PG1</li> <li>•C-MOS Input Terminal (IC) : PG1</li> <li>•C-MOS Output Terminal (OC) : PG0,PG1</li> </ul>

Note ) INPUT/OUTPUT : Input or Output is selected by the mask option.  
INOUT : Input or Output is changed by the program.

## ■ TERMINAL DESCRIPTION 3

No.		SYMBOL	INPUT/OUTPUT	FUNCTIONS
NJU 3503M	NJU 3503L			
24	22	SCK/CKOUT	SCK :INOUT CKOUT: OUTPUT	Selects a function of either of 1) or 2) by the mask option. 1) Serial Clock Input or Output Terminal with Pull-up Resistance. : SCK (SCP)  2) Clock Divided by Pre-scaler Output Terminal. Selects the dividing times of the clock in the pre-scaler by the mask option. : CKOUT
25 26 27 28	23 24 25 26	PA0 PA1 PA2 PA3	INOUT INOUT INOUT INOUT	4-bit Programmable Input / Output PORTA. These 4-bit terminals direction can be changed by the program as each terminal of Input or Output. Use of Pull-up resistance for a terminal is in accordance with the mask option.(IOP,IO) •as Input : C-MOS Input Terminals •as Output: Nch-FET Open-Drain Output Terminals
29	27	$\overline{\text{RESET}}$	INPUT	RESET Terminal. When the low level input-signal, the system is initialized.
30	28	V <sub>DD</sub>	—	Power Source (2.4V to 5.5V)

Note ) INPUT/OUTPUT : Input or Output is selected by the mask option.  
 INOUT : Input or Output is changed by the program.  
 "IOP,IO,AD,ICP,ONP,ON,OC,ISP,IS,AD,P,F,IIP,II,SO,SCP,CKOUT" are symbols using on MASK OPTION GENERATOR(MOG).

## ■ INTERNAL SYSTEM DESCRIPTION

The NJU3503 is a C-MOS 4-Bit Single Chip Micro Controller consisted of Original CPU Core, Selectable Input-Output(I/O) Ports(MAX. 20 lines), Program ROM(2048 bytes), Data RAM(128 nibbles), 8-Bit A/D Converter, 8-bit Serial Interface, Dual 8-Bit Timer/Counter, Interrupt Control Circuit and Oscillator Circuit.

The CPU block in the NJU3503 is consisted of ALU(Arithmetic Logic Unit) executing the binary adding, subtracting or logical calculating, AC(Accumulator), four Registers, STACK allowing the 8-level subroutine-nesting or Interrupt operation, Program Counter indicating 2048 addresses sequentially, and Timing generator.

The NJU3503 can be applied to the various markets because of the rich and efficient instruction set(59 instructions), wide operating voltage range(2.4V to 5.5V), low operating current, and STANDBY function reducing the power supply current.

### (1) INTERNAL REGISTER

#### ● Accumulator(AC)

Accumulator(AC) is structured by the 4-bit register. It holds a data or a result of calculation, and executes the shift-operation (ROTATE) or the data transference between the other registers and Data Memory (RAM).

The accumulator condition is unknown on the "RESET" operation.

#### ● X-register(X-reg)

X-register(X-reg) operates as the 4-bit register. Bit0 and bit1 of X-reg operates also as the RAM address pointer with Y-register.

The X-reg condition is unknown on the "RESET" operation.

#### ● Y-register(Y-reg)

Y-register(Y-reg) operates as the 4-bit register or the RAM address pointer with X-reg.

The Y-reg condition is unknown on the "RESET" operation.

#### ● X'-register(X'-reg)

X'-register(X'-reg) operates as the 4-bit register or a part of Program Memory(ROM) address pointer for looking data in the ROM(TRM instruction) up function.

The X'-reg condition is unknown on the "RESET" operation.

#### ● Y'-register(Y'-reg)

Y'-register(Y'-reg) operates as the 4-bit register or the peripheral register number(PHYn) pointer.

The Y'-reg condition is unknown on the "RESET" operation.

### (2) INTERNAL FLAG

#### ● RPC flag(RPC)

RPC flag(RPC) changes the instruction table. Several instructions perform either of the dual tasks in accordance with the RPC flag condition. The RPC flag condition selects either of two couples of registers which are X- and Y- reg, or X'- and Y'-reg. X- or Y- reg is selected when the RPC flag condition is "0"(RPC=0). X'- or Y'- reg is selected when the RPC flag condition is "1"(RPC=1). The RPC flag condition is set to "1"(RPC=1) by SRPC instruction, and is set to "0"(RPC=0) by RRPC instruction.

The RPC flag condition is set to "0" on the "RESET" operation.

#### ● CARRY flag(CY)

When the carry occurs after the adding calculation, the CARRY flag(CY) condition is set to "1"(CY=1), and when no carry, the CY flag condition is set to "0"(CY=0). When the borrow occurs after the subtracting calculation, the CY flag condition is set to "0"(CY=0), and when no borrow, the CY flag condition is set to "1"(CY=1). The bit-operation instruction operates the bit data rotation on the CY flag combined with the accumulator or the other register.

The CY flag condition is set to "1"(CY=1) by SEC instruction and is set to "0"(CY=0) by CLC instruction. The CY flag condition is kept until the end of the next instruction executing cycle. The CY flag condition is unknown on the "RESET" operation.

● STATUS flag(ST)

STATUS flag(ST) is the conditional flag in accordance with the result of the instruction execution. Its condition is in accordance with follows:

- 1) to be same as CY flag condition.
- 2) to be set the condition to "0"(ST=0) when the result of the logical calculation(AND, OR, XOR, YNEA) is zero.
- 3) to be set the condition to "0"(ST=0) when the result of the comparison(CMP) is zero.

However, ST flag condition is always set to "1"(ST=1) except above three.

ST flag controls the branch operation. Branch instruction does not branch when ST flag condition is "0", and branches when ST flag condition is "1". ST flag condition is kept until the end of the next instruction executing cycle.

The ST flag condition is unknown on the "RESET" operation.

(3) FUNCTIONAL BLOCK

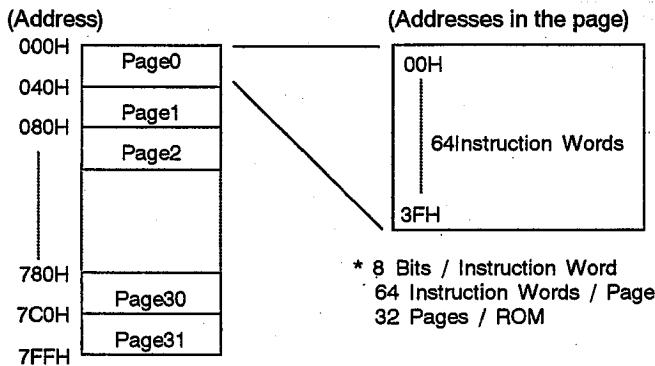
● ARITHMETIC LOGIC UNIT(ALU)

ARITHMETIC LOGIC UNIT(ALU) is a 4-bit binary paralleled calculation circuit operating binary addition, binary subtraction, comparison, logical AND, logical OR, exclusive OR, and SHIFT(Rotation). And it also can detect CARRY, BORROW or ZERO in accordance with the result of each calculation.

● PROGRAM MEMORY(ROM)

PROGRAM MEMORY(ROM) consists of 32 pages, and a page consists of 64 bytes memory capacity. Therefore the NJU3503 prepares the 2048-byte ROM for the application program. The ROM address is indicated by the Program Counter(PC).

[PROGRAM MEMORY AREA]

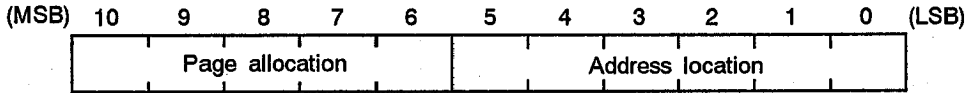




●PROGRAM COUNTER(PC)

PROGRAM COUNTER(PC) consisted of the 10-bit binary counter stores the address for the next operating instruction in ROM. Data figures limited from b0 to b5 on the PC indicate the address in a page, and data figures limited from b6 to b10 on the PC indicate the page in a bank. Although the ROM address can be indicated 2048 addresses continuously, the target address of JMP instruction is restricted by Paging structure in ROM. The target address of JPL or CALL instruction is restricted by Banking structure in ROM.

The PC condition is set to "0" on the "RESET" operation.



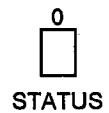
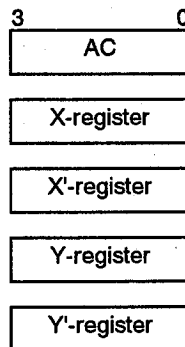
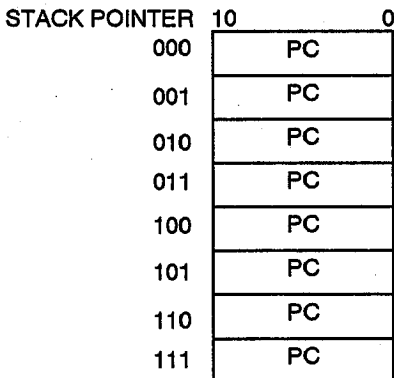
JMP instruction can branch to the optional address in the page. The target address is indicated by the data figures limited from b0 to b5 (6bits) on PC as shown in above. The paging structure can reduce the program size in ROM and the JMP instruction execution time against JPL instruction because JMP instruction is consisted of one byte (8bits) length. JPL and CALL instructions can branch to the optional address without considering the paging structure, because they consist of two bytes (16bits) length including the 11 bits of PC.

●STACK

STACK consists of three types of registers which are the 8 by 11 bits, the 5 by 4 bits, and the 2 by 1 bit registers. The registers of STACK hold the data of PC automatically when the interrupt routine or the subroutine is called. The 5 by 4 bits registers of STACK hold the data of the internal registers automatically when the interrupt operation is executed. The 2 by 1 bit registers of STACK hold the data of the internal flag automatically when the interrupt operation is executed. In the return (RET or RETI) operation, PC, the internal registers, and the internal flags registers get the held data from STACK automatically.

[ For branch(CALL) and interrupt operation ]

[ For interrupt operation ]



● **STACK POINTER(SP)**

STACK POINTER(SP) consists of the 3 bits binary counter. SP indicates the number of next operating position in the STACK. It counts one up(increment) after the subroutine call(CALL) or the interrupt operation, and it counts one down(decrement) after the return(RET or RETI) operation.

Data storing operation to STACK after that SP overflowed (over than 7) or underflowed(under than 0), breaks the former held data in STACK. Therefore the subroutine nesting level must be cautioned in the application program.

SP condition is set to "0" on "RESET" operation.

● **DATA MEMORY(RAM)**

DATA MEMORY(RAM) is formed with the 4-bit length a word. The NJU3503 prepares 128 words(512 bits) RAM. The data formed with the 4-bit length a word can be read/written from/to RAM, and the data formed with the 1-bit length in a word can be set, reset, or tested by the bit-operation instruction.

The RAM address is indicated indirectly by X-reg and Y-reg. The lower 3 bits(b0,b1,b2) in X-reg are used as the RAM address pointer and higher a bit (b3) is not used.

[ RAM ADDRESS MAP ]

Y-reg →	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	[HEX]
0																	
1																	
2																	
3																	
4																	
5																	
6																	
7																	
[HEX] ↑																	
X-reg																	

● PERIPHERAL REGISTERs(PH)

PERIPHERAL REGISTERs(PH) controlling I/O Ports or the ROM address are selected by the data in Y'-reg.

Two Peripheral Register tables called as table0 and table1 in the NJU3503 consist of 32 registers totally.

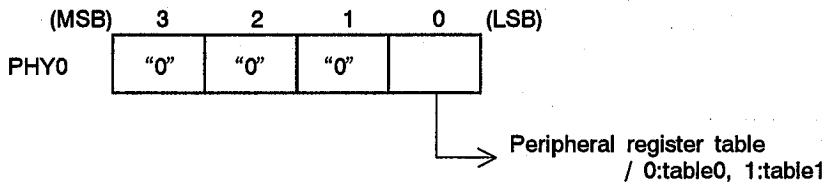
The Peripheral Register assigned for each I/O Port can get the signal data from the external application by reading operation, or can output the signal data to the external application by writing operation in accordance with the type of input or output selected by the mask option. Although the data can be read from the Peripheral Register assigned as the Output, it sometimes takes the incorrect data of the Output Port.

《Peripheral Register Table Change》

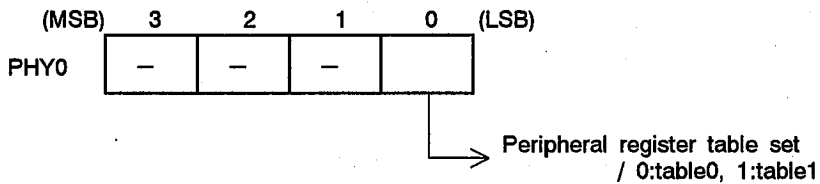
When LSB(b0) of the peripheral register table change register(PHY0) is written "0", the table0 is selected. When LSB of PHY0 is written "1", the table1 is selected.

The table0 is selected on "RESET" operation.

[ Reading from the Peripheral Register Table Change Register (PHY0) ]



[ Writing to the Peripheral Register Table Change Register (PHY0) ]



**[ PERIPHERAL REGISTER TABLE0 ]**

Y'-register	Register No.	Peripheral Register Name	Number of Port	Write or Read ※1	Data in Reset
0H	PHY0	Peripheral Register Table Change Register	1	WR	0
1H	PHY1	Serial Input/Output Control Register	3	WR	0 ※2
2H	PHY2	Serial Input/Output Shift Register	8	WR	0 ※2
3H	PHY3	Timer1/Pre-scaler Control Register	3	WR	0
4H	PHY4	Initial Value Register1 / Timer Counter1	8	WR	0
5H	PHY5	Timer2 Control Register	4	WR	0 ※5
6H	PHY6	Initial Value Register2 / Timer Counter2	8	WR	0
7H	PHY7	A/D Converter Control Register	4	WR	0 ※3
8H	PHY8	A/D Converter Control Register	1	WR	0 ※3
9H	PHY9	A/D Converter Output Register	8	R	0 ※3
AH	PHY10	Interrupt Control Register	4	WR	0 ※5
BH	PHY11				
CH	PHY12				
DH	PHY13	ROM Addressing Register	3	WR	unknown
EH	PHY14				
FH	PHY15				

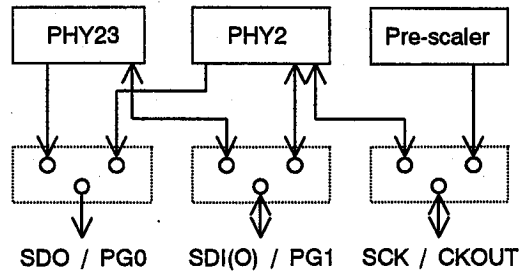
**[ PERIPHERAL REGISTER TABLE1 ]**

Y'-register	Register No.	Peripheral Register Name	Number of Port	Write or Read ※1	Data in Reset
0H	PHY0	Peripheral Register Table Change Register	1	WR	0
1H	PHY17	PORTA Output or PORTA Input	4	WR	0
2H	PHY18	PORTB Output or PORTB Input	3	W / R	0
3H	PHY19	PORTC Input	2	R	0 ※4
4H	PHY20	PORTD Output or PORTD Input	4	W / R	0 ※3
5H	PHY21	PORTE Output or PORTE Input	3	W / R	0 ※3
6H	PHY22	PORTF Input	2	R	0 ※5
7H	PHY23	PORTG Output or PORTG Input	2	W / R	0 ※2
8H	PHY24	Programmable Input/Output Port Control Register	4	WR	0
9H	PHY25				
AH	PHY26				
BH	PHY27				
CH	PHY28				
DH	PHY29				
EH	PHY30				
FH	PHY31				

※1 W : Write only  
 R : Read only  
 WR : Read and Write  
 W / R : Fixed as Read or Write by the mask option

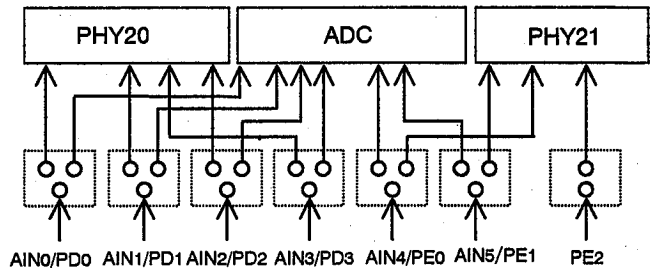
※2 Wiring of terminals

The mask option selects a terminal type from SDO/PG0, SDI(O)/PG1 or SCK/CKOUT as shown in right.



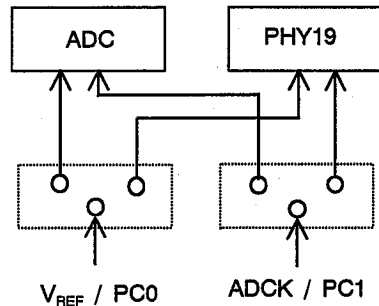
※3 Wiring of terminals

The mask option selects a terminal type from AIN0/PD0, AIN1/PD1, AIN2/PD2, AIN3/PD3, AIN4/PE0, AIN5/PE1, PE2 as shown in right.



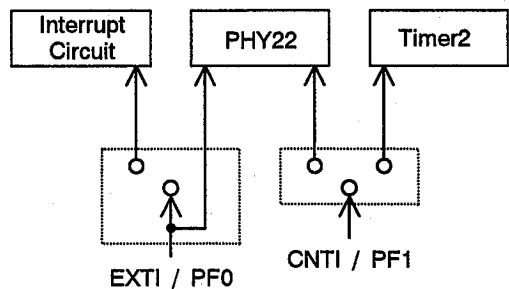
※4 Wiring of terminals

The mask option selects a terminal type from V<sub>REF</sub>/PJ0, or ADCK/PJ1 as shown in right.



※5 Wiring of terminals

The mask option selects a terminal type from EXTI/PF0, or CNTI/PF1 as shown in right.



● ROM ADDRESSING REGISTER(PHY13)

ROM ADDRESSING REGISTER (PHY13) indicates the address of ROM with Accumulator and X-reg for the data transference operation (TRM) from ROM to RAM.

The PHY13 condition are unknown on "RESET" operation. The lower 3 bits(b0,b1,b2) in PHY13 are used as the ROM ADDRESSING and higher a bit(b3) is not used,

[ ROM ADDRESSING ]

no used	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
b3	b2	b1	b0	b3	b2	b1	b0	b3	b2	b1	b0
PHY13				X'				AC			

## INPUT OUTPUT PORT

The NJU3503 prepares 8 Input-Output lines and 12 dual-function lines for the interface to an external application circuit. All lines are assigned to each Peripheral Register.

Data reading operation from the peripheral register can input the actual signals through the input terminal. Data writing operation to the peripheral register can output the actual signals through the output terminal.

[ PORT FUNCTION TABLE ]

PORT NAME	FUNCTION	INPUT/OUTPUT
PORTA	Input / Output port	Programmable Input / Output PORT(4-bit).
PORTB	Input / Output port	Input / Output selectable ports by the mask option.
PORTC(PC0)	Input port or ADCK	Input
PORTC(PC1)	Input or V <sub>REF</sub>	Input
PORTD	Input / Output port or AIN0 to AIN3	Input / Output selectable ports by the mask option
PORTE(PE0,PE1)	Input / Output port or AIN4 to AIN5	Input / Output selectable ports by the mask option.
PORTE(PE2)	Input / Output port	Input / Output selectable ports by the mask option.
PORTF(PF0)	Input port or EXTI	Input
PORTF(PF1)	Input port or CNTI	Input
PORTG(PG0)	Output Port or SDO	output
PORTG(PG1)	Input / Output port or SDI(O)	Input / Output selectable ports by the mask option.

Note1) Pull-up resistance is selected by the mask option.(refer ■INPUT OUTPUT TERMINAL TYPE)

### (1) INPUT OUTPUT PORT

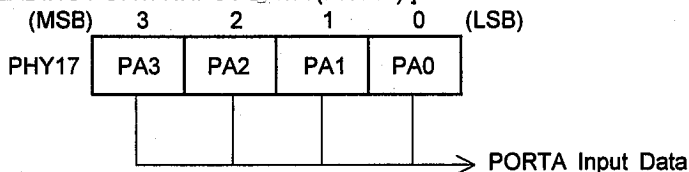
#### ●PORTA(PA0 to PA3)

PORTA is a 4-bit programmable input-output PORT. The input or the output is selected for each bit by the programmable input/output control register (PHY24). It is set to "1" as the output, and is set to "0" as the input. When the PORT is set as the output, the 4-bit signals are output through the output terminals by writing data into the peripheral register assigned for PORTA (PHY17). PHY17 as the output register should be written the output data before the PORTA is set as the output by PHY24, because the conditions of the output terminals are unknown while the output data is not written in PHY17. When this PORT is set as the input, the 4-bit external signals are gotten directly through the input terminals by reading data from PHY17. PHY17 can be written or read independent of the state of PHY24 as the input or output.

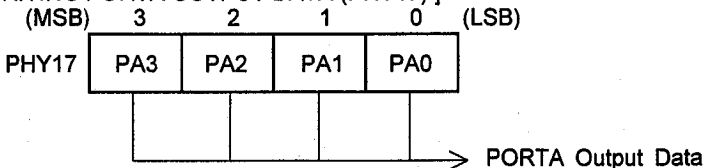
Though the output circuit is Nch open drain type, the C-MOS input buffer is connected to the same terminal. Therefore, the operating current of the chip by the short circuit current when the middle level voltage between V<sub>DD</sub> and V<sub>SS</sub> is input to this terminal.

PORTA is set as the input in accordance with the state of PHY24 set to "0" on the "RESET" operation.

[ READING PORTA INPUT DATA (PHY17) ]



[ WRITING PORTA OUTPUT DATA (PHY17) ]



●PORTB(PB0 to PB2)

PORTB is a 3-bit input-output PORT. The input or the output is selected for each bit by the mask option. When the port is set as the output, the signal is output through the output terminal by writing data to the PORTB register (PHY18). When the port is set as the input, the external signal is gotten directly through the input terminal by reading data from PHY18.

When this PORTB is set as the input, these two ports perform the extra functions as follows:

a. PB0 TERMINAL

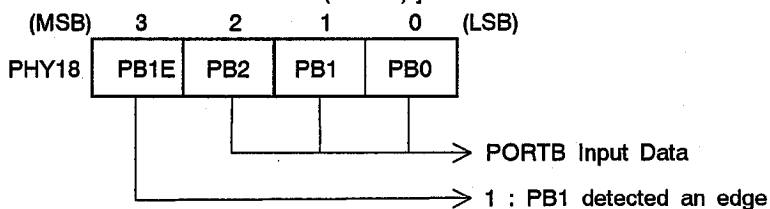
PB0 terminal performs the extra function as the re-start signal input terminal to return from the "STANDBY" mode. When the rising edge of the signal from the external circuit is input into the PB0 terminal in mode of "STANDBY", the "STANDBY" mode is released and the CPU starts the execution again from the suspended address of the program. (refer ■STANDBY FUNCTION)

b. PB1 TERMINAL

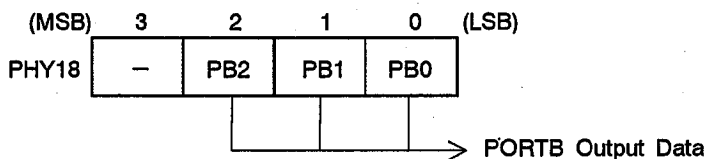
PB1 terminal performs the extra function as the edge detector terminal. When the PB1 terminal detects the edge of the signal from the external circuit, the forth bit(b3) condition of PHY18 is set to "1". The "b3" of PHY18 is set to "1" even when the edge is input during the "STANDBY" mode. The condition of "b3" is kept until the writing operation to PHY18.

The polarity as low to high or high to low of the input signal edge can be selected by the mask option.

[ READING PORTB INPUT DATA (PHY18) ]



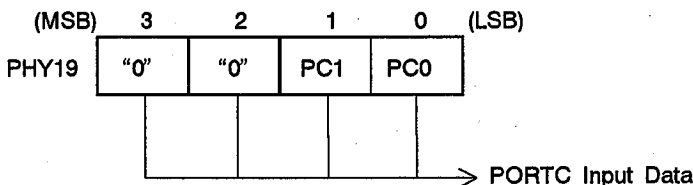
[ WRITING PORTB OUTPUT DATA (PHY18) ]



●PORTC(PC0, PC1)

PORTC is a 2-bit input PORT. It operates also as V<sub>REF</sub> and ADCK terminals of the internal A/D converter by the mask option. When the PORTC is set as the input PORT, the two external signals are gotten directly through the input terminals by reading data from PHY19.

[ READING PORTC INPUT DATA (PHY20) ]

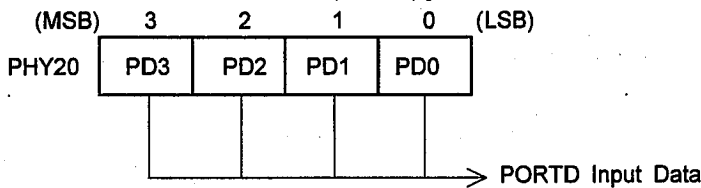


●PORTD(PD0 to PD3)

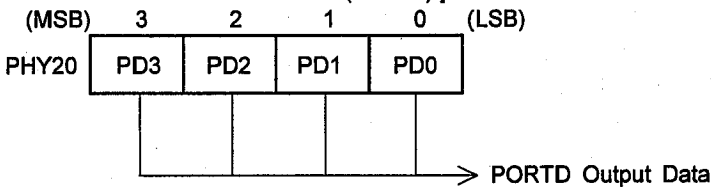
PORTD is a 4-bit input-output PORT. It operates also as the multiplexed 4-bit analog signal input terminals (AIN0 to AIN3) to the internal A/D converter by the mask option. The input or the output is selected for each bit by the mask option. When the PORT is set as the output, the 4-bit signals are output through the output terminals by writing data into the peripheral register assigned for PORTD (PHY20). PHY20 as the output register should be written the output data, because the conditions of the output terminals are unknown while the output data is not written in PHY20. When this PORT is set as the input, the 4-bit external signals are gotten directly through the input terminals by reading data from PHY20.

Though the output circuit is Nch open drain type, the C-MOS input buffer is connected to the same terminal. Therefore, the operating current of the chip by the short circuit current when the middle level voltage between  $V_{DD}$  and  $V_{SS}$  is input to this terminal.

[ READING PORTD INPUT DATA (PHY20) ]



[ WRITING PORTD OUTPUT DATA (PHY20) ]

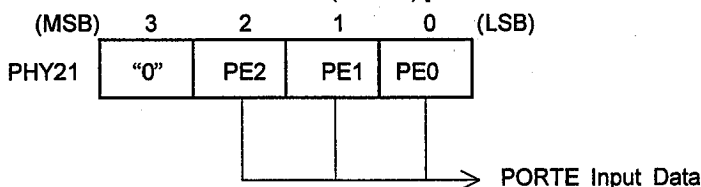


●PORTE(PE0 to PE2)

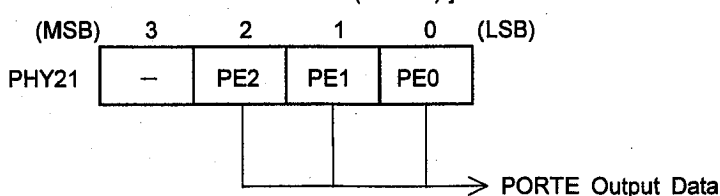
PORTE is a 3-bit input-output PORT. It operates also as the multiplexed 2-channel analog signal input terminals (AIN4 to AIN5) to the internal A/D converter by the mask option. The input or the output is selected for each bit by the mask option. When the PORT is set as the output, the 3-bit signals are output through the output terminals by writing data into the peripheral register assigned for PORTD (PHY21). PHY21 as the output register should be written the output data, because the conditions of the output terminals are unknown while the output data is not written in PHY21. When this PORT is set as the input, the 3-bit external signals are gotten directly through the input terminals by reading data from PHY21.

Though the output circuit is Nch open drain type, the C-MOS input buffer is connected to the same terminal. Therefore, the operating current of the chip by the short circuit current when the middle level voltage between  $V_{DD}$  and  $V_{SS}$  is input to this terminal.

[ READING PORTE INPUT DATA (PHY21) ]



[ WRITING PORTE OUTPUT DATA (PHY21) ]

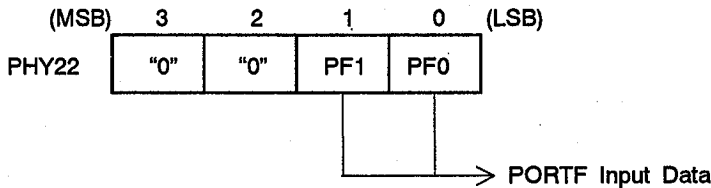




●PORTF(PF0 to PF1)

PORTF is a 2-bit input PORT. It operates also as EXTI input terminal for the external interrupt input and CNT1 terminal for the event counter external clock input by the mask option. When the PORTF is set as the input PORT, the two external signals are gotten directly from the input terminals by reading data from PHY22.

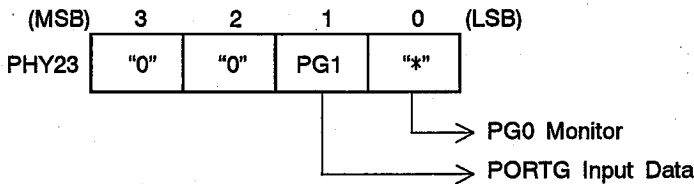
[ READING PORTF INPUT DATA (PHY22) ]



●PORTG(PG0, PG1)

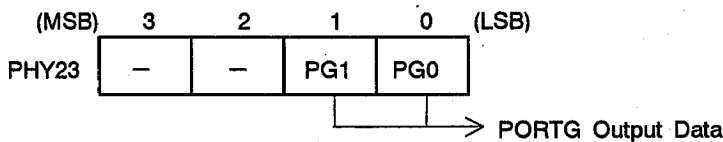
PORTG is a 2-bit input-output PORT. It operates also as SDO and SDI(O) terminals for the 8-bit serial interface by the mask option. When the PORTG is selected as the input-output PORT, PG0 is fixed as the output and PG1 can be selected as the input or the output by the mask option. When the PORTG is selected as the output, the two signals are output through the output terminals to the external circuit by writing data to the PORTG register(PHY23). When PL1 is selected as the input, the external signal is gotten directly through the input terminal by reading data from PHY23.

[ READING PORTG INPUT DATA (PHY23) ]



When PG0 is output, its output condition can be monitored.

[ WRITING PORTG OUTPUT DATA (PHY23) ]

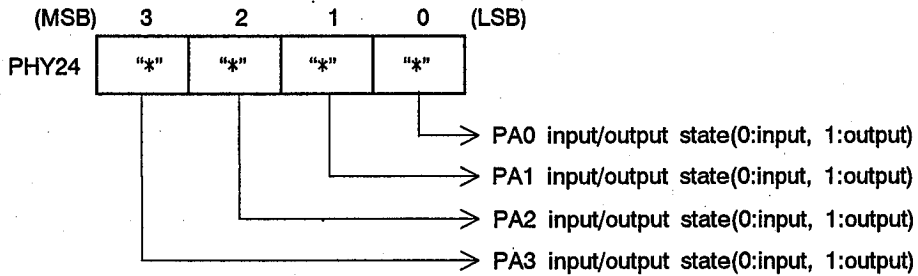


● PROGRAMMABLE INPUT/OUTPUT PORT CONTROL REGISTER(PHY24)

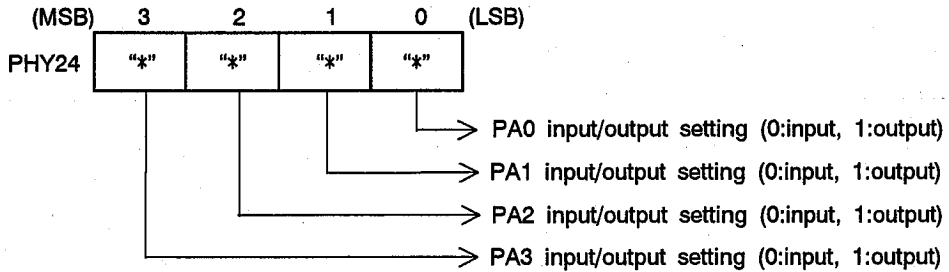
Programmable Input / Output Port Control Register(PHY24) is a peripheral register to set the programmable input / output PORTA. The input or the output is selected for each bit by the mask option. It is set to "1" as the output, and is set to "0" as the input.

PORTA are set as the input in accordance with the state of PHY24 which is set to "0" on the "RESET" operation.

[ READING Programmable Input / Output Port Control Register(PHY24) ]



[ WRITING Programmable Input / Output Port Control Register(PHY24) ]



**(2) PROGRAMMABLE INPUT/OUTPUT PORT OPERATION**
**a. The output operation example**

PA0 and PA1 of PORTA output "H", and PA2 and PA3 of PORTA output "L".

```

SRPC      ;
LDI       Y,0      ; Peripheral table is
LDI       A,%0001 ; set as the table1
TAP      ;
LDI       Y,1      ; PHY17 is pointed
LDI       A,%0011 ; "0011" is stored into Accumulator
TAP      ; Data in Accumulator is transmitted to PHY17
           ; (PORTA output register)
LDI       Y,8      ; PHY24 is pointed
LDI       A,%1111 ; "1111" is stored into Accumulator
TAP      ; Data in Accumulator is transmitted to PHY24
           ; PORTA is set as the output
    
```

**b. The input operation example**

Accumulator gets the input data from PORTA.

```

SRPC      ;
LDI       Y,0      ; Peripheral table is
LDI       A,%0001 ; set as the table1
TAP      ;
LDI       Y,8      ; PHY24 is pointed
LDI       A,%0000 ; "0000" is stored into Accumulator
TAP      ; Data in Accumulator is transferred to PHY24
LDI       Y,1      ; PHY17 is pointed
TPA      ; The input data from PHY17 is transferred to Accumulator
    
```

The signal from PA0 terminal is stored into the LSB of Accumulator, the signal from PA1 terminal is stored into the b1 of Accumulator, the signal from PA2 terminal is stored into the b2 of Accumulator, and the signal from PA3 terminal is stored into the b3 of Accumulator.

**INPUT OUTPUT TERMINAL TYPE**

Each terminal of PORTA, B, C, D, E, F, and G can select a terminal type from the follows by the mask option which is the same mask of the program coding into ROM and the others. But PORTC, and F select only the input terminal type. PG0 of PORTG select only the output terminal type.

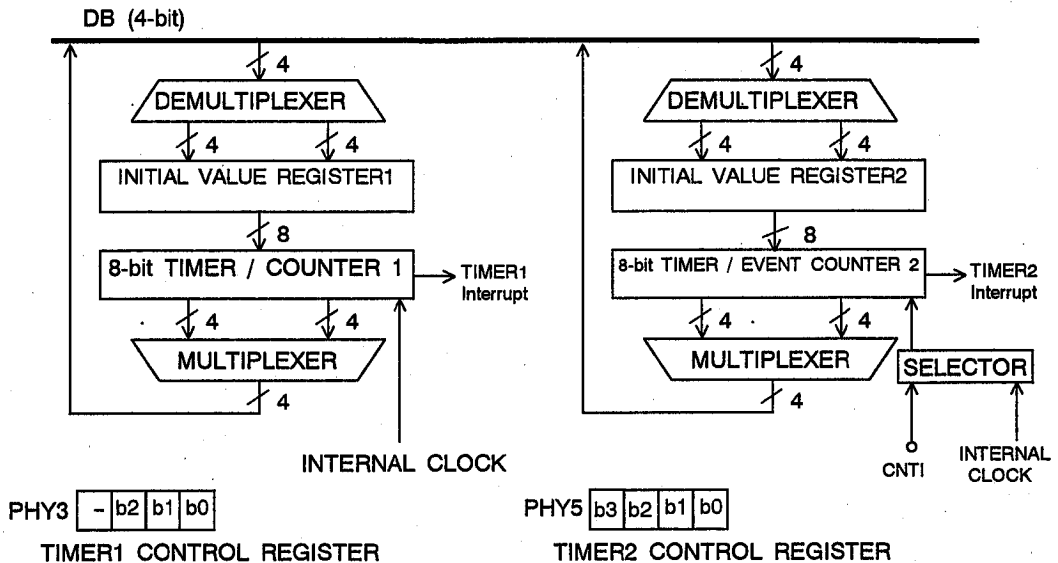
**INPUT OUTPUT TERMINAL TYPES**

	Types	With Pull-up	Without Pull-up	Terminals	
INPUT TERMINAL	C-MOS	Type ICP 	Type IC 	AIN0/PD0~ AIN3/PD3, AIN4/PE0, AIN5/PE1, PE2, SDI(O)/PG1	
	SCHMITT TRIGGER	Type ISP 	Type IS 	PB0~PB2, ADCK/PC0, VREF/PC1, EXT1/PF0, CNT1/PF1	
OUTPUT TERMINAL	C-MOS	/		Type ON 	PB0~PB2, SDO/PG0, SDI(O)/PG1
	N-channel (Nch) OPEN DRAIN	Type ONP 	Type ON 	AIN0/PD0~ AIN3/PD3, AIN4/PE0, AIN5/PE2, PE3	
PROGRAMMABLE INPUT OUTPUT TERMINAL	C-MOS INPUT / N-channel (Nch) OPEN DRAIN OUTPUT	Type IOP 	Type IO 	PA0~PA3	

**■ TIMER**

The NJU3503 prepares a couple of Programmable Timer / Counter(Timer1,Timer2) consisted of the 8-bit binary counter.

[ Structure of Timer / Counter ]



Timer1 counts only the internal clock and Timer2 counts either of the internal clock or the external clock in accordance with the condition of bit2(b2) of the Timer2 Control Register(PHY5). The initial value of the counter can be set the optional value by the program which instructs to write the data(a value of the time-interval or the event-count) into the Initial Value Register(Timer1 or Timer2 is set the each value independently). In enabling the timer interrupt, when the counter counts from "FF" to "00" (overflow), the timer interrupt request occurs and the internal interrupt process starts the own operation.

In the repeat mode of the Timer operation, when the counter overflows, the initial value is loaded into the counter automatically and the counter continues the count from the loaded initial value(Auto re-load function: See the repeat mode of the Timer operation timing chart). In the single mode of the Timer operation, when the counter overflows, the count is stopped(See the single mode of the Timer operation timing chart). For starting the count operation again, the start bit(LSB) of the Timer1 or Timer2 Control Register must be set to "1". The latest initial value is set into the counter and the counter starts the count.

In enabling the interrupt operation, when the counter overflows, the Timer / Counter overflow flag is set to "1" and the internal interrupt process starts to the own operation. In disabling the timer interrupt, the Timer / Counter overflow flag is not set. The Timer / Counter overflow flag is initialized by the Timer Start or the Reset signal.

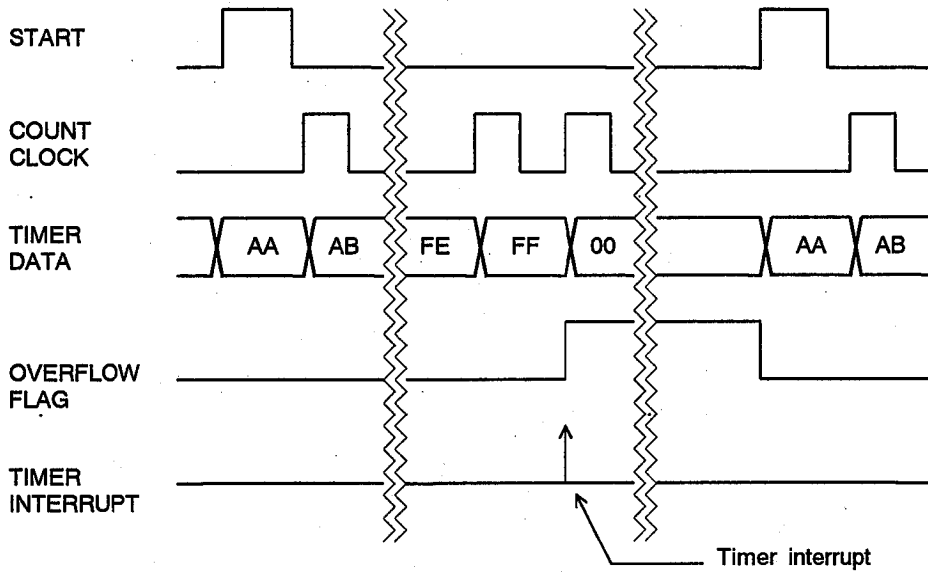
The internal clock into the counter is the divided clock from the internal prescaler. The frequency of the clock can be selected by the mask option from follows which are the dividing numbers based on the inverse of the 1-instruction executing period( $1/f_{osc} \times 6$ ).

1/2, 1/4, 1/8, 1/16, 1/32,1/64, 1/128, 1/256, 1/512, 1/1024, 1/2048,1/4096

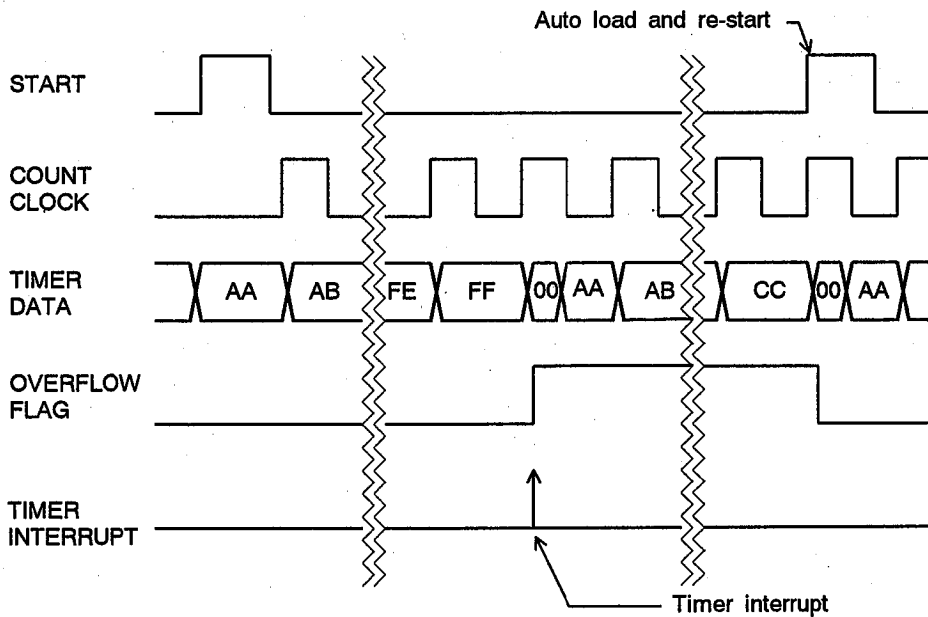
When the bit2(b2) of the Timer1 / Prescaler Control Register is set to "1", the prescaler generating the internal count clock is stopped the operation. As the result, Timer / Counter stops the count operation.

In the external clock operation of Timer2, the external clock must be input to CNTI terminal. The Timer2 Control Register selects either the internal clock operation or the external clock operation.

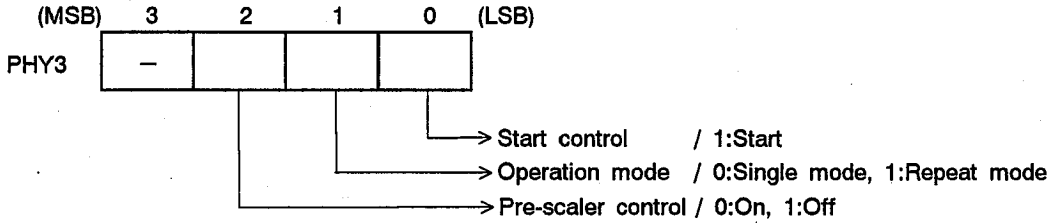
[ THE SINGLE MODE OF THE TIMER OPERATION TIMING ] (The initial value is set to "AAh")



[ THE REPEAT MODE OF THE TIMER OPERATION TIMING ] (The initial value is set to "AAh")



●Timer1 / Prescaler Control Register { PHY3 ; (Y'=3, Peripheral register table 0) }  
 [ Writing to the Timer1 / Prescaler Control Register ]



EX.) An example of the start procedure in the single mode and the internal clock operation.

```

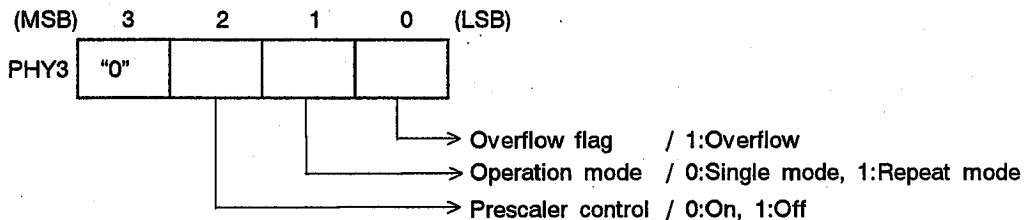
:
:
SRPC
LDI Y,3 ;PHY3(Timer1/Prescaler Control Register) is pointed.
LDI A,%0000;"0000"(BIN) is stored to accumulator
TAP ;Data is transferred from accumulator to PHY3
LDI A,%0001;"0001"(BIN) is stored to accumulator
TAP ;Data is transferred from accumulator to PHY3
:
:

```

} Single mode,  
Prescaler is enable  
} The count is started.

Remarks) When the prescaler generating the internal count clock is stopped the operation, Timer is also stopped. But the data in the counter is kept. Therefore Timer can continue to count from the kept condition of the counter when the prescaler is started the operation again. However, the clocks from the prescaler are delivered to Serial I/O, CKOUT terminal and A/D converter controller, therefore the prescaler requires careful operation, especially stop or start. When the prescaler is started the operation again after it was stopped, it is reset and start to count from "zero".

[ Reading from the Timer1 / Prescaler Control Register ]



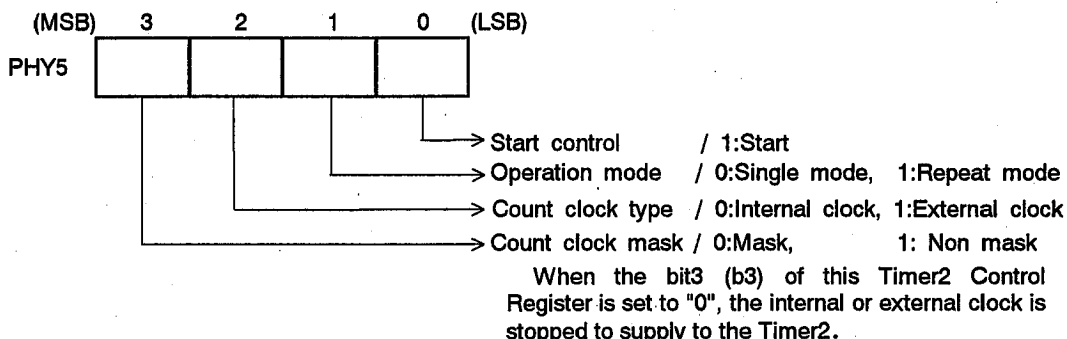
EX.) An example of the overflow in the single mode and the internal clock operation.(The data of the Timer1 / Prescaler Control Register is "0001"(BIN).)

```

:
:
SRPC
LDI Y,3 ;PHY3(Timer1/Prescaler Control Register) is pointed.
TPA ;"0001"(BIN) of PHY3 is transferred to accumulator.
:
:

```

●Timer2 Control Register { PHY5 ; (Y'=5, Peripheral register table 0) }  
 [ Writing to the Timer2 Control Register ]



EX.) An example of the start procedure for the repeat mode, the external clock operation and releasing the count clock mask.

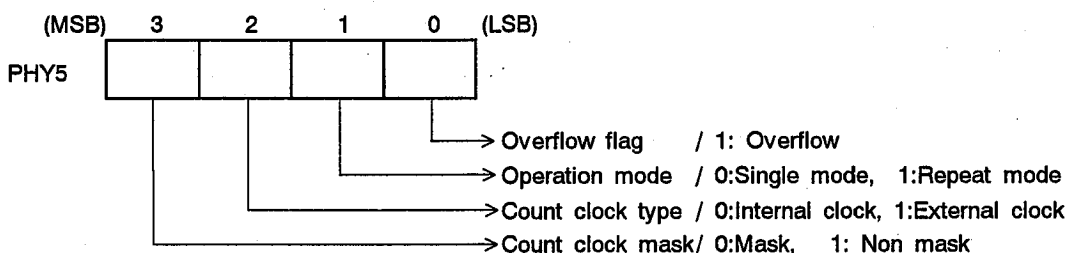
```

    ...
    SRPC      ;
    LDI       Y,5      ;PHY5(Timer2 Control Register) is pointed.
    LDI       A,%1110 ;"1110"(BIN) is stored to accumulator
    TAP      ;Data is transferred from accumulator to PHY5
    LDI       A,%1111 ;"1111"(BIN) is stored to accumulator
    TAP      ;Data is transferred from accumulator to PHY5
    ...
    
```

} Repeat mode, External clock operation.  
 The count is started.

Remarks) In the Timer2 operation, when the count clock mask bit(b3) of the Timer2 Control Register is set to "0", the Timer2 is stopped to count and it holds the latest data of the 8-bit counter2. When the b3 is set to "0", the Timer2 starts to count from the hold data of the 8-bit counter2.

[ Reading from the Timer2 Control Register ]



EX.)An example of the Timer2 starting information as the Single mode, the internal clock operation and the released clock mask. (The data of Timer2 Control Register is "1001"(BIN).)

```

    ...
    SRPC      ;
    LDI       Y,5      ;PHY5(Timer2 Control Register) is pointed
    TPA      ;Data is transferred "1001"(BIN) of PHY5 to accumulator
    ...
    
```



- Initial Value Register / Timer Counter

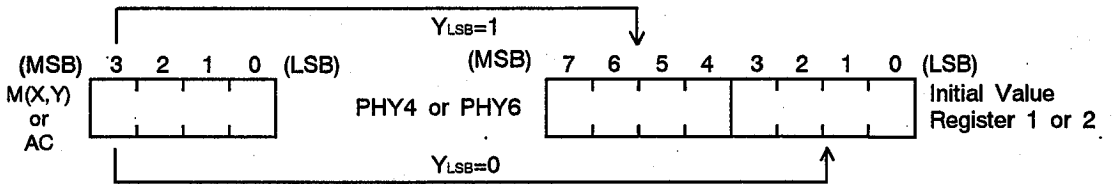
Initial Value Register1 / Timer Counter1 {PHY4;(Y'=4, Peripheral register table 0)}

Initial Value Register2 / Timer Counter2 {PHY6;(Y'=6, Peripheral register table 0)}

The Initial Value Register consisted of a 8-bit register sets the initial value to the counter, or gets the counted value from the counter.

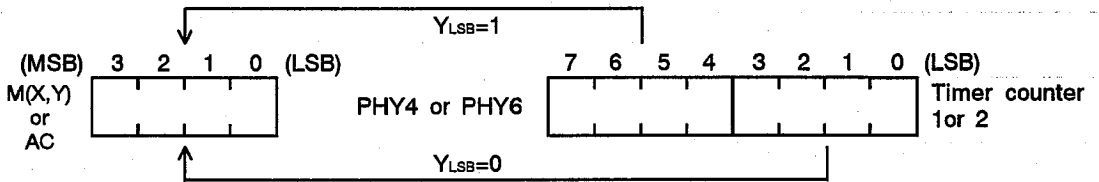
[ Writing to the Initial Value Register1 or 2 ]

When a data in RAM or Accumulator is transferred to the Initial Value Register, the data is loaded into the higher 4-bit(b7 to b4 ) or lower 4-bit(b3 to b0) of the Initial Value Register in accordance with the condition of LSB of Y-register.



[ Reading from the Timer Counter1 or 2 ]

When a current data in the Timer Counter1 or Timer Counter2 is transferred into RAM or Accumulator, the data is gotten from higher 4-bit(b7 to b4) or lower 4-bit(b3 to b0) of the Timer Counter1 or Timer Counter2 in accordance with the condition of LSB of Y-register.

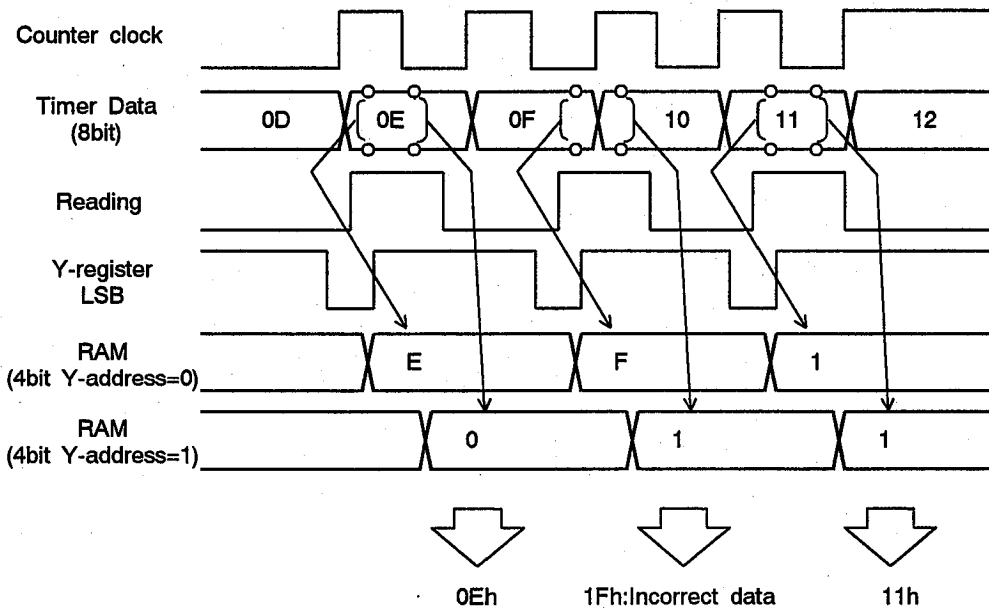


[ Reading data from 8-bit Timer Counter1 or 2 to RAM ]

Though the data of the Timer and Counter can be read in the count operation, the read data is sometimes incorrect when the clock inputs to the counter during the reading operation.

When the 8-bit counter data is read in count operation as shown in the following timing chart (An example of data reading from the counter to RAM), Timer often counts up between the first 4-bit data reading and the second. In case of the following chart, though the timer data is "0Fh" when the lower 4-bit data is gotten, it is "10h" when the higher 4-bit data is gotten. Therefore the final data becomes to be "1Fh".

[ An example of data reading from the counter to RAM ]

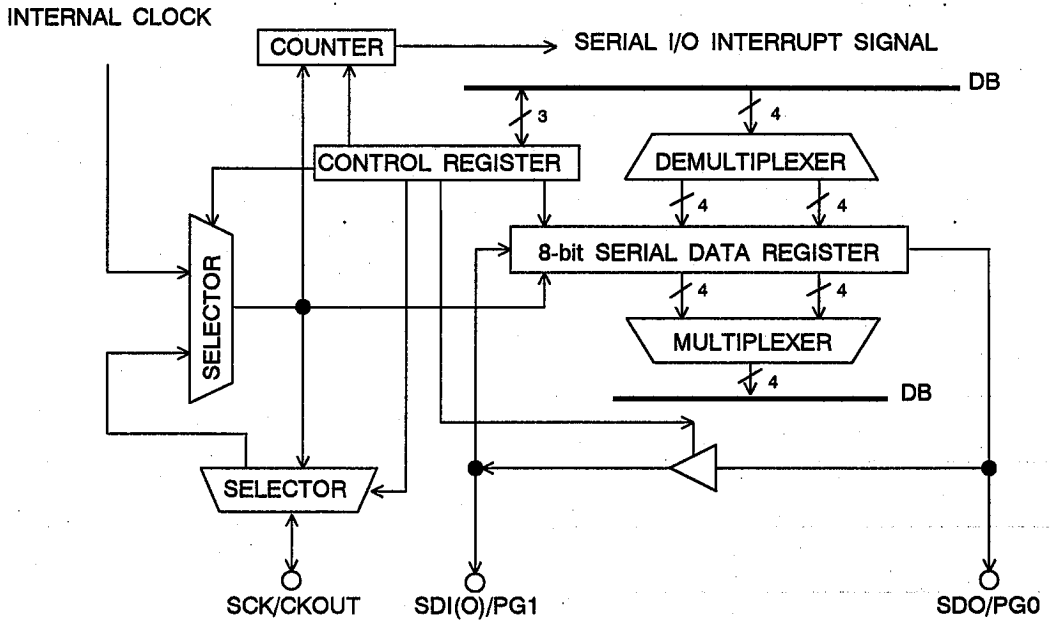


There are some other cases to read the incorrect data from the 8-bit counter during the count operation depending on the relation with the external clock speed and the system execution speed.

● SERIAL INPUT OUTPUT

SERIAL INPUT OUTPUT consists of the shift registers to convert from 8-bit parallel data to serial data, the 3-bit serial clock counter, and the 3-bit serial control register. It operates as the 8-bit serial input or output. The external or internal clock is selected as the shift clock in accordance with the Serial Input / Output control register.

[ Block diagram of the Serial Input Output ]



The serial input or output operation starts when the LSB of the Serial Input / Output control register(PHY1) is set to "1". In the external clock operation, the serial input or output operation waits to start until the external clock come in.

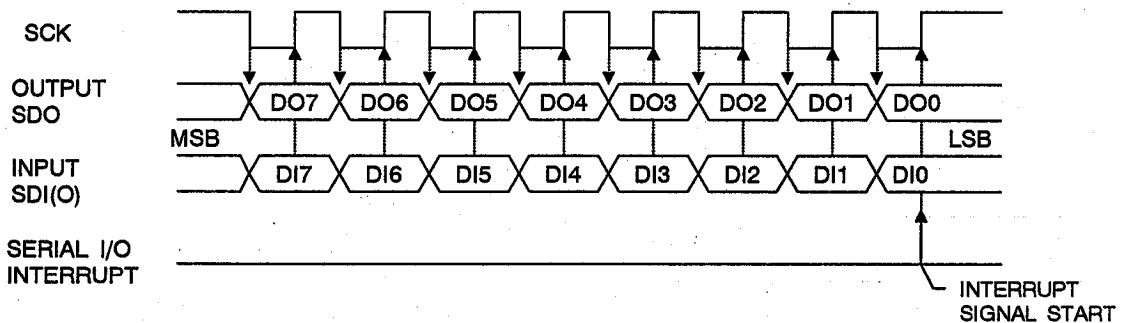
When the serial shift register (PHY2) is set the data in advance, the data is output(transmitted) through the SDO or the SDI(O) terminal. The SDI(O) terminal can be changed as a transmitter or a receiver in accordance with the bit3(b3) of PHY1. The data order, MSB or LSB first, is selected by the mask option.

Serial Input Output operates as the 3-wire method using SDI(O), SCK and SDO terminals, or the 2-wire using SDI(O) and SCK terminal.

<<The 3-wire method>>

The data synchronized with the falling edge of the SCK clock is output(transmitted) through the SDO terminal. The data synchronized with the rising edge of the SCK clock is input(received) through the SDI(O) terminals.

[ The 3-wire transmission timing chart (MSB first) ]

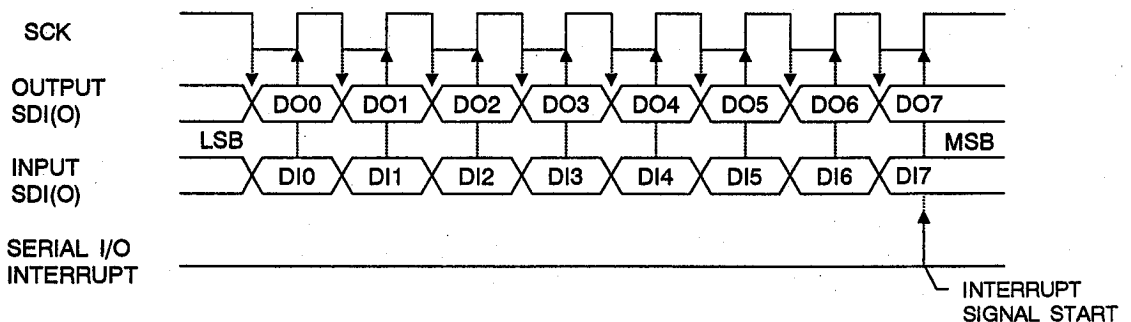


<<The 2-wire method>>

The data synchronized with the falling edge of the SCK clock is transmitted through the SDI(O) terminal. The data synchronized with the rising edge of the SCK clock is received through the SDI(O) terminal.

※ In case of the data transmission through the SDI(O) terminal, the SDI(O) terminal must be set as the output by the condition of the bit3(b3) of the Serial Input / Output control register(PHY1) set to "1". In case of the data reception through the SDI(O) terminal, the SDI(O) terminal must be set as the input by the condition of the b3 of PHY1 set to "0".

[ The 2-wire transmission timing chart (LSB first) ]

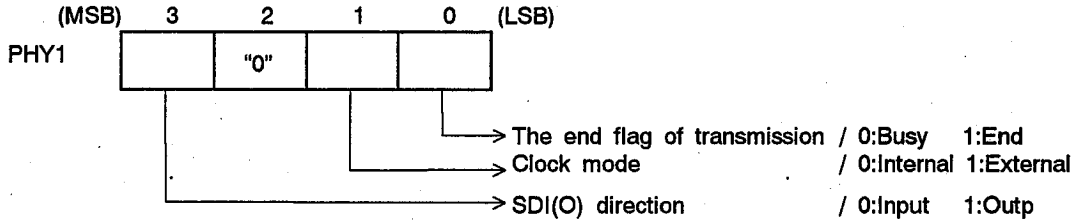




Remarks 3) In case of the external clock operation at the both of the transmission and reception mode, inputting the external clock must wait while the 2-instruction execution period after that LSB of Serial Input / Output control register is set to "1"(START). (one instruction execution period =  $1 / f_{osc} \times 6$ )

If the external clock is input within the 2-instruction execution period, the Serial Input / Output shift register can not recognize the first SCK. The number of the shift operation is decreased a time, 8 times to 7.

[ Reading from the Serial Input / Output Control Register ]



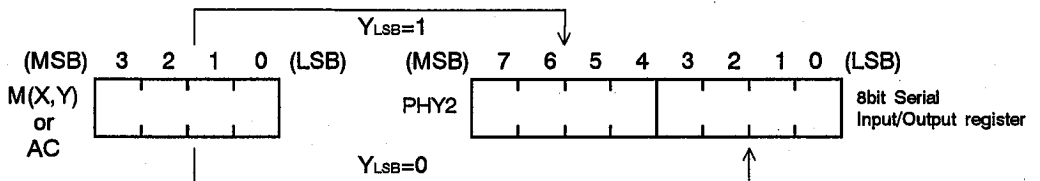
Remarks 4) The end flag of transmission is set to "1" when the serial data(8 bits) transmission operation is ended. It is cleared by setting the serial data transmission start signal in the Serial Input /Output control register.

- Serial Input/Output Shift register { PHY2 ; (Y'=2) }

The Serial Input / Output Shift register consisted of a 8-bit register operates to set the transmission data or to get the reception data.

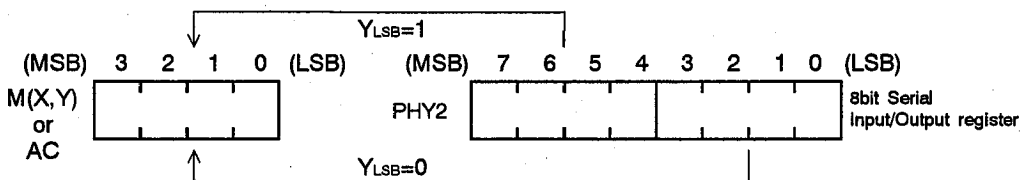
[ Writing to the Serial Input / Output Shift Register ]

The data in RAM or Accumulator is transferred to the Serial Input / Output Shift register, and it is loaded into lower 4-bit(b0 to b3) or higher(b4 to b7) in PHY2 in accordance with the condition of LSB of Y-register.



[ Reading from the Serial Input / Output Shift Register ]

The Serial Input data is transferred to RAM or Accumulator, it is loaded from lower 4-bit(b0 to b3) or higher(b4 to b7) of PHY2 in accordance with the condition of LSB of Y-register.



An example of the serial data reception program

In the internal clock operation, SDI(O) terminal is set as the input and the serial input data is transferred to RAM.

```

WSEG                                ;The RAM area is set
SIO_DAT DS    2                    ;The area to store the serial input data is secured
:
:
;---- Interrupt process ----
ORG    $40                          ;Interrupt vector address of FULL or EMPTY
SINT   SRPC                          ;
      LDI    Y,1                      ;The Serial Input / Output control register is set
      TPA
      TBA    0                        ;The end flag of transmission is tested
      JMP    SIO_OK
      JMP    SINT_E
;
SIO_OK LDI    Y,2                    ;The Serial Input / Output shift register is set
      RRPC                          ;RAM to store the serial input data is pointed
      LDI    X,SIO_DAT.X             ;RAM address, X=0
      LDI    Y,SIO_DAT.Y             ;RAM address, Y=0
      TPMICY                          ;The serial input data is transferred to RAM(lower 4-bit)
                                      ;and Y-register is incremented
      TPMICY                          ;The serial input data is transferred to RAM(higher 4-bit)
                                      ;and Y-register is incremented
;
SINT_E RETI                          ; End of the interrupt process
;
;----- Serial data inputting process -----
SIO_IN SRPC                          ;
      LDI    Y,0                    ;The peripheral register table is set
      CLA
      TAP
      LDI    Y,1                    ;The Serial Input / Output control register is set
      LDI    A,%0000                ;The internal clock operation is set and the SDI(O)
                                      ;terminal is set as the input
      TAP
      LDI    A,%0001                ;The serial data reception is started
      TAP
;
:
:

```

An example of the serial data transmitting program)

In the internal clock operation, the SDI(O) terminal is set as the output and the data in RAM is transmitted.

```

WSEG                                ;The RAM area
SIO_DAT DS 2                        ;The area to store the serial output data
SIO_FLG DS 1                        ;The end flag of transmission
:
:
;---- Interrupt process ----
SINT  ORG $40                        ;Interrupt vector address of FULL or EMPTY
      SRPC
      LDI Y,1                        ;The Serial Input / Output control register is set
      TPA
      TBA 0                          ;The end flag of transmission is tested
      JMP SIO_OK
      JMP SINT_E
:
SIO_OK RRPC                          ;The end flag of transmission is set
      LDI X,SIO_FLG.X
      LDI Y,SIO_FLG.Y
      LDI A,1
      TAM
:
SINT_E RETI                          ;End of the interrupt process
:
;----- Serial data transmitting process -----
SIO_OUT SRPC
      LDI Y,0                        ;The peripheral register table is set
      CLA
      TAP
:
      LDI Y,2                        ;The Serial Input / Output shift register is set
:
      RRPC                          ;RAM to store the serial output data is set
      LDI X,SIO_DAT.X                ;RAM address, X=0
      LDI Y,SIO_DAT.Y                ;RAM address, Y=1
      TMPICY                          ;The data in RAM is transferred to the Serial Input /
      ; Output shift register(lower 4-bit)
      ; and Y-register is incremented
      TMPICY                          ;The data in RAM is transferred to the Serial Input /
      ; Output shift register(higher 4-bit)
      ; & Increments Y
:
      SRPC
      LDI Y,1                        ;The Serial Input / Output control register is set
      LDI A,%1000                    ;The internal clock operation and the transmission
      ; mode are set
      TAP
      LDI A,%1001                    ;The serial data transmitting operation is started
      TAP
:
:
:

```



## ■ INTERRUPT

The NJU3503 prepares four kinds of the interrupt. The interrupt "enable" or "disable" is controlled by the program. The interrupt operates as single process and no multiple. However, when new interrupt request occurs during the other interrupt process, the request is kept, and then the new interrupt process starts after the prior interrupt process. The priority order of the interrupt is that the first is (1)External interrupt-1, the second is (2)Internal interrupt-1, the third is (3)Internal interrupt-2, and the fourth is (4)Internal interrupt-3 as shown in bellow.

When the interrupt request flag is set by the own factor, the interrupt enabled by the interrupt control register (PHY10) stores the data of Program Counter, Accumulator, X-reg, X'-reg, Y-reg, Y'-reg, RPC, and STATUS into the STACK register, and sets the interrupt vector address into Program Counter, and then the interrupt process is started. The return from the interrupt process by "RETI" instruction resets the corresponded interrupt request flag, and regains the held data from STACK, and then the operation before the interrupt process is started continuously. When the interrupt control register disables the interrupt process, the interrupt request flag is not set.

### [ THE PRIORITY ORDER OF FOUR INTERRUPTS ]

Order	Interrupt	Vector Address(H:HEX)
(1)	External interrupt-1	10H
(2)	Internal interrupt-1    Timer/Counter-1 Overflow	20H
(3)	Internal interrupt-2    Timer/Counter-2 Overflow	30H
(4)	Internal interrupt-3    Serial shift register Full/Empty	40H

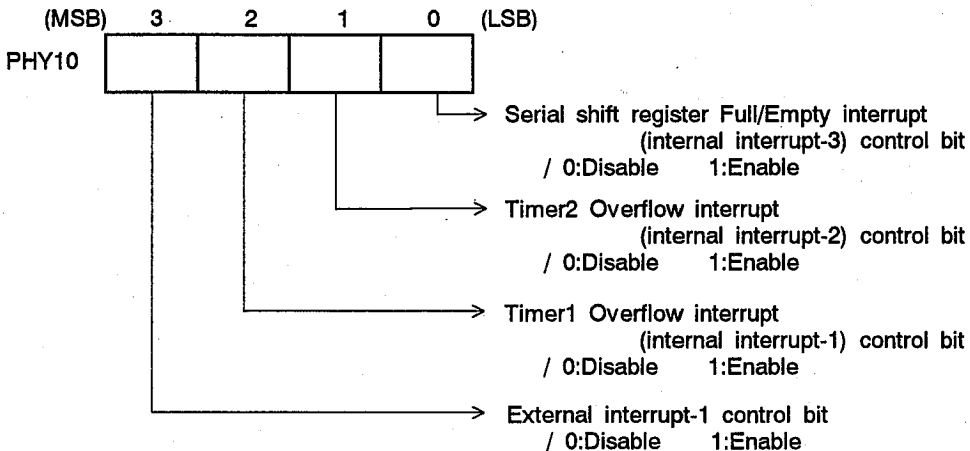
The External interrupt-1 enabled by PHY10 is started the interrupt process when the rising edge of signal pulse is input to the external interrupt signal input terminal(EXTI). The External interrupt-1 request flag is re-set by "RETI" instruction. When the external interrupt-1 occurs during the standby mode by the HALT instruction, the External interrupt-1 request signal is latched and its interrupt process is started after that the standby mode is released.

The Internal interrupt enabled by PHY10 is started the interrupt process when the internal interrupt request flag is set.

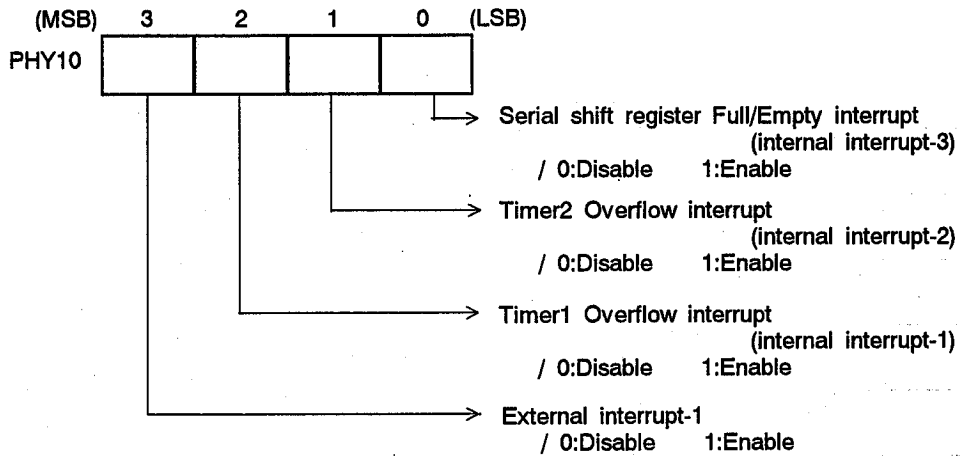
The Timer1 and the Timer2 interrupt request flags are independent of the overflow flag, and they are reset by "RETI" instruction, (TIMER)START signal of the Timer control register, or RESET signal from the external circuit. Serial Input Output interrupt request flag is set synchronizing with the transmission end flag when its interrupt is enabled by PHY10. And the flag is reset by the "RETI" instruction or the RESET signal from the external circuit.

### ● INTERRUPT CONTROL REGISTER { PHY10 ; (Y'=10) }

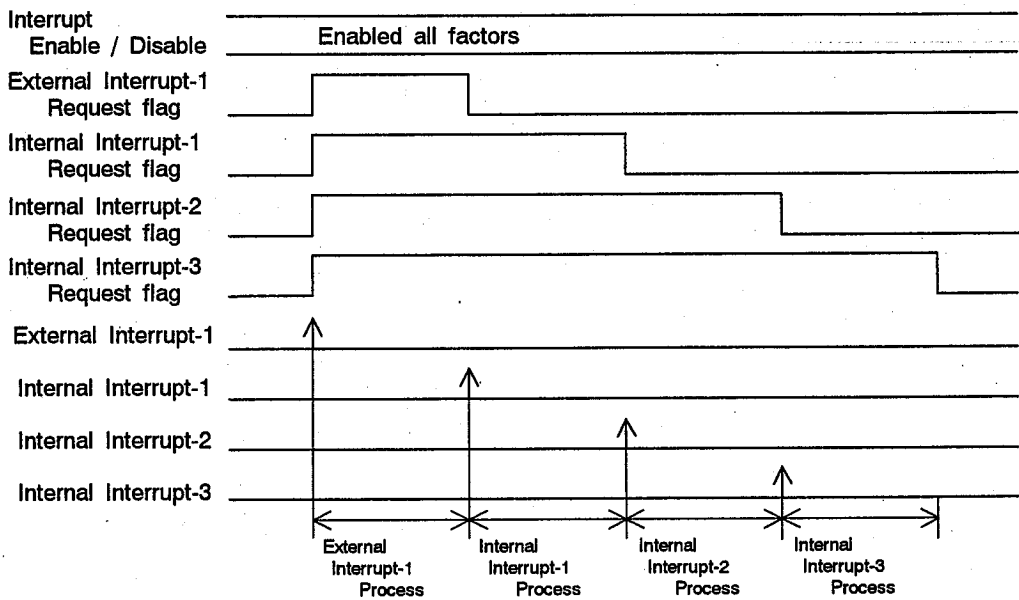
#### [ Writing to the Interrupt Control Register ]



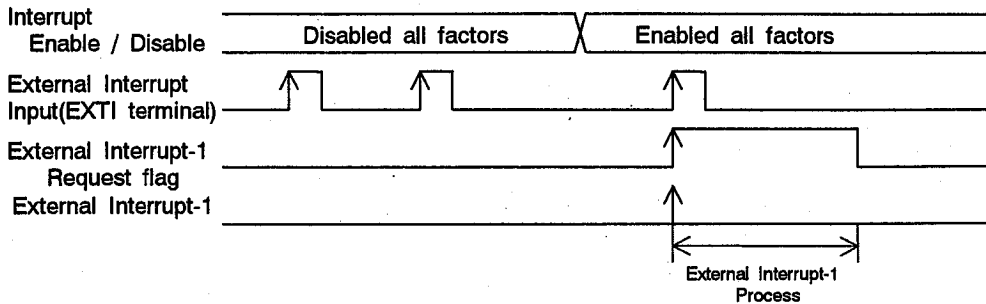
[ Reading from the Interrupt Control Register ]



[ Enabled all factors (b0 to b3 of PHY10 were set to "1" ) ]

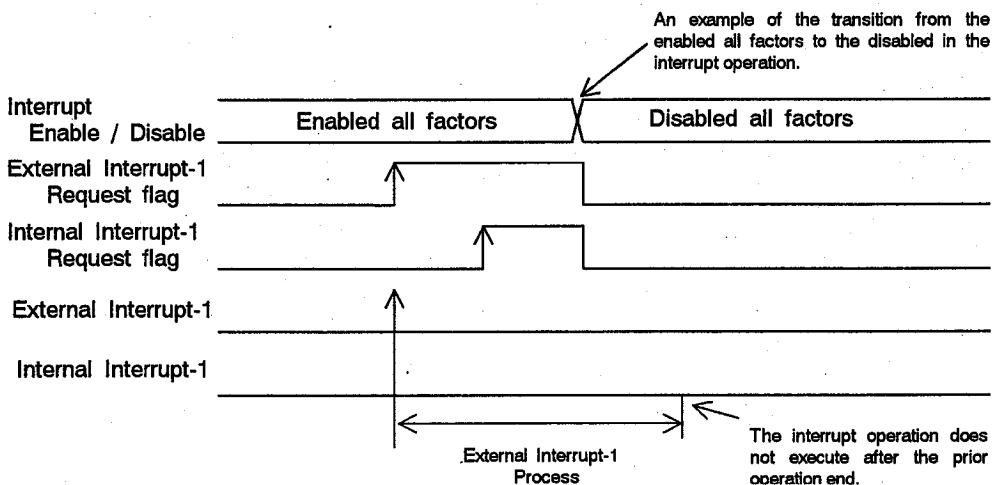


[ From the all factors disabled to the enabled (b0 to b3 of PHY10 are changed from "0" to "1") ]



※ The internal interrupt is also ignored while it is disabled.

[ From the all factors enabled to the disabled (b0 to b3 of PHY10 are changed from "1" to "0") ]



※ When the interrupt is enabled, the latest interrupt request occurred during the prior other interrupt process starts its interrupt process after the prior interrupt operation. However, when the interrupt is disabled during the prior interrupt process as shown in above timing chart, the latest interrupt request does not start. But the prior interrupt process is completed.

## ■ A/D CONVERTER

The A/D converter operates with the following specification.

- A/D Conversion : Successive Approximation method
- Minimum conversion Time : 40  $\mu$ sec ( $V_{DD}=5V$ ,  $V_{REF}=5V$ ,  $f_{ADCK}=225kHz$ )
- Resolution : 8 bit (256 step)
- Absolute Accuracy :  $\pm 2$  LSB ( $V_{DD}=5V$ ,  $V_{REF}=5V$ )
- Reference Voltage : 2.4V  $\sim$   $AV_{DD}$
- Analog Input Voltage :  $V_{SS} \sim V_{REF}$
- Channel : Multiplexed 6-channel Input

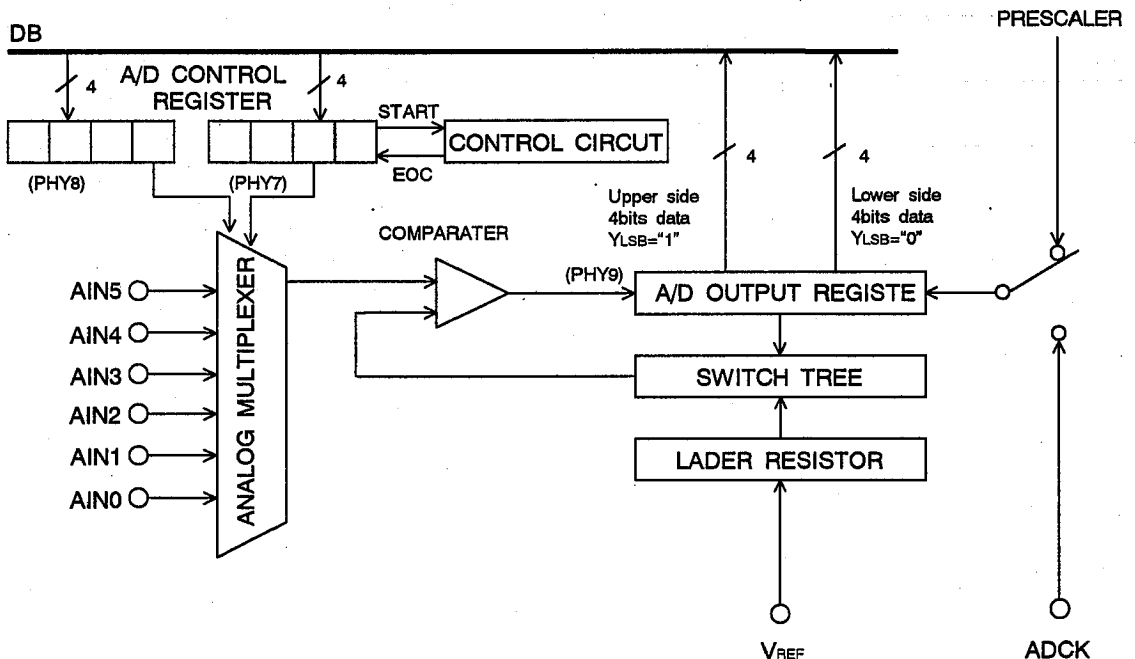
The A/D converter block diagram and the timing chart are shown in bellow.

The lower 2 bits of the A/D control register(PHY7) and the lower 1 bit of the A/D control register(PHY8) are the switches to select an analog input channel from four multiplexed inputs(AIN0 to AIN5). The analog input signal to the analog input port selected by the A/D control register is converted to the digital data, and then the digital data is stored into the A/D output register(PHY9).

The A/D control clock can selected either the external clock or the internal by the mask option. In the external clock operation, the input clock from the "ADCK" terminal operates as the A/D control clock. In the internal clock operation, the clock divided in the internal Prescaler operates as the A/D control clock. The frequency of the clock from the internal Prescaler can be selected by the mask option from follows which are dividing numbers based on the inverse of one instruction execution time( $1/f_{osc} \times 6$ ).

1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512, 1/1024, 1/2048, 1/4096

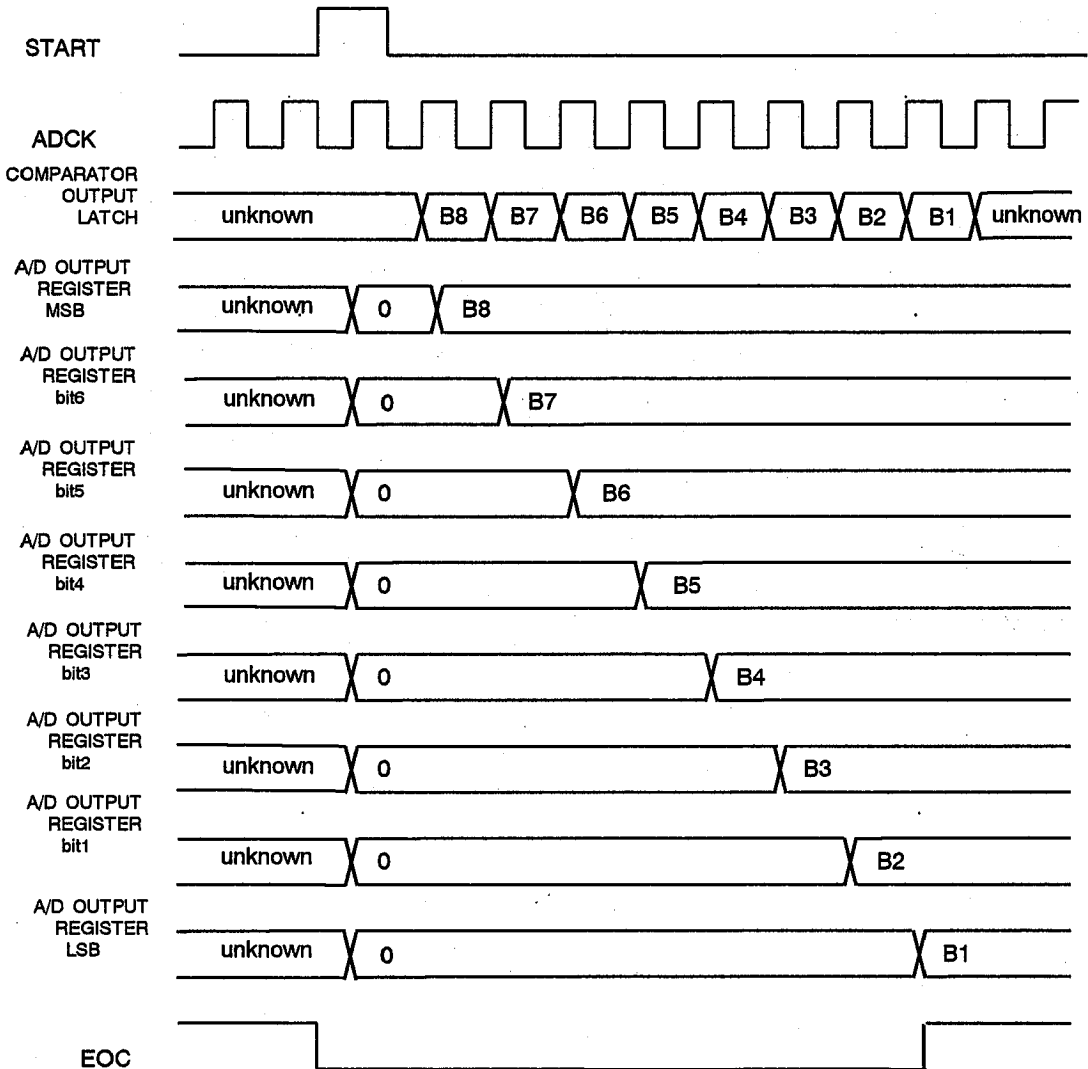
[ A/D CONVERTER BLOCK DIAGRAM ]



Remarks) The A/D control clock can be selected either the external clock from the ADCK terminal or the internal clock from the Prescaler by the mask option. The Prescaler supplies clocks to Timer/Counter, Serial Input Output, and A/D converter.

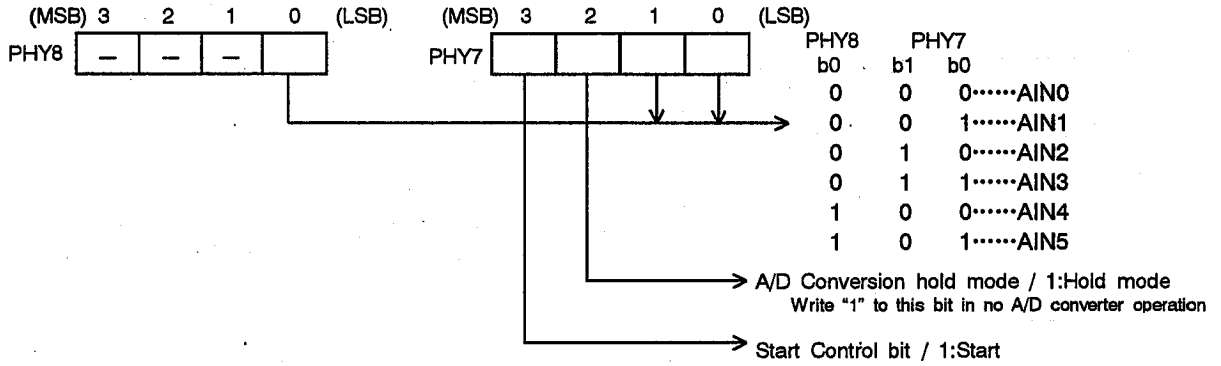
The maximum frequency of the A/D control clock is 225KHz in the both of the internal and the external clock operation.

### [ A/D CONVERTER OPERATION TIMING CHART ]



●A/D CONTROL REGISTER { PHY7; (Y'=7), PHY8; (Y'=8) }

[ Writing to the A/D Control Register { PHY7; (Y'=7), PHY8; (Y'=8) } ]



EX.) An example of A/D converter start procedure for selecting AIN1 as the input and releasing the A/D hold mode.

```

SRPC
LDI Y,8 ; PHY8(A/D control register) is pointed
LDI A,%0000 ; "0000"(BIN) is stored to AC
TAP ; Data transferred from AC to PHY10
LDI Y,7 ; PHY7(A/D control register) is pointed
LDI A,%0001 ; "0001"(BIN) is stored to AC
TAP ; Data transferred from AC to PHY7
LDI A,%1001 ; "1001"(BIN) is stored to AC
TAP ; Data transferred from AC to PHY7

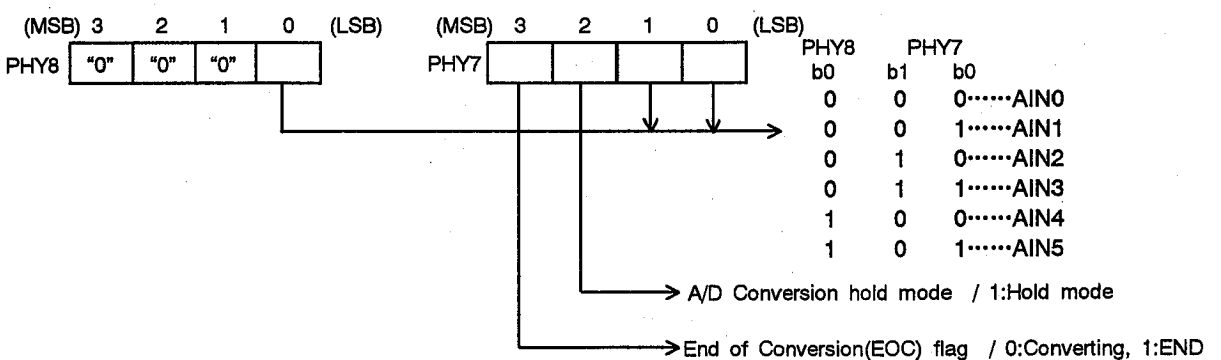
```

AIN1 as the input,  
Releasing Hold mode

Start of conversion

REMARKS) In the external clock operation, the external clock must be input to the ADCK terminal before the start of A/D conversion.

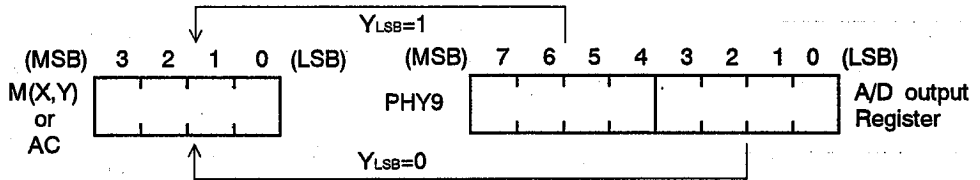
[ Reading from the A/D Control Register ]



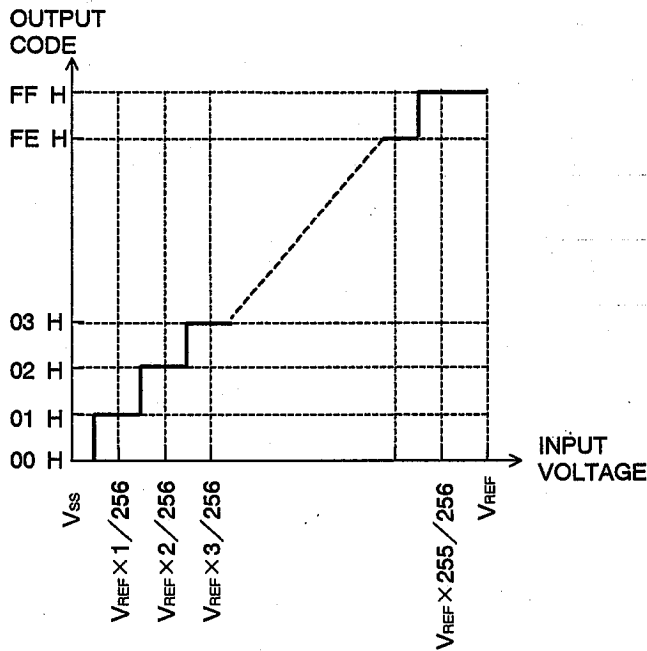
● A/D OUTPUT REGISTER { PHY9; (Y'=9) }

The 8-bit data converted by the A/D converter can be transferred to RAM or Accumulator. Either the higher 4-bit data or the lower is gotten in accordance with the condition of LSB of Y-register.

[ Reading from the A/D Output Register ]



[ Analog input voltage vs Output digital data ]



An example of A/D conversion operation)

AIN2 terminal is selected and the result of the A/D conversion is transferred to RAM.

```

ADC_DAT  WSEG          ;RAM area
DS        2           ;Are for the result of A/D conversion
:
:
ADC_EXE  SRPC          ;
LDI      Y,0         ;Peripheral register table 0
CLA
TAP
;
LDI      Y,8
LDI      A,%0000
TAP      ;A/D control register
LDI      Y,7         ;AIN2 as the input
LDI      A,%0010
TAP
LDI      A,%1010    ;Start of A/D conversion
TAP      ; & AIN2 terminal
;
LP_ADC   TPA          ;End of conversion ?
TBA      3
JMP      ADC_END
JMP      LP_ADC
;
ADC_END  LDI          ;A/D conversion register
Y,9
;
RRPC     ;RAM to store the result of A/D conversion
LDI      X,ADC_DAT.X ;RAM address X=0
LDI      Y,ADC_DAT.Y ;RAM address Y=0
TPMICY   ;The A/D converted data to RAM
; lower 4-bit at YLSB=0
TPMICY   ;The A/D converted data to RAM
; higher 4-bit at YLSB=1
:
:

```



## ■ STANDBY FUNCTION

STANDBY FUNCTION halts the IC operation and reduces the current consumption.

The STANDBY function starts by the HLT instruction. After the HLT instruction execution cycle, the internal oscillator operation is stopped and all of the operation is halted. In case of the external clock operation, the clock is stopped automatically delivering into the internal system by the internal circuit, and all of the operation is halted as same as the internal oscillator operation. This is STANDBY mode.

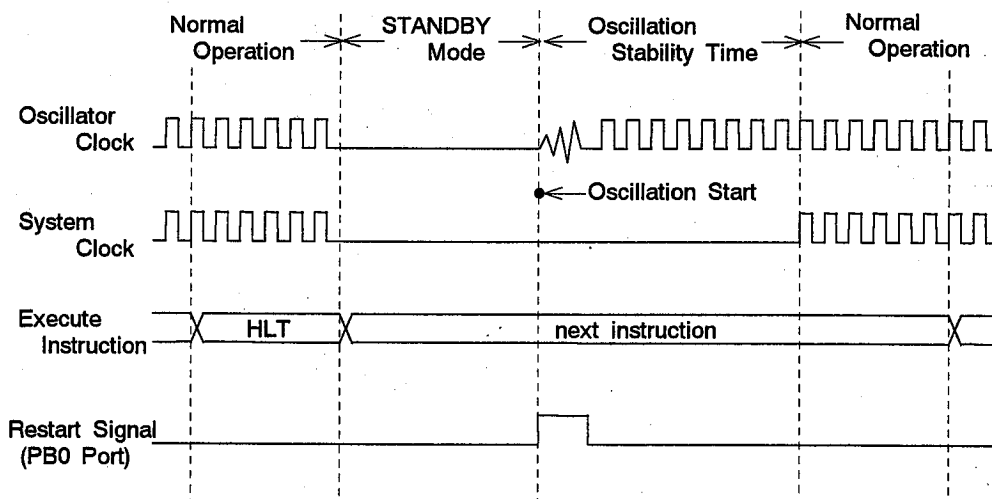
In the STANDBY mode, the operating current can be reduced. Though the clock into the internal system is stopped and all of the operation is halted, all conditions of Program Counter, Registers, and data in RAM are kept certainly.

Two ways to release from the STANDBY mode are prepared. One way is the reset operation that when the reset signal is input to RESET terminal, the operation starts from the initial condition. The other way is the re-start operation that when the re-start signal is input to PB0 terminal, the operation starts from the kept Program Counter location which is the program address after the final operation. In case of the re-start signal operation, if the rising signal, low to high, is input to PB0 terminal, the internal oscillator circuit starts at first. After the stabilized clock from the internal oscillator was counted eight times, the clock is started delivering into the internal system. Then the NJU3503 starts to operate from the kept Program Counter location with all of the kept conditions. (See \*1)

In case of the external clock operation, the external clock must be started to supply to the OSC1 terminal before the STANDBY mode is released. The external clock is recommended to stop supplying to the OSC1 terminal for reducing the power consumption during the STANDBY mode.

\*1: When the re-start signal is input to PB0 terminal to release the STANDBY mode, PORTB must be selected as the input by the mask option.

### [ STANDBY MODE TIMING CHART ]



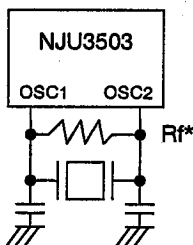
## ■ CLOCK GENERATION

The system clock is generated in the internal oscillator circuit with the external crystal or ceramic resonator, or the resistor connected to OSC1 and OSC2 terminals. Furthermore, the NJU3503 can operate by the external clock to the OSC1 terminal for the system clock. In the external clock operation, the OSC2 terminal must be opened.

The typical application examples for each oscillator circuit are shown in follows. However a Crystal or a Ceramic operation requires the considered evaluation, because the oscillator operates in accordance with the characteristics of each component.

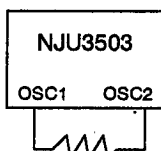
### [ OSCILLATOR APPLICATION EXAMPLES ]

① X'tal/Ceramic oscillation

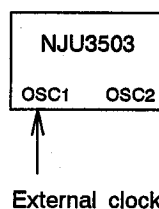


The resistor  $Rf^*$  is sometimes required to connect when the Crystal operation.

② CR oscillation



③ External clock input

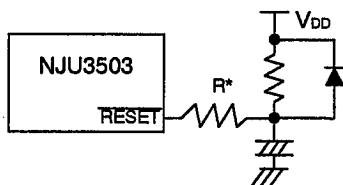


## ■ RESET OPERATION

All of the internal circuits are initialized by inputting the low level signal to the RESET terminal.

A circuit example for Power On Reset Operation with a resistor, a capacitor, and a diode is shown in bellow. Power On Reset Operation requires to keep the low level of the input signal to RESET terminal until the stabilized oscillation of the internal oscillator. Therefore the constants on the reset circuit must be decided in accordance with the characteristics of the clock generator circuit.

### [ An example of Power On Reset circuit ]



$R^*$ : A resistor is RESET terminal protector. It is required depending on the condition of an application.

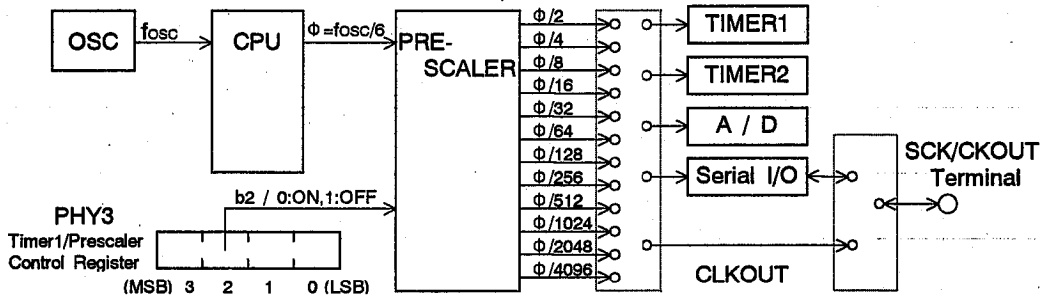
## ■ PRESCALER

The NJU3503 prepares a built-in Prescaler consisted of 12-bit binary counter which counts the machine cycle period clock( $1/f_{osc} \times 6$ ) from 2 to 4096 times. The Prescaler can supply the clock to Timer1 and 2, Serial Input Output, A/D converter, and the external application through the "SCK/CKOUT" terminal. A frequency of the clock can be selected from 12 kinds shown in follows.

1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512, 1/1024, 1/2048, 1/4096

When the bit2(b2) of Timer1/Prescaler control register(PHY3) is set to "1", the Prescaler operation is stopped, but the output clock is also stopped to Timer1 and 2, Serial Input Output, A/D converter and the external application through the "SCK/CKOUT" terminal. When the b2 of PHY3 is set to "0", the Prescaler operation is started to count from "0".

[ AROUND THE PRESCALER BLOCK DIAGRAM ]



EX.) The output frequency of Prescaler at  $f_{osc} = 4\text{MHz}$  ( $\Phi = 4\text{MHz}/6$ )

Prescaler Divider	Output Frequency
$\Phi/2$	333.33kHz
$\Phi/4$	166.67kHz
$\Phi/8$	83.33kHz
$\Phi/16$	41.67kHz
$\Phi/32$	20.83kHz
$\Phi/64$	10.42kHz
$\Phi/128$	5.21kHz
$\Phi/256$	2.60kHz
$\Phi/512$	1.30kHz
$\Phi/1024$	651kHz
$\Phi/2048$	326kHz
$\Phi/4096$	163kHz

**■ ABSOLUTE MAXIMUM RATINGS**

(Ta=25°C)

P A R A M E T E R	S Y M B O L	R A T I N G S	U N I T
Supply Voltage	V <sub>DD</sub>	-0.3~+7.0	V
Input Voltage	V <sub>IN</sub>	-0.3~V <sub>DD</sub> +0.3	V
Output Voltage	V <sub>OUT</sub>	-0.3~V <sub>DD</sub> +0.3	V
Analog Supply Voltage	AV <sub>DD</sub>	-0.3~V <sub>DD</sub> +0.3	V
Analog Reference Voltage	V <sub>REF</sub>	-0.3~AV <sub>DD</sub> +0.3	V
Analog Input Voltage	AIN0~AIN5	-0.3~AV <sub>DD</sub> +0.3	V
Operating Temperature	T <sub>opr</sub>	-20~+75	°C
Storage Temperature	T <sub>stg</sub>	-55~+125	°C

**■ ELECTRICAL CHARACTERISTICS**
**DC CHARACTERISTICS 1-1**
 $(V_{DD}=3.6\sim 5.5V, V_{SS}=0V, T_a=-20\sim 75^{\circ}C)$ 

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE	
Supply Voltage	$V_{DD}$	$V_{DD}$	3.6		5.5	V		
Supply Current	$I_{DD1}$	$V_{DD}$ $V_{DD}=5V, f_{osc}=2MHz$ X'tal Oscillation In Reset		0.8	1.2	mA	*3	
	$I_{DD2}$	$V_{DD}$ $V_{DD}=5V, f_{osc}=2MHz$ Ceramic Oscillation In Reset		0.8	1.2	mA	*3	
	$I_{DD3}$	$V_{DD}$ $V_{DD}=5V, f_{osc}=2MHz$ CR Oscillation In Reset		1.1	1.6	mA	*3	
	$I_{DD4}$	$V_{DD}$ $V_{DD}=5V, f_{osc}=4MHz$ Operating (Except ADC)		2.4	3.6	mA	*3	
	$I_{DD5}$	$V_{DD}$ $V_{DD}=5V, STANDBY Mode$				4.0	$\mu A$	*3
	$I_{ADD}$	$AV_{DD}$ $AV_{DD}=V_{DD}=5V, ADCK=225kHz$			3.0	5.0	mA	*3
High-Level Input Voltage	$V_{IH1}$	PA0~PA3, AIN0/PD0~AIN3/PD3, AIN4/PE0, AIN5/PE1, PE2, SDI(O)/PG1, SCK/CKOUT	$0.7V_{DD}$		$V_{DD}$	V	*1	
	$V_{IH2}$	PB0~PB2, ADCK/PC0, $V_{REF}/PC1, EXTI/PF0,$ CNTI/PF1, RESET	$0.8V_{DD}$		$V_{DD}$	V	*1	
	$V_{IH3}$	OSC1	$V_{DD}-1.0$		$V_{DD}$	V		
Low-Level Input Voltage	$V_{IL1}$	PA0~PA3, AIN0/PD0~AIN3/PD3, AIN4/PE0, AIN5/PE1, PE2, SDI(O)/PG1, SCK/CKOUT	0		$0.3V_{DD}$	V	*1	
	$V_{IL2}$	PB0~PB2, ADCK/PC0, $V_{REF}/PC1, EXTI/PF0,$ CNTI/PF1, RESET	0		$0.2V_{DD}$	V	*1	
	$V_{IL3}$	OSC1	0		1.0	V		

\*1 Input/output port is set as an Input terminal.

\*2 Input/output port is set as an Output terminal.

\*3 Except the current through Pull-up resistor.

**■ ELECTRICAL CHARACTERISTICS**
**DC CHARACTERISTICS 1-2**
 $(V_{DD}=3.6\sim 5.5V, V_{SS}=0V, T_a=-20\sim 75^{\circ}C)$ 

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
High-Level Input Current	$I_{IH1}$	$V_{DD}=5.5V, V_{IN}=5.5V$ PA0~PA3, PB0~PB2, ADCK/PC0, $V_{REF}/PC1$ , AIN0/PD0~AIN3/PD3, AIN4/PE0, AIN5/PE1, PE2, EXTI/PF0, CNTI/PF1, SDI(O)/PG1, RESET			10	$\mu A$	*1
Low-Level Input Current	$I_{IL1}$	$V_{DD}=5.5V, V_{IN}=0V$ Without Pull-up Resistance PA0~PA3, PB0~PB2, ADCK/PC0, $V_{REF}/PC1$ , AIN0/PD0~AIN3/PD3, AIN4/PE0, AIN5/PE1, PE2, EXTI/PF0, CNTI/PF1, SDI(O)/PG1, RESET			-10	$\mu A$	*1
	$I_{IL2}$	$V_{DD}=5.5V, V_{IN}=0V$ With Pull-up Resistance PA0~PA3, PB0~PB2, ADCK/PC0, $V_{REF}/PC1$ , AIN0/PD0~AIN3/PD3, AIN4/PE0, AIN5/PE1, PE2, EXTI/PF0, CNTI/PF1, SDI(O)/PG1, RESET			-100	$\mu A$	*1
High-Level Output Voltage	$V_{OH}$	$I_{OH}=-100\mu A$ PB0~PB2, SDO/PG0, SDI(O)/PG1, SCK/CKOUT	$V_{DD}-0.5$			V	*2
Low-Level Output Voltage	$V_{OL1}$	$I_{OL1}=400\mu A$ PB0~PB2, SDO/PG0, SDI(O)/PG1, SCK/CKOUT			0.5	V	*2
	$V_{OL2}$	$I_{OL2}=15mA$ PA0~PA3, AIN0/PD0~AIN3/PD3, AIN4/PE0, AIN5/PE1, PE2			2.0	V	*2
Output Leakage Current	$I_{OD}$	$V_{DD}=5.5V, V_{OH}=5.5V$ PA0~PA3, AIN0/PD0~AIN3/PD3, AIN4/PE0, AIN5/PE1, PE2,			10	$\mu A$	*2
Input Capacitance	$C_{IN}$	Except $V_{DD}, V_{SS}$ terminals $f_{OSC}=1MHz$		10	20	pF	

\*1 Input/output port is set as an Input terminal.

\*2 Input/output port is set as an Output terminal.

**■ ELECTRICAL CHARACTERISTICS**
**DC CHARACTERISTICS 2-1**
 $(V_{DD}=2.4\sim 3.6V, V_{SS}=0V, T_a=-20\sim 75^{\circ}C)$ 

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	$V_{DD}$	$V_{DD}$	2.4		3.6	V	
Supply Current	$I_{DD1}$	$V_{DD}$ $V_{DD}=3V, f_{osc}=1MHz$ X'tal Oscillation In Reset		0.3	0.5	mA	*3
	$I_{DD2}$	$V_{DD}$ $V_{DD}=3V, f_{osc}=1MHz$ Ceramic Oscillation In Reset		0.3	0.5	mA	*3
	$I_{DD3}$	$V_{DD}$ $V_{DD}=3V, f_{osc}=1MHz$ CR Oscillation In Reset		0.4	0.6	mA	*3
	$I_{DD4}$	$V_{DD}$ $V_{DD}=3V, f_{osc}=2MHz$ Operating (Except ADC)		0.6	1.0	mA	*3
	$I_{DD5}$	$V_{DD}$ $V_{DD}=3V, \text{STANDBY Mode}$			2.0	$\mu A$	*3
	$I_{ADD}$	$AV_{DD}$ $AV_{DD}=V_{DD}=3V, ADCK=225kHz$			2.5	3.5	mA
High-Level Input Voltage	$V_{IH1}$	PA0~PA3, AIN0/PD0~AIN3/PD3, AIN4/PE0, AIN5/PE1, PE2, SDI(O)/PG1, SCK/CKOUT	$0.8V_{DD}$		$V_{DD}$	V	*1
	$V_{IH2}$	PB0~PB2, ADCK/PC0, $V_{REF}/PC1$ , EXTI/PF0, CNTI/PF1, RESET	$0.85V_{DD}$		$V_{DD}$	V	*1
	$V_{IH3}$	OSC1	$V_{DD}-0.3$		$V_{DD}$	V	
Low-Level Input Voltage	$V_{IL1}$	PA0~PA3, AIN0/PD0~AIN3/PD3, AIN4/PE0, AIN5/PE1, PE2, SDI(O)/PG1, SCK/CKOUT	0		$0.2V_{DD}$	V	*1
	$V_{IL2}$	PB0~PB2, ADCK/PC0, $V_{REF}/PC1$ , EXTI/PF0, CNTI/PF1, RESET	0		$0.15V_{DD}$	V	*1
	$V_{IL3}$	OSC1	0		0.3	V	

\*1 Input/output port is set as an Input terminal.

\*2 Input/output port is set as an Output terminal.

\*3 Except the current through Pull-up resistor.

**■ ELECTRICAL CHARACTERISTICS**
**DC CHARACTERISTICS 2-2**
 $(V_{DD}=2.4\sim 3.6V, V_{SS}=0V, T_a=-20\sim 75^{\circ}C)$ 

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
High-Level Input Current	$I_{IH}$	$V_{DD}=3.6V, V_{IN}=3.6V$ PA0~PA3, PB0~PB2, ADCK/PC0, $V_{REF}/PC1$ , AIN0/PD0~AIN3/PD3, AIN4/PE0, AIN5/PE1, PE2, EXTI/PF0, CNTI/PF1, SDI(O)/PG1, RESET			10	$\mu A$	*1
Low-Level Input Current	$I_{IL1}$	$V_{DD}=3.6V, V_{IN}=0V$ Without Pull-up Resistance PA0~PA3, PB0~PB2, ADCK/PC0, $V_{REF}/PC1$ , AIN0/PD0~AIN3/PD3, AIN4/PE0, AIN5/PE1, PE2, EXTI/PF0, CNTI/PF1, SDI(O)/PG1, RESET			-10	$\mu A$	*1
	$I_{IL2}$	$V_{DD}=3.6V, V_{IN}=0V$ With Pull-up Resistance PA0~PA3, PB0~PB2, ADCK/PC0, $V_{REF}/PC1$ , AIN0/PD0~AIN3/PD3, AIN4/PE0, AIN5/PE1, PE2, EXTI/PF0, CNTI/PF1, SDI(O)/PG1, RESET			-100	$\mu A$	*1
High-Level Output Voltage	$V_{OH}$	$I_{OH}=-80\mu A$ PB0~PB2, SDO/PG0, SDI(O)/PG1, SCK/CKOUT	$V_{DD}-0.5$			V	*2
Low-Level Output Voltage	$V_{OL1}$	$I_{OL1}=350\mu A$ PB0~PB2, SDO/PG0, SDI(O)/PG1, SCK/CKOUT			0.5	V	*2
	$V_{OL2}$	$I_{OL2}=5mA$ PA0~PA3, AIN0/PD0~AIN3/PD3, AIN4/PE0, AIN5/PE1, PE2			1.0	V	*2
Output Leakage Voltage	$I_{OD}$	$V_{DD}=3.6V, V_{OH}=3.6V$ PA0~PA3, AIN0/PD0~AIN3/PD3, AIN4/PE0, AIN5/PE1, PE2			10	$\mu A$	*2
Input Capacitance	$C_{IN}$	Except $V_{DD}, V_{SS}$ terminals $f_{OSC}=1MHz$		10	20	pF	

\*1 Input/output port is set as an Input terminal.

\*2 Input/output port is set as an Output terminal.

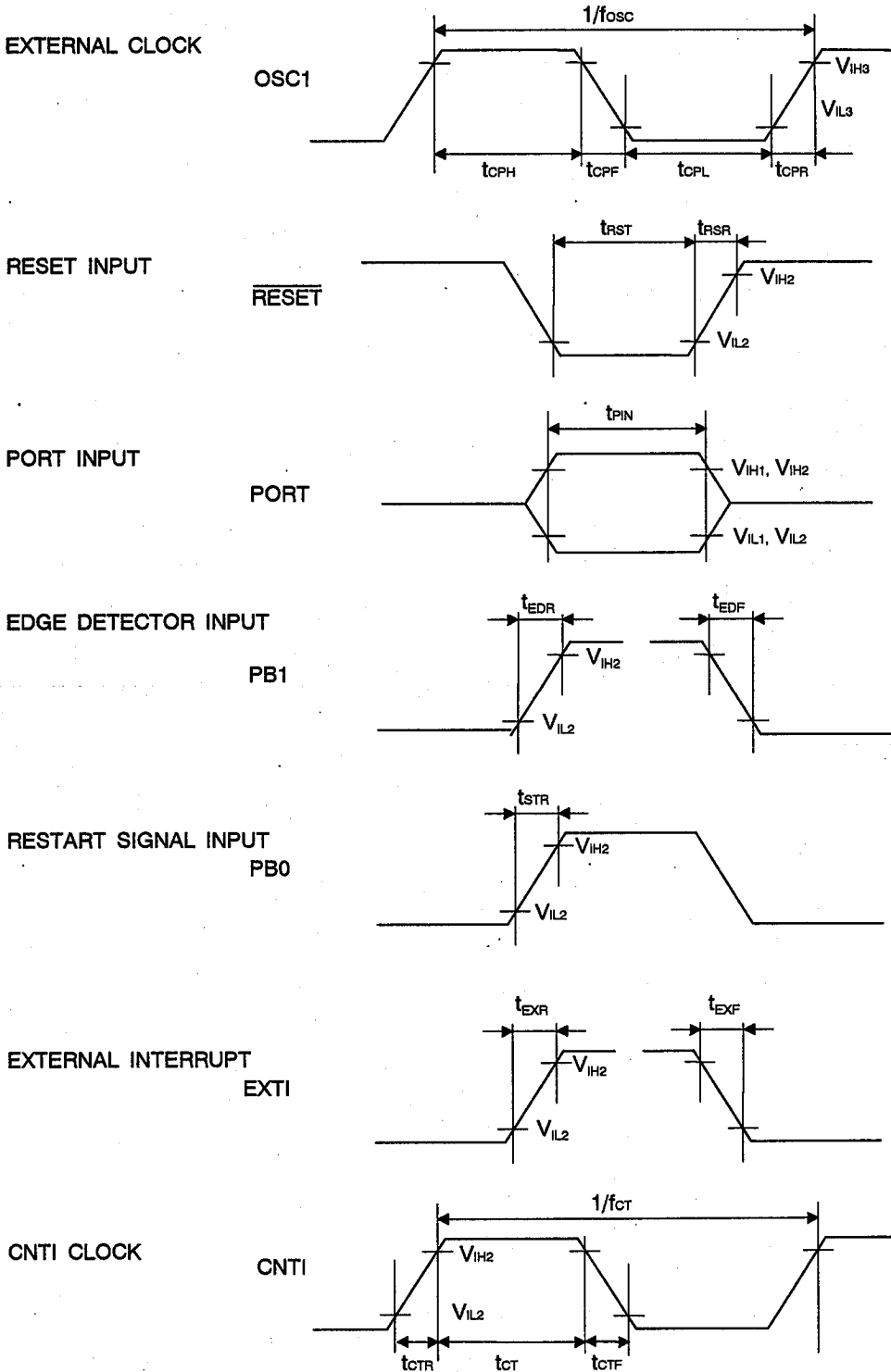


**■ ELECTRICAL CHARACTERISTICS**
**AC CHARACTERISTICS 1**

 (V<sub>SS</sub>=0V, T<sub>a</sub>=-20~75°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Operating Frequency	f <sub>OSC</sub>	V <sub>DD</sub> =2.4~3.6V	X'tal Resonator	0.03		2.0	MHz
			Ceramic Resonator	0.03		2.0	
			External Resistor Oscillation	0.03		1.0	
			External Clock	0.03		2.0	
		V <sub>DD</sub> =3.6~5.5V	X'tal Resonator	0.03		4.0	
			Ceramic Resonator	0.03		4.0	
			External Resistor Oscillation	0.03		2.0	
			External Clock	0.03		4.0	
Instruction Cycle Time	t <sub>C</sub>			/	6/f <sub>OSC</sub>	/	s
External Clock	t <sub>CPH</sub>	V <sub>DD</sub> =2.4~3.6V	250		16600		ns
Pulse Width	t <sub>CPL</sub>	V <sub>DD</sub> =3.6~5.5V	125		16600		ns
External Clock Rise Time Fall Time	t <sub>CPR</sub> t <sub>CPF</sub>	V <sub>DD</sub> =2.4~5.5V			20		ns
RESET Low-Level Width	t <sub>RST</sub>	V <sub>DD</sub> =2.4~5.5V	4/f <sub>OSC</sub>				s
RESET Rise Time	t <sub>RSR</sub>	V <sub>DD</sub> =2.4~5.5V			20		ms
Port Input Level Width	t <sub>PIN</sub>	V <sub>DD</sub> =2.4~5.5V	6/f <sub>OSC</sub>				s
Edge Detection Rise Time Fall Time	t <sub>EDR</sub> t <sub>EDF</sub>	V <sub>DD</sub> =2.4~5.5V PB1 terminal			200		ns
Restart Signal Rise Time	t <sub>STR</sub>	V <sub>DD</sub> =2.4~5.5V PB0 terminal			200		ns
External Interrupt Signal Rise Time	t <sub>EXR</sub>	V <sub>DD</sub> =2.4~5.5V EXTI/PF0 terminal			200		ns
CNTI Clock Frequency	f <sub>CT</sub>	V <sub>DD</sub> =2.4~5.5V CNTI/PF1 terminal			f <sub>OSC</sub> /64		Hz
CNTI High Level Width	t <sub>CT</sub>	V <sub>DD</sub> =2.4~5.5V CNTI/PF1 terminal	6/f <sub>OSC</sub>				s
CNTI Rise Time Fall Time	t <sub>CTR</sub> t <sub>CTF</sub>	V <sub>DD</sub> =2.4~5.5V CNTI/PF1 terminal			200		ns

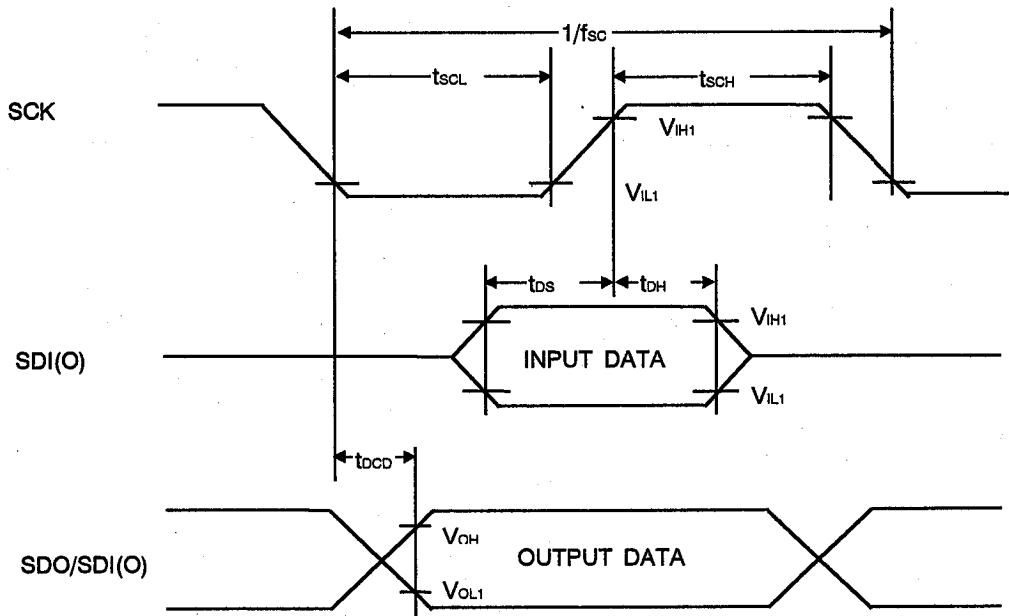
## ■ AC CHARACTERISTICS 1 TIMING CHART



**ELECTRICAL CHARACTERISTICS**
**AC CHARACTERISTICS 2 · SERIAL INTERFACE** ( $V_{DD}=2.4\sim 5.5V$ ,  $V_{SS}=0V$ ,  $T_a=-20\sim 75^\circ C$ )

PARAMETER	SYMBOL	C O N D I T I O N S		MIN	TYP	MAX	UNIT
Serial Operating Frequency	$f_{sc}$	Internal Clock				$(1/12)f_{osc}^*$	kHz
		External Clock				500	
Clock Pulse Width Low-Level	$t_{scl}$	Internal Clock	$V_{DD}=2.4\sim 3.6V$ $f_{osc}=2MHz$	3.0			$\mu s$
			$V_{DD}=3.6\sim 5.5V$ $f_{osc}=4MHz$	1.5			
		External Clock		1.0			
Clock Pulse Width High-Level	$t_{sch}$	Internal Clock	$V_{DD}=2.4\sim 3.6V$ $f_{osc}=2MHz$	3.0			$\mu s$
			$V_{DD}=3.6\sim 5.5V$ $f_{osc}=4MHz$	1.5			
		External Clock		1.0			
SDI setup Time To SCK ↑	$t_{ds}$			0.5			$\mu s$
SDI Hold time To SCK ↑	$t_{dh}$			0.5			$\mu s$
SDO Data Fix Time To SCK ↓	$t_{dcd}$					0.5	$\mu s$

\* The maximum frequency of the internal serial clock  $f_{sc}$  is selected the one-divided out put of the prescaler by the mask option.

**AC CHARACTERISTICS 2 SERIAL INTERFACE TIMING CHART**


■ **ELECTRICAL CHARACTERISTICS**  
**A/D CONVERTER CHARACTERISTICS**

( $V_{DD}=AV_{DD}=2.4\sim 5.5V$ ,  $V_{SS}=0V$ ,  $T_a=25^\circ C$ ,  $f_{osc}=4MHz$ )

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Resolution	-		-	8	-	bits
Absolute Accuracy	-	$V_{DD}=5V, AV_{DD}=5V, V_{REF}=5V$			$\pm 2$	LSB
Conversion time	$t_{CONV}$	$V_{DD}=5V, AV_{DD}=5V, V_{REF}=5V$	40			$\mu s$
Reference Voltage	$V_{REF}$		2.4		$AV_{DD}$	V
Analog Input Voltage	$V_{IA}$		$V_{SS}$		$V_{REF}$	V
ADCK frequency	$f_{ADCK}$				225	kHz

## ■ MASK OPTION

The NJU3503 can set or select the following options by the mask option as same as the mask of program coding in ROM.

### 1) INPUT OUTPUT Terminal Selection

All of input-output terminals select a type for each port from the following table1 to table2 by the mask option.  
[ CIRCUIT TYPE TABLE 1 ]

SYMBOL	TERMINAL TYPES						REMARKS
	Input/ Output Terminal *1			EXTRA FUNCTION			
	Port of Input	Port of Output	Programmable Input / Output				
PA0			IOP IO				
PA1			IOP IO				
PA2			IOP IO				
PA3			IOP IO				
PB0	ISP IS	OC			Restart signal input	E D	Restart signal input Not Restart
PB1	ISP IS	OC			Edge detector	R F D	Rising edge detector Falling edge detector Not edge detector
PB2	ISP IS	OC					
ADCK / PC0	ISP IS			ACP AC	External clock input		
V <sub>REF</sub> / PC1	ISP IS			AD	Reference input		
AIN0 / PD0	ICP IC	ONP ON		AD	Analog input (AIN0)		
AIN1 / PD1	ICP IC	ONP ON		AD	Analog input (AIN1)		
AIN2 / PD2	ICP IC	ONP ON		AD	Analog input (AIN2)		
AIN3 / PD3	ICP IC	ONP ON		AD	Analog input (AIN3)		
AIN4 / PE0	ICP IC	ONP ON		AD	Analog input (AIN4)		
AIN5 / PE1	ICP IC	ONP ON		AD	Analog input (AIN5)		
PE2	ICP IC	ONP ON					

Note) "IOP, IO, ISP, IS, OC, ICP, IC, ONP, ON, ACP, AC, AD, R, F, D" are symbols using on MASK OPTIONGENERATOR(MOG).

\*1) The symbol and the detail circuits of INPUT OUTPUT TERMINAL are written in INPUT OUTPUT TERMINAL TYPE.

[ CIRCUIT TYPE TABLE 2 ]

SYMBOL	TERMINAL TYPES						REMARKS	
	Input/ Output Terminal *1			EXTRA FUNCTION				
	Port of Input	Port of Output	Programmable Input / Output					
EXTI / PF0 *2	ISP IS			IIP II	External Interrupt input (EXTI)	R F	Rising edge Falling edge	
CNTI / PF1 *2	ISP IS			IIP II	External clock to Timer2 input (CNTI)			
SDO / PG0		OC		SO	Serial data output	MSB LSB	MSB first LSB first	
SDI(O) / PG1 *2	ICP IC	OC		SDP SD	Serial data input / output			
SCK / CKOUT *2 *3				SCP SC	Serial clock input-output			
				-	Output clock divide by pre-scaler			

Note) "IOP,IO,AD,ICP,ONP,ON,OC,ISP,IS,AD,R,F,IIP,II,SO,SCP," are symbols using on MASK OPTIN GENERATOR(MOG).

\*1) The symbol and the detail circuits of INPUT OUTPUT TERMINAL are written in INPUT OUTPUT TERMINAL TYPE.

\*2) The pull-up resistance is added to the terminal selected as the extra function.

\*3) When Serial INPUT-OUTPUT is selected, "SCK" is selected automatically. When it is not selected, "CKOUT" is selected automatically.

**INPUT OUTPUT TERMINAL TYPES**

	Types	With Pull-up	Without Pull-up	Terminals
INPUT TERMINAL	C-MOS	Type ICP 	Type IC 	AIN0/PD0~ AIN3/PD3, AIN4/PE0, AIN5/PE1, PE2, SDI(O)/PG1
	SCHMITT TRIGGER	Type ISP 	Type IS 	PB0~PB2, ADCK/PC0, V <sub>REF</sub> /PC1, EXTI/PF0, CNT1/PF1
OUTPUT TERMINAL	C-MOS	/		PB0~PB2, SDO/PG0, SDI(O)/PG1
	N-channel (Nch) OPEN DRAIN	Type ONP 	Type ON 	AIN0/PD0~ AIN3/PD3, AIN4/PE0, AIN5/PE1, PE2
PROGRAMMABLE INPUT OUTPUT TERMINAL	C-MOS INPUT / N-channel (Nch) OPEN DRAIN OUTPUT	Type IOP 	Type IO 	PA0~PA3

**② Re-start signal Input Selection**

PB0 terminal performs the extra function as the re-start signal input terminal to return from the "STANDBY" mode. When the rising edge of the signal from the external circuit is input into the PB0 terminal in mode of "STANDBY", the "STANDBY" mode is released and the CPU starts the execution again from the suspended address of the program.

**③ Edge Detector Selection**

PB1 terminal performs the extra function as the edge detector terminal. When the PB1 terminal detects the edge of the signal from the external circuit, the third bit(b2) condition of PHY18 is set to "1". The "b2" of PHY18 is set to "1" even when the edge is input during the "STANDBY" mode. The condition of "b2" is kept until the writing operation to PHY18.

The polarity as low to high or high to low of the input signal edge can be selected by the mask option.


**④ External Interrupt of the edge Selection**

When PF0 terminal operates as EXTI Input terminal for the external interrupt, the polarity of the edge, rising as "low to high" or falling as "high to low", is selected by the mask option.


**⑤ The data order(MSB, LSB) of the Serial Interface**

The data order of the Serial Interface can select either MSB or LSB first by the mask option.

**⑥ A/D Control Clock**

A/D Control Clock can select either the external clock from ADCK terminal or the internal clock from the Pre-scaler by the mask option.

**⑦ Each Internal Clock**

The count clocks of Timer1 and Timer2, the Internal shift clock of the Serial Interface, the clock of the A/D control clock and the output clock through the SCK/CKOUT terminal are clocks divided in the internal pre-scaler, and the frequency of this clock can be selected by the mask option from follows which are dividing numbers based on the inverse of the 1-instruction executing period (1/fOSC x 6).

1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512, 1/1024, 1/2048, 1/4096

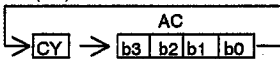
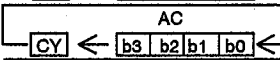
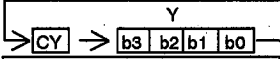
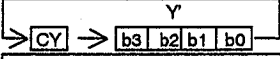
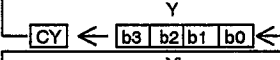
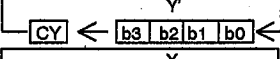
Note) Count clock of Timer2 can select the internal or external clock by the program.

The shift clock of the serial interface can select the internal or external clock by the program.



**MNEMONIC LIST**

	Mnemonic	Operation code	Function	Status	Cycle	Memo
DATA TRANSFERENCE	TAY	04	Y←AC	1	1	RPC=0
			Y←AC	1	1	RPC=1
	TYA	14	AC←Y	1	1	RPC=0
			AC←Y'	1	1	RPC=1
	XAX	1B	AC**X	1	1	RPC=0
			AC**X'	1	1	RPC=1
	TAP	26	PH(Y)←AC	1	1	
	TPA	16	AC←PH(Y)	1	1	
	TAPICY	17	PH(Y)←AC, Y←Y+1	*	1	
	TAPDCY	27	PH(Y)←AC, Y←Y-1	*	1	
	TMA	0D	AC←M(X, Y)	1	1	
	TAM	1D	M(X, Y)←AC	1	1	
	TAMICY	0A	M(X, Y)←AC, Y←Y+1	*	1	
	TAMDCY	1A	M(X, Y)←AC, Y←Y-1	*	1	
	TMY	05	Y←M(X, Y)	1	1	RPC=0
			Y←M(X, Y)	1	1	RPC=1
	XMA	0B	AC**M(X, Y)	1	1	
	TPMICY	03	M(X, Y)←PH(Y), Y←Y+1	*	1	
	TMPICY	13	PH(Y)←M(X, Y), Y←Y+1	*	1	
	TRM	23	M(X, Y)←ROM(PHY13, X, AC)	1	2	Y=an odd number:ROM of 4bit hi-data Y=an even number:ROM of 4bit low-data
CLA	80	AC←0	1	1		
LDI A, #K	80~8F	AC←#K	1	1	#K=0~15	
LDI Y, #K	90~9F	Y←#K	1	1	RPC=0, #K=0~15	
		Y←#K	1	1	RPC=1, #K=0~15	
LDI X, #K	A0~AF	X←#K	1	1	RPC=0, #K=0~15	
		X←#K	1	1	RPC=1, #K=0~15	
CALCULATING	ADD A, M	0E	AC←AC+M(X, Y)	*	1	
	INC A	71	AC←AC+1	*	1	
	DEC A	7F	AC←AC-1	*	1	
	ADD A, #K	70~7F	AC←AC+#K	*	1	#K=0~15
	AND A, M	0F	AC←AC∧M(X, Y)	*	1	
	CMP A, M	2E	AC←>M(X, Y)	*	1	
	CMP Y, #K	B0~BF	Y←>#K	*	1	#K=0~15
	INC Y	08	Y←Y+1	*	1	RPC=0
			Y←Y+1	*	1	RPC=1
	DEC Y	18	Y←Y-1	*	1	RPC=0
			Y←Y-1	*	1	RPC=1
	INC M	09	AC←M(X, Y)+1	*	1	
	DEC M	19	AC←M(X, Y)-1	*	1	
	YNEA	01	Y←>AC	*	1	
	OR A, M	1F	AC←AC∨M(X, Y)	*	1	
	XOR A, M	2F	AC←AC⊕M(X, Y)	*	1	
	NEG	2D	AC←0-AC	1	1	
	SUB A, M	1E	AC←M(X, Y)-AC	*	1	
	AND A, #K	40~4F	AC←AC∧#K	*	1	#K=0~15
	OR A, #K	50~5F	AC←AC∨#K	*	1	#K=0~15

	Mnemonic	Operation code	Function	Status	Cycle	Memo	
BRANC	JPL addr	68~6F	ST=1:PC←addr,ST=0:No branch	1	2	2byte Mnemonic	
	JMP addr	C0~FF	ST=1:PC←addr,ST=0:No branch	1	1		
	CALL addr	60~67	ST=1:(SP)←PC+2,SP←SP+1,PC←addr ST=0:No branch	1	2	2byte Mnemonic	
	RET	2B	PC←(SP),SP←SP-1	1	1		
	RETI	2C	PC←(SP),AC←(SP),SP←SP-1 X←(SP), X'←(SP), Y←(SP), Y'←(SP) RPC←(SP),ST←(SP)	*	1		
	BIT OPERATI	SBIT b	30~33	M(X,Y)b←1	1	1	b=0~3
RBIT b		34~37	M(X,Y)b←0	1	1	b=0~3	
TBIT b		38~3B	ST←M(X,Y)b	*	1	b=0~3	
TBA b		3C~3F	ST←(AC)b	*	1	b=0~3	
RAR		21		*	1		
RAL		22		*	1		
RXR		24		*	1	RPC=0	
RYL		25		*	1	RPC=1	
RXL		28		*	1	RPC=0	
RRPC		20		*	1	RPC=1	
SEC		0C	CY←1	1	1	RPC=0	
CLC		1C	CY←0	0	1	RPC=1	
SRPC		10	RPC←1	1	1	RPC=0	
RRPC		20	RPC←0	1	1	RPC=1	
SPECIAL		NOP	00	No Operation	1	1	
		HLT	07	CPU Halted	1	1	
	MDT	06	Memory Dump Test	-	-		

※

← :Transfer direction  
 ^ :AND  
 v :OR  
 ⊕ :Exclusive OR  
 + :Add  
 - :Subtraction  
 < > :Comparison

AC :Accumulator  
 X :Xregister  
 X' :X'register  
 Y :Yregister  
 Y' :Y'register  
 PH :Peripheral register  
 M :Data memory  
 ROM :Program memory  
 PC :Program counter

SP :Stack pointer  
 RPC :RPC flag  
 CY :Carry flag  
 ST :Status flag  
 #K :Immediate data  
 addr :Blanch address  
 ( ) :A content of register or memory pointed by the address indicated in ( ).  
 b :Bit position

※Status description

0:After the command execution, ST-flag is always set to "0".

1:After the command execution, ST-flag is always set to "1".

\*:Status

## MEMO

[CAUTION]

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.