PRELIMINARY

4-BIT SINGLE CHIP OTP MICRO CONTROLLER

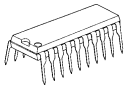
■ GENERAL DESCRIPTION

The **NJU3551** is the C-MOS 4-bit Single Chip OTP type Micro Controller with programmable Flash Memory.

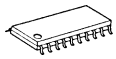
It is completely compatible with the **NJU3501** in function and the pin configuration. Therefore, the **NJU3551** is suitable for the final evaluation before **NJU3501** mask generation, the small quantity production and short lead-time.

* *In this data sheet, only OTP programming and the difference between **NJU3551** and **NJU3501** are mentioned mainly.*
*Therefore the detail function and specification should be referred on the **NJU3501** data sheet.*

■ PACKAGE OUTLINE



NJU3551D

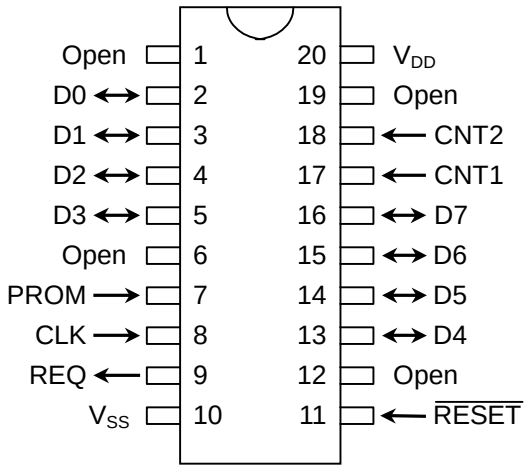


NJU3551G

■ FEATURES

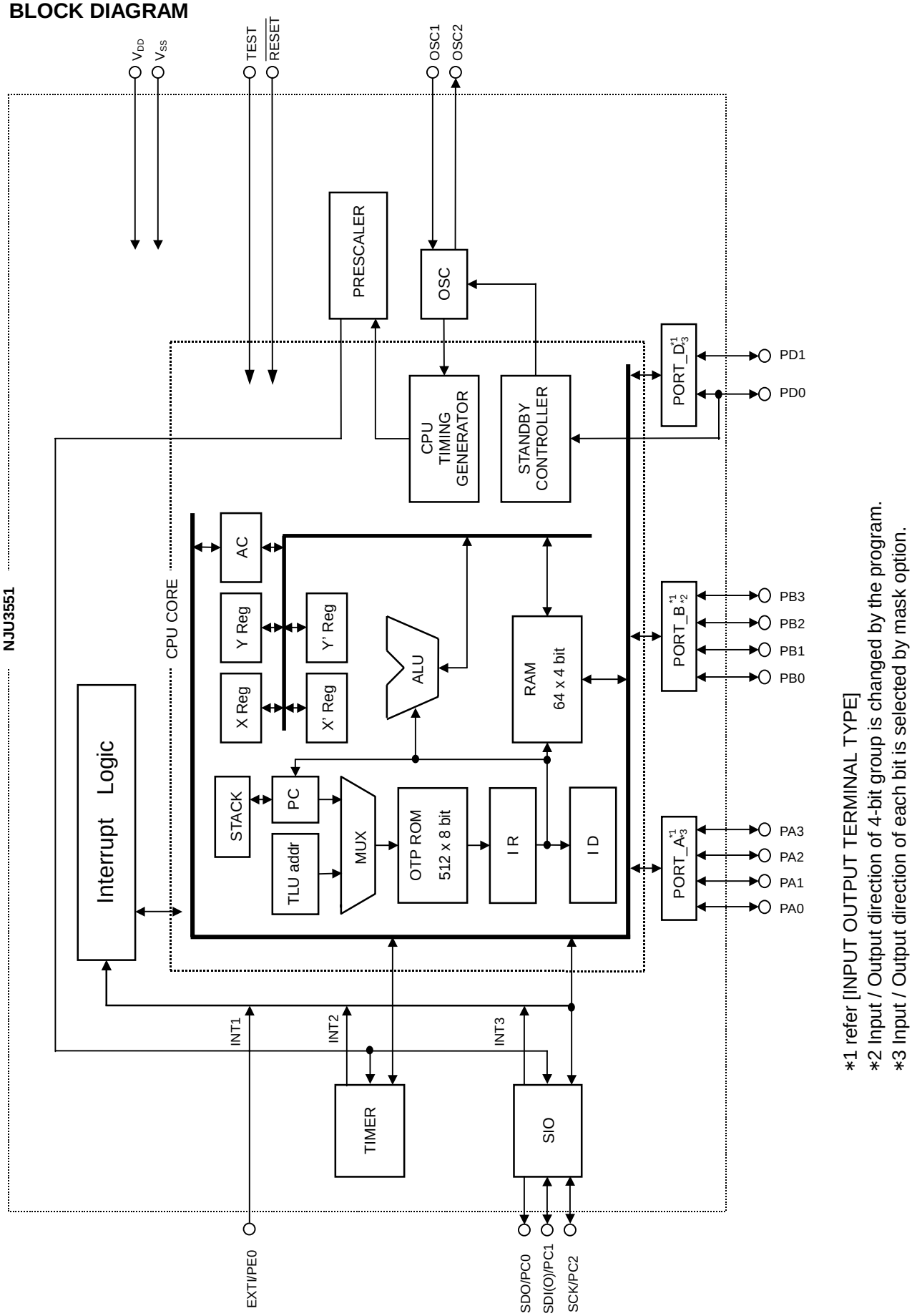
- Internal One Time Programmable ROM 512 X 8bits
- Internal Data RAM 64 X 4bits
- Wide operating voltage range 2.7V ~ 5.5V
- Package outline DIP20 / SOP20
- ROM programmer “SUPERPRO/L” by XELTEK co,.

■ PIN CONFIGURATION IN OTP PROGRAMMING MODE



Note) The pin configuration in Normal operating mode is the same as **NJU3501**.

■ BLOCK DIAGRAM



*1 refer [INPUT OUTPUT TERMINAL TYPE]
*2 Input / Output direction of 4-bit group is changed by the program.
*3 Input / Output direction of each bit is selected by mask option.

■ TERMINAL DESCRIPTION IN OTP PROGRAMMING MODE

No.	SYMBOL	INPUT/OUTPUT	F U N C T I O N
11	$\overline{\text{RESET}}$	INPUT	RESET terminal. When the low-level input-signal, the system is initialized.
2 - 5, 13 - 16	D0 - D7	INPUT/OUTPUT	Data bus
17, 18	CNT1 CNT2	INPUT INPUT	OTP control input terminal
9	REQ	OUTPUT	Request output terminal
8	CLK	INPUT	Clock input terminal
7	PROM	INPUT	OTP programming enable terminal
20	V_{DD}	-	Power Source (5V)
10	V_{SS}	-	Power Source (0V)

Note 1) Use at V_{DD}=5V in OTP programming mode.
2) Non connect anything to the other terminals.

■ Difference between NJU3551 (OTP version) and NJU3501 (MASK version)

● Operating mode

NJU3552 has two operating modes. One is "Normal operating mode" and the other is "OTP programming mode".

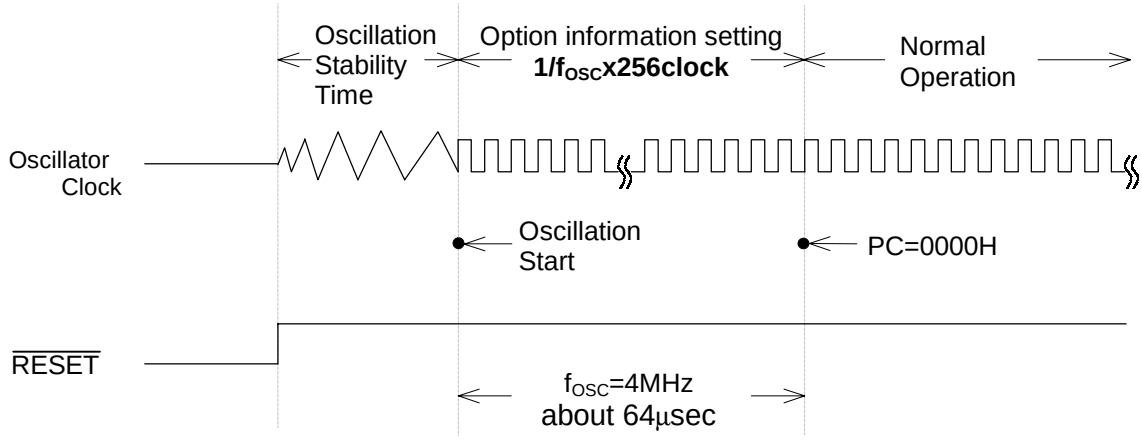
- Normal operating mode
  The "TEST" terminal is set to low level. (The terminal is recommended to connect to GND.)
  Operating voltage range; 2.7V ~ 5.5V.

- OTP Programming mode
  User program is read out from or written into the OTP by the universal programmer "SUPERPRO/L" and converting adapter made by XELTEK co,.(USA).

● Option information set in the initialization

When the initialization is performed($\overline{\text{RESET}}$ terminal is "L"), the operation information stored in option area is set as shown in the following timing chart . The option information is set in the term of **1 / f_{osc} x 256clock** after RESET releasing and oscillation stability time. After information set, the program counter is set to 0000H and the **NJU3551** operates in normal.

[TIMING CHART]



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.3 ~ +7.0	V
Input Voltage	V_{IN}	-0.3 ~ V_{DD} + 0.3	V
Output Voltage	V_{OUT}	-0.3 ~ V_{DD} + 0.3	V
Operating Temperature	T_{opr}	-20 ~ +75	°C
Storage Temperature	T_{stg}	-55 ~ +125	°C

Note)

The difference of electrical characteristics between NJU3551 (OTP version) and NJU3501 (MASK version)

		NJU3501		**NJU3551**
•Supply Voltage (V_{DD}) MIN.		2.4V	→	2.7V
•Supply Current				
5V	(I_{DD1}) Max.	4.0mA	→	30mA
	(I_{DD2}) Max.	4.0mA	→	30mA
	(I_{DD3}) Max.	3.8mA	→	30mA
	(I_{DD4}) Max.	4.0μA		20μA
3V	(I_{DD1}) Max.	2.0mA	→	20mA
	(I_{DD2}) Max.	2.0mA	→	20mA
	(I_{DD3}) Max.	1.8mA		20mA
	(I_{DD4}) Max.	2.0μA	→	20μA

■ ELECTRICAL CHARACTERISTICS DC CHARACTERISTICS 1

(V_{DD}=3.6~5.5V, V_{SS}=0V, Ta=-20~75°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{DD}	V_{DD}	3.6		5.5	V	
Supply Current	I_{DD1}	V_{DD} V_{DD}=5V, f_{OSC}=2MHz X'tal Oscillation in Reset			30	mA	*3
	I_{DD2}	V_{DD} V_{DD}=5V, f_{OSC}=2MHz Ceramic Oscillation in Reset			30	mA	*3
	I_{DD3}	V_{DD} V_{DD}=5V, f_{OSC}=2MHz CR Oscillation in Reset			30	mA	*3
	I_{DD4}	V_{DD} V_{DD}=5V, STANDBY Mode			20	μA	*3
	I_{DD5}	V_{DD} V_{DD}=5V, f_{OSC}=4MHz, Operating			30	mA	*3
High-Level Input Voltage	V_{IH1}	PA0~PA3, PB0~PB3, SDO/PC0, SDI(O)/PC1, SCK/PC2	$0.7V_{DD}$		V_{DD}	V	*1
	V_{IH2}	PD0, PD1, EXTI/PE0, $\overline{RESET}$	$0.8V_{DD}$		V_{DD}	V	*1
	V_{IH3}	OSC1	V_{DD}-1.0		V_{DD}	V	
Low-level Input Voltage	V_{IL1}	PA0~PA3, PB0~PB3, SDO/PC0, SDI(O)/PC1, SCK/PC2	0		$0.3V_{DD}$	V	*1
	V_{IL2}	PD0, PD1, EXTI/PE0, $\overline{RESET}$	0		$0.2V_{DD}$	V	*1
	V_{IL3}	OSC1	0		1.0	V	
High-Level Input Current	I_{IH}	V_{DD}=5.5V, V_{IN}=5.5V PA0~PA3, PB0~PB3, SDO/PC0, SDI(O)/PC1, SCK/PC2, PD0, PD1, EXTI/PE0, $\overline{RESET}$			10	μA	*1
Low-Level Input Current	I_{IL1}	V_{DD}=5.5V, V_{IN}=0V Without pull-up resistance PA0~PA3, PB0~PB3, SDO/PC0, SDI(O)/PC1, SCK/PC2, PD0, PD1, EXTI/PE0, $\overline{RESET}$			-10	μA	*1
	I_{IL2}	V_{DD}=5.5V, V_{IN}=0V With pull-up resistance PA0~PA3, PB0~PB3, SDO/PC0, SDI(O)/PC1, SCK/PC2, PD0, PD1, EXTI/PE0			-100	μA	*1
High-Level Output Voltage	V_{OH}	I_{OH}=-100μA PA0~PA3, SDO/PC0, SDI(O)/PC1, SCK/PC2, PD0, PD1	V_{DD}-0.5			V	*2
Low-Level Output Voltage	V_{OL1}	I_{OL1}=400μA PA0~PA3, SDO/PC0, SDI(O)/PC1, SCK/PC2, PD0, PD1			0.5	V	*2
	V_{OL2}	I_{OL2}=15mA PB0~PB3			2.0	V	*2
Output Leakage Current	I_{OD}	V_{DD}=5.5V, V_{OH}=5.5V PB0~PB3			10	μA	*2
Input Capacitance	C_{IN}	Except V_{DD}, V_{SS} terminals f_{OSC}=1MHz Other terminals : 0V		10	20	pF	

*1 Input/output port is set as an Input terminal.
*2 Input/output port is set as an Output terminal.
*3 Except the current through Pull-up resister.

■ ELECTRICAL CHARACTERISTICS DC CHARACTERISTICS 2

(V_{DD}=2.7~3.6V, V_{SS}=0V, Ta=-20~75°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{DD}	V_{DD}	2.7		3.6	V	
Supply Current	I_{DD1}	V_{DD} V_{DD}=3V, f_{OSC}=1MHz X'tal Oscillation in Reset			20	mA	*3
	I_{DD2}	V_{DD} V_{DD}=3V, f_{OSC}=1MHz Ceramic Oscillation in Reset			20	mA	*3
	I_{DD3}	V_{DD} V_{DD}=3V, f_{OSC}=1MHz CR Oscillation in Reset			20	mA	*3
	I_{DD4}	V_{DD} V_{DD}=3V, STANDBY Mode			20	μA	*3
	I_{DD5}	V_{DD} V_{DD}=3V, f_{OSC}=2MHz, Operating			20	mA	*3
High-Level Input Voltage	V_{IH1}	PA0~PA3, PB0~PB3, SDO/PC0, SDI(O)/PC1, SCK/PC2	0.8V_{DD}		V_{DD}	V	*1
	V_{IH2}	PD0, PD1, EXTI/PE0, $\overline{RESET}$	0.85V_{DD}		V_{DD}	V	*1
	V_{IH3}	OSC1	V_{DD}-0.3		V_{DD}	V	
Low-level Input Voltage	V_{IL1}	PA0~PA3, PB0~PB3, SDO/PC0, SDI(O)/PC1, SCK/PC2	0		0.2V_{DD}	V	*1
	V_{IL2}	PD0, PD1, EXTI/PE0, $\overline{RESET}$	0		0.15V_{DD}	V	*1
	V_{IL3}	OSC1	0		0.3	V	
High-Level Input Current	I_{IH}	V_{DD}=3.6V, V_{IN}=3.6V PA0~PA3, PB0~PB3, SDO/PC0, SDI(O)/PC1, SCK/PC2, PD0, PD1, EXTI/PE0, $\overline{RESET}$			10	μA	*1
Low-Level Input Current	I_{IL1}	V_{DD}=3.6V, V_{IN}=0V Without pull-up resistance PA0~PA3, PB0~PB3, SDO/PC0, SDI(O)/PC1, SCK/PC2, PD0, PD1, EXTI/PE0, $\overline{RESET}$			-10	μA	*1
	I_{IL2}	V_{DD}=3.6V, V_{IN}=0V With pull-up resistance PA0~PA3, PB0~PB3, SDO/PC0, SDI(O)/PC1, SCK/PC2, PD0, PD1, EXTI/PE0			-100	μA	*1
High-Level Output Voltage	V_{OH}	I_{OH}=-80μA PA0~PA3, SDO/PC0, SDI(O)/PC1, SCK/PC2, PD0, PD1	V_{DD}-0.5			V	*2
Low-Level Output Voltage	V_{OL1}	I_{OL1}=350μA PA0~PA3, SDO/PC0, SDI(O)/PC1, SCK/PC2, PD0, PD1			0.5	V	*2
	V_{OL2}	I_{OL2}=5mA PB0~PB3			1.0	V	*2
Output Leakage Current	I_{OD}	V_{DD}=3.6V, V_{OH}=3.6V PB0~PB3			10	μA	*2
Input Capacitance	C_{IN}	Except V_{DD}, V_{SS} terminals f_{OSC}=1MHz Other terminals : 0V		10	20	pF	

*1 Input/output port is set as an Input terminal.
*2 Input/output port is set as an Output terminal.
*3 Except the current through Pull-up resister.

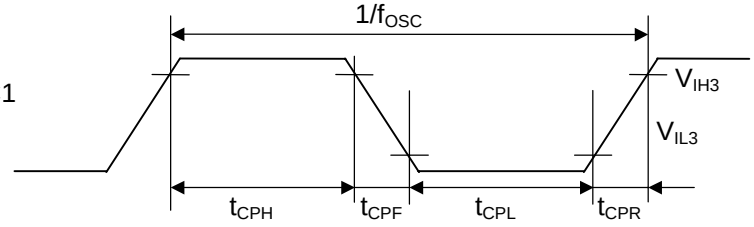
■ ELECTRICAL CHARACTERISTICS AC CHARACTERISTICS 1

(V_{SS}=0V, Ta= -20~75°C)

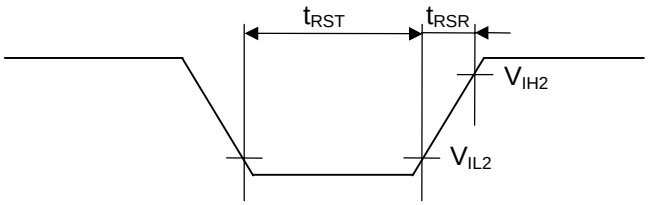
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Operating Frequency	f_{OSC}	V_{DD}=2.7~3.6V	X'tal Resonator	0.03		2.0	MHz
			Ceramic Resonator	0.03		2.0	
			External Resistor Oscillation	0.03		1.0	
			External Clock	0.03		2.0	
		V_{DD}=3.6~5.5V	X'tal Resonator	0.03		4.0	
			Ceramic Resonator	0.03		4.0	
			External Resistor Oscillation	0.03		2.0	
			External Clock	0.03		4.0	
Instruction Cycle Time	t_C				$6/f_{OSC}$		s
External Clock Pulse Width	t_{CPH}	V_{DD}=2.7~3.6V		250		16600	ns
	t_{CPL}	V_{DD}=3.6~5.5V		125		16600	
External Clock Rise Time Fall Time	t_{CPR} t_{CPF}	V_{DD}=2.7~5.5V				20	ns
$\overline{RESET}$ Low-Level Width	t_{RST}	V_{DD}=2.7~5.5V		$4/f_{OSC}$			s
$\overline{RESET}$ Rise Time	t_{RSR}	V_{DD}=2.7~5.5V				20	ms
Port Input Level Width	t_{PIN}	V_{DD}=2.7~5.5V		$6/f_{OSC}$			s
Edge Detection (PD1) Rise Time Fall Time	t_{EDR} t_{EDF}	V_{DD}=2.7~5.5V				200	ns
Restart Signal (PD0) Rise Time	t_{STR}	V_{DD}=2.7~5.5V				200	ns
External interrupt input (EXTI) Rise Time	t_{EXR}	V_{DD}=2.7~5.5V				200	ns

■ AC CHARACTERISTICS 1 TIMING CHART

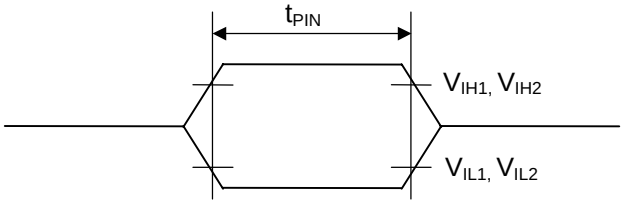
EXTERNAL CLOCK



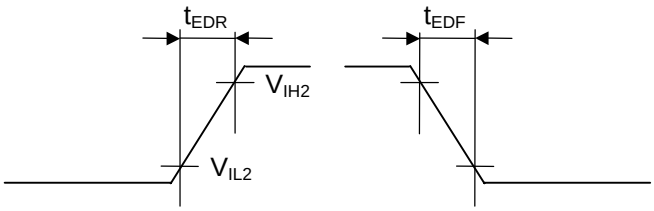
RESET INPUT



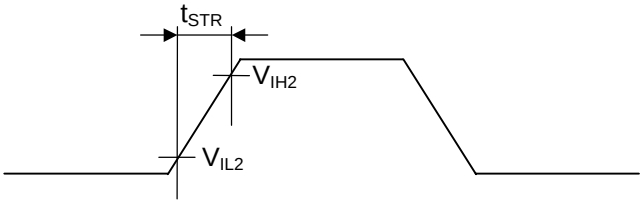
PORT INPUT



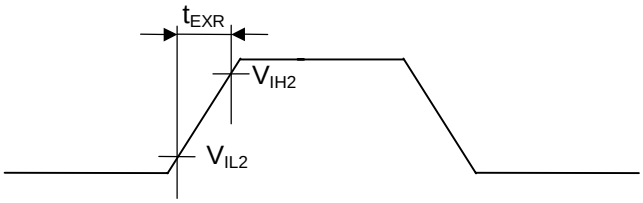
EDGE DETECTOR INPUT



RESTART SIGNAL INPUT



EXTERNAL INTERRUPT



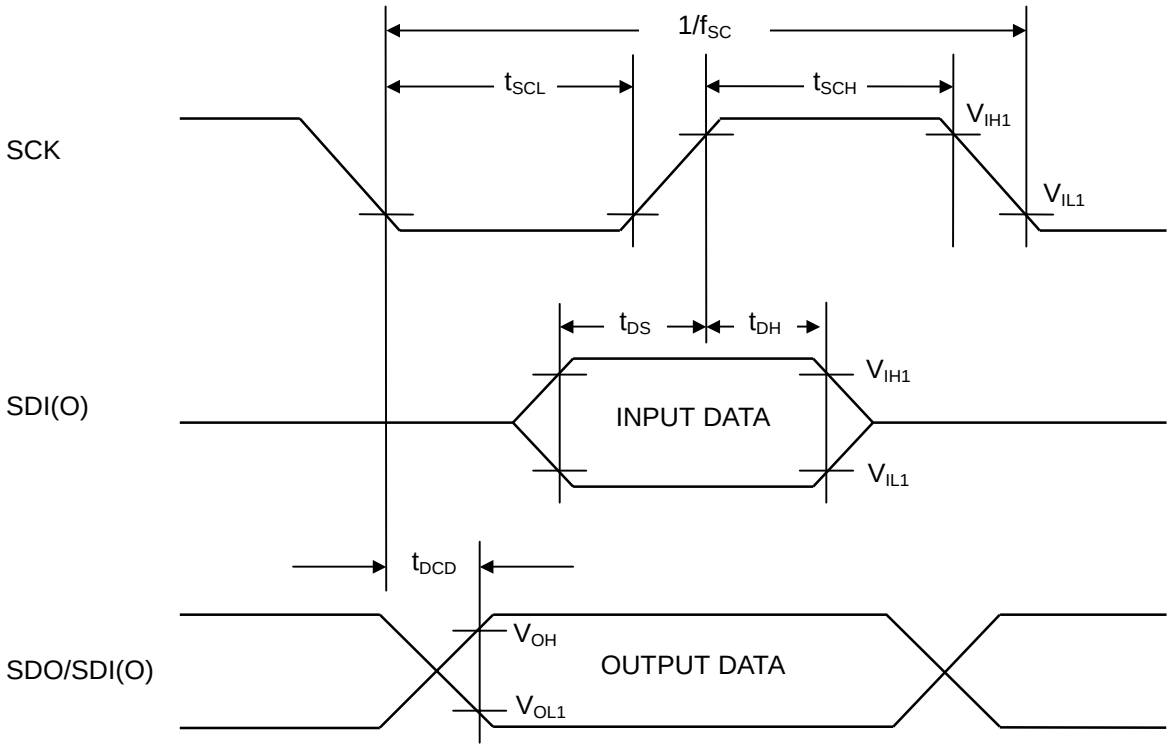
■ ELECTRICAL CHARACTERISTICS AC CHARACTERISTICS 2 SERIAL INTERFACE

(V_{SS}=0V, V_{DD}=2.7~5.5V, Ta= -20~75°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Serial Operating Frequency	f_{SC}	Internal Clock				(1/12) × f_{OSC}*	Hz
		External Clock				500k	
Clock Pulse Width Low-Level	t_{SCL}	Internal Clock	V_{DD}=2.7~3.6V f_{OSC}=2MHz	3.0			µs
			V_{DD}=3.6~5.5V f_{OSC}=4MHz	1.5			
		External Clock		1.0			
Clock Pulse Width High-Level	t_{SCH}	Internal Clock	V_{DD}=2.7~3.6V f_{OSC}=2MHz	3.0			µs
			V_{DD}=3.6~5.5V f_{OSC}=4MHz	1.5			
		External Clock		1.0			
SDI setup Time To SCK	t_{DS}			0.5			µs
SDI Hold time To SCK	t_{DH}			0.5			µs
SDO Data Fix Time To SCK	t_{DCD}					0.5	µs

* The dividing ratio of the internal clock is 1/2.

■ AC CHARACTERISTICS 2 SERIAL INTERFACE TIMING CHART



■ OPTION as same as mask version (NJU3501)

1) INPUT OUTPUT Terminal Selection
All of input-output terminals select a terminal type for each port from the following table by the mask option.

[CIRCUIT TYPE TABLE]

SYMBOL	TERMINAL TYPES					REMARKS	
	Input / Output Terminal*1			EXTRA FUNCTION			
	Port of Input	Port of Output	Programmable Input / Output				
PA0	ICP IC	OC					
PA1	ICP IC	OC					
PA2	ICP IC	OC					
PA3	ICP IC	OC					
PB0			IOP IO				
PB1			IOP IO				
PB2			IOP IO				
PB3			IOP IO				
SDO / PC0	ICP IC	OC		SO	Serial data output	MSB LSB	MSB first LSB first
SDI(O) / PC1 *2	ICP IC	OC		SDP SD	Serial data input/output		
SCK / PC2 *2	ICP IC	OC		SCP SC	Serial clock input/output		
PD0	ISP IS	OC			Restart signal input		
PD1	ISP IS	OC			Edge detection	R F	Rise edge detection Fall edge detection
EXTI / PE0 *2	ISP IS			IIP II	External interrupt input (EXTI)		

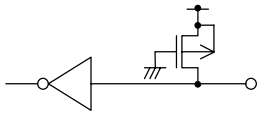
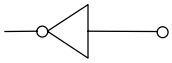
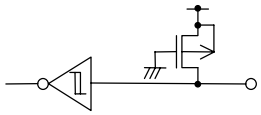
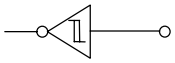
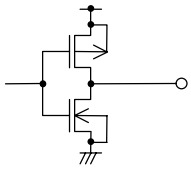
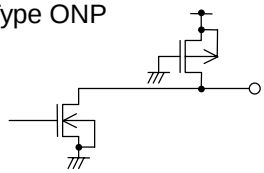
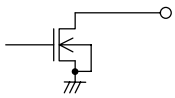
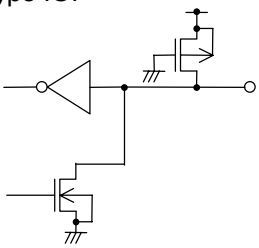
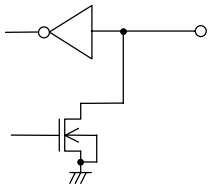
Note) The symbol in the above table is the same as in mask option generator software.
*1) The symbol and the detail circuits of INPUT OUTPUT TERMINAL are written in INPUT OUTPUT TERMINAL TYPE.
*2) The pull-up resistance is added to the terminal selected as the extra function.

[MASK OPTION LIST]

SYMBOL	FUNCTION
ICP	C-MOS input with pull-up resistance
ISP	C-MOS Schmitt trigger input with pull-up resistance
IC	C-MOS input
IS	C-MOS Schmitt trigger input
OC	C-MOS output
IIP	External interrupt input with pull-up resistance
II	External interrupt input
SDP	Serial data input/output with pull-up resistance
SD	Serial data input/output
SO	Serial data output
SCP	Serial clock input/output with pull-up resistance
SC	Serial clock input/output
IOP	Programmable input/output with pull-up resistance
IO	Programmable input/output
R	Rise edge detection
F	Fall edge detection

SYMBOL	FUNCTION
MSB	Serial data order MSB first
LSB	Serial data order LSB first
1	1/2
2	1/4
3	1/8
4	1/16
5	1/32
6	1/64
7	1/128
8	1/256
9	1/512
a	1/1024
b	1/2048
c	1/4096

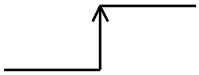
[INPUT OUTPUT TERMINAL TYPE]

	Types	With Pull-up	Without Pull-up	Terminals
INPUT TERMINAL	C-MOS	Type ICP 	Type IC 	PA0~PA3, SDO/PC0, SDI(O)/PC1, SCK/PC2
	SCHMITT TRIGGER	Type ISP 	Type IS 	PD0, PD1, EXTI/PE0
OUTPUT TERMINAL	C-MOS		Type ON 	PA0~PA3, SDO/PC0, SDI(O)/PC1, SCK/PC2, PD0, PD1
	N-channel(Nch) OPEN DRAIN	Type ONP 	Type ON 	
PROGRAMMABLE INPUT OUTPUT TERMINAL	C-MOS INPUT / Nch OPEN DRAIN OUTPUT	Type IOP 	Type IO 	PB0~PB3

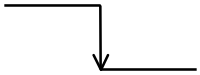
2) Edge Detector Selection

PD1 terminal is added the “Edge detect function” by the mask option.

Rising edge



Falling edge



3) The data order (MSB, LSB) of the Serial Interface

The data order of the Serial Interface is selected select either MSB or LSB first by the mask option.

4) Dividing ration of the internal clock

Each dividing ration of the count clocks of Timer, the Internal shift clock of the Serial Interface and the output clock through the SCK/CKOUT terminal is selected among the following by the mask option.
The frequency of each clock is determined by the dividing ration and the 1-instruction term ($1/f_{OSC}$x6).

1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512, 1/1024, 1/2048, 1/4096

Note) As the shift clock of the serial interface, the external clock or the internal is selected by the program.