# 8-BIT SERIAL TO PARALLEL CONVERTER

## ■ GENERAL DESCRIPTION

The NJU3712 is an 8-bit serial to parallel converter especially apply to MPU outport expander.

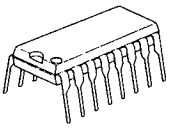
The effective outport assignment of MPU is available as the connection between NJU3712 and MPU is required only 4 lines.

Up to 5MHz signal can be input to the serial data input terminal and the data is output from parallel output buffer through serial in parallel out shift register and parallel data latches.

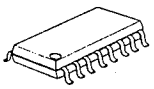
Furthermore, the NJU3712 output the serial data from SO terminal through the shift register, therefore output bit number can increase by cascade connection.

The hysteresis input circuit realized wide noise margin and high driverbility output buffer ( 25mA ) can drive LED directly.

## ■ PACKAGE OUTLINE



NJU3712D



NJU3712M

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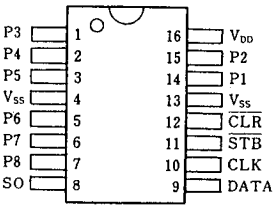
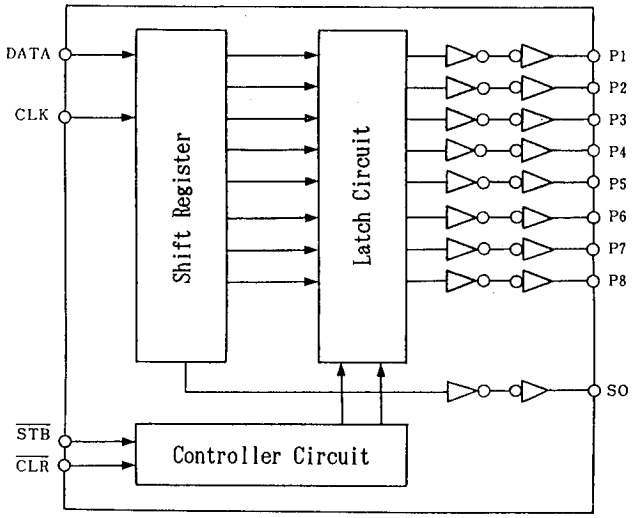
## ■ FEATURES

- 8-Bit Serial In Parallel Out
- Cascade Connection
- Hysteresis Input ---- 0.5V typ
- Operating Voltage ---- 5V±10%
- Operating Frequency ---- 5MHz or more
- Output Current ---- 25mA
- C-MOS Technology
- Package Outline ---- DIP/DMP 16

## ■ PIN CONFIGURATION




## ■ BLOCK DIAGRAM



## ■ TERMINAL DESCRIPTION

| NO. | SYMBOL | FUNCTION | NO. | SYMBOL | FUNCTION |
|---|---|---|---|---|---|
| 1 | P3 | Parallel Converts Data Output Terminals | 9 | DATA | Serial Data Input Terminal |
| 2 | P4 | | 10 | CLK | Clock Signal Input Terminal |
| 3 | P5 | | 11 | $\overline{STB}$ | Strove Signal Input Terminal |
| 4 | $V_{SS}$ | GND | 12 | $\overline{CLR}$ | Clear Signal Input Terminal |
| 5 | P6 | Parallel Converts Data Output Terminals | 13 | $V_{SS}$ | GND |
| 6 | P7 | | 14 | P1 | Parallel Converts Data Output Terminals |
| 7 | P8 | | 15 | P2 | |
| 8 | SO | Serial Data Output Terminal | 16 | $V_{DD}$ | Power Supply Terminal |

## ■ FUNCTIONAL DESCRIPTION

(1) **Reset**

When the "L" level is input to the $\overline{CLR}$ terminal, all latches are reset and all parallel conversion output are "L" level.

Normally, the $\overline{CLR}$ terminal should be "H" level.

(2) **Data Transmission**

In the $\overline{STB}$ terminal is "H" level and input the clock signal to the CLK terminal, the serial data input from DATA terminal shift in the shift register by synclonizing at rising edge of the clock signal.

When the $\overline{STB}$ terminal change to "L" level, the data in the shift register transfer to the latch.

Even if the $\overline{STB}$ terminal is "L" level, the input clock signal shift the data in the shift register, therefore, the clock signal control is needed.

(3) **Cascade Connection**

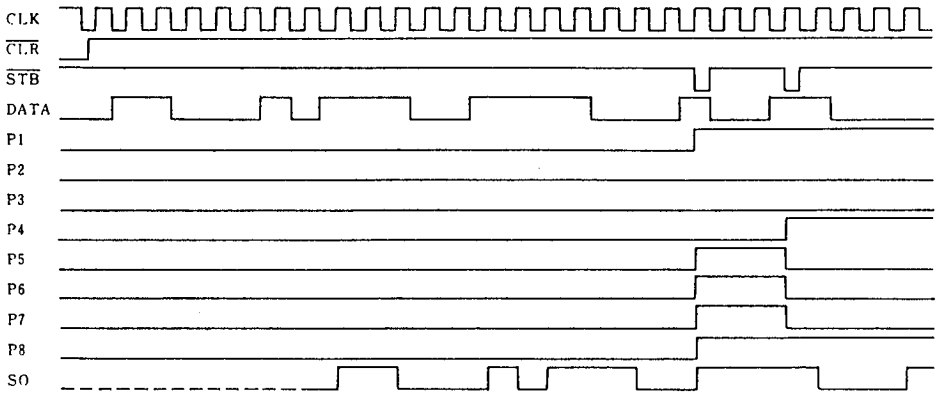
The serial data input from DATA terminal output from the SO terminal through internal shift register unrelated the $\overline{CLR}$ and $\overline{STB}$ status.

Furthermore, the 4 input terminals have a hysteresis characteristics by using the schmitt trigger structure to protect the noise.

| CLK | $\overline{STB}$ | $\overline{CLR}$ | OPERATION |
|---|---|---|---|
| X | X | L | All latch are reset (the data in the shift register is no change). All of Parallel convert output are "L". |
| ↑ | H | H | The serial data input from DATA terminal input to the shift register. In this stage, the data in the latch is no change. |
| L | L | H | The data in the shift register transfer to the latch. And the data in the latch output from parallel output. |
| H | | | |
| ↑ | | | The CLK input in the $\overline{STB}$="L" and $\overline{CLR}$="H" state, the data shift in the shift register and latched data also change in accordance with the shift register. |

Note ) X: Don't care

## ■ TIMING CHART

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## ■ ABSOLUTE MAXIMUM RATINGS

( Ta=25°C )

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Supply Voltage Range | $V_{DD}$ | − 0.5 ～ + 7.0 | V |
| Input Voltage Range | $V_I$ | $V_{SS}$−0.5 ～ $V_{DD}$+0.5 | V |
| Output Voltage Range | $V_O$ | $V_{SS}$−0.5 ～ $V_{DD}$+0.5 | V |
| Output Current | $I_O$ | ±25 | mA |
| Power Dissipation | $P_D$ | 700 (DIP)<br>300 (DMP) | mW |
| Operating Temperature Range | Topr | −25 ～ +85 | °C |
| Storage Temperature Range | Tstg | −65 ～ +150 | °C |

## ■ DC ELECTRICAL CHARACTERISTICS

($V_{DD}$=4.5～5.5V, $V_{SS}$=0V, Ta=25℃)

| PARAMETER | | SYMBOL | CONDITION | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| Operating Current | | $I_{DDS}$ | $V_{IH}$=$V_{DD}$, $V_{IL}$=$V_{SS}$ | | | | 0.1 | mA |
| Output Voltage | High-Level | $V_{OH}$ | $I_{OH}$=-0.4mA | SO Terminal | 4.0 | | $V_{DD}$ | V |
| | Low-Level | $V_{OL}$ | $I_{OL}$=+3.2mA | | $V_{SS}$ | | 0.4 | |
| Input Voltage | High-Level | $V_{IH}$ | | | 0.7$V_{DD}$ | | $V_{DD}$ | V |
| | Low-Level | $V_{IL}$ | | | $V_{SS}$ | | 0.3$V_{DD}$ | |
| Input Leakage Current | | $I_{LI}$ | $V_I$=0～$V_{DD}$ | | -10 | | 10 | μA |
| High-Level Output Voltage | | $V_{OHD}$ | $I_{OH}$=-25mA | P1～P8 Terminals (Note 1) | $V_{DD}$-1.5 | | $V_{DD}$ | V |
| | | | $I_{OH}$=-15mA | | $V_{DD}$-1.0 | | $V_{DD}$ | |
| | | | $I_{OH}$=-10mA | | $V_{DD}$-0.5 | | $V_{DD}$ | |
| Low-Level Output Voltage | | $V_{OLD}$ | $I_{OL}$=+25mA | | $V_{SS}$ | | 1.5 | V |
| | | | $I_{OL}$=+15mA | | $V_{SS}$ | | 0.8 | |
| | | | $I_{OL}$=+10mA | | $V_{SS}$ | | 0.4 | |
| Output Short Current | | $I_{OS}$ | $V_O$=7V, $V_I$=0V | SO Terminal (Note 2) | | | 10 | mA |
| | | | $V_O$=0V, $V_I$=7V | | | | -10 | |
| | | $I_{OSD}$ | $V_O$=7V, $V_I$=0V | P1～P8 Terminals (Note 2) | | | 20 | mA |
| | | | $V_O$=0V, $V_I$=7V | | | | -20 | |

Note 1) Specified value represent output current per pin. When use, total current consideration and less than power dissipation rating operation should be required.
Note 2) $V_{DD}$=7V, $V_{SS}$=0V, 1 second per pin.

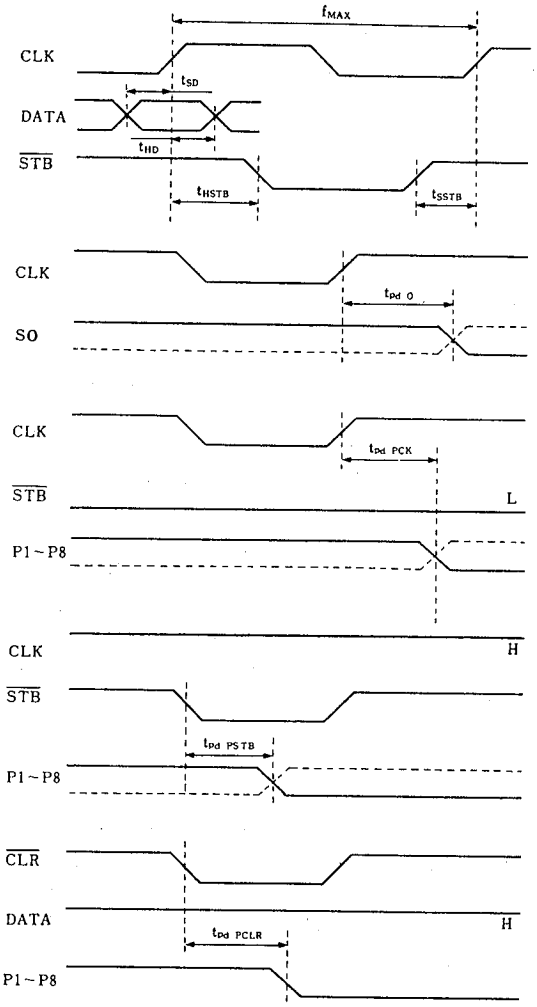
## ■ SWITCHING CHARACTERISTICS

($V_{DD}$=4.5V～5.5V, $V_{SS}$=0V, Ta=-20～75℃)

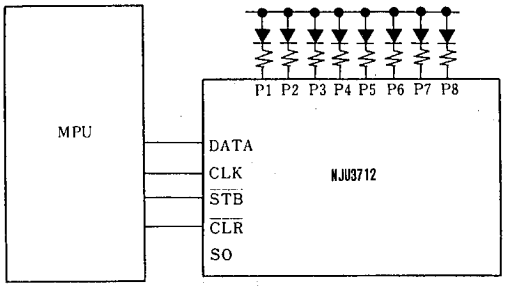
| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Set-Up Time | $t_{SD}$ | DATA - CLK | 20 | | | ns |
| Hold Time | $t_{HD}$ | CLK - DATA | 20 | | | ns |
| Set-Up Time | $t_{SSTB}$ | $\overline{STB}$ - CLK | 30 | | | ns |
| Hold Time | $t_{HSTB}$ | CLK - $\overline{STB}$ | 30 | | | ns |
| Output Delay Time | $t_{pd\ O}$ | CLK - SO | | | 70 | ns |
| | $t_{pd\ PCK}$ | CLK - P1～P8 | | | 100 | ns |
| | $t_{pd\ PSTB}$ | $\overline{STB}$ - P1～P8 | | | 80 | ns |
| | $t_{pd\ PCLR}$ | $\overline{CLR}$ - P1～P8 | | | 80 | ns |
| Max. Operating Frequency | $f_{MAX}$ | | 5 | | | MHz |

＊) $C_{OUT}$=50pF

## ■ SWITCHING CHARACTERISTICS TEST WAVEFORM



■ APPLICATION CIRCUIT (1)

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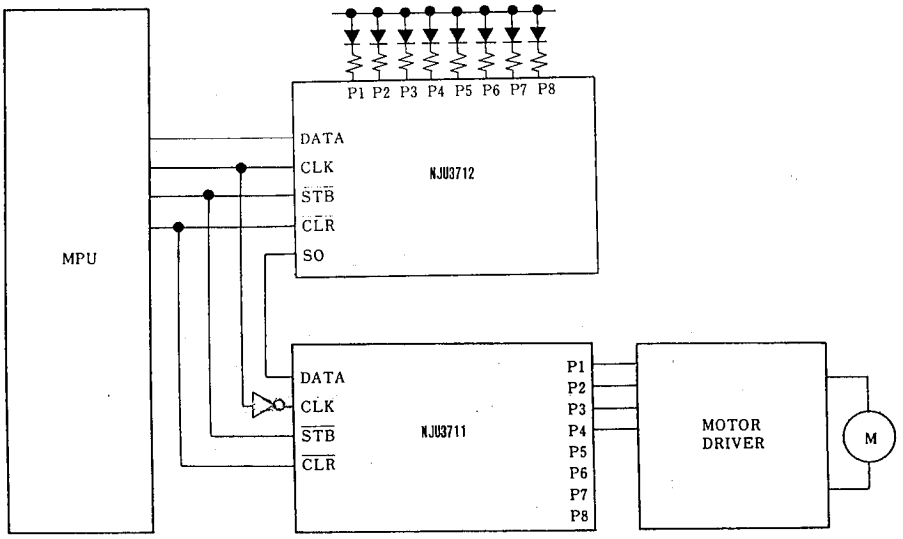
■ APPLICATION CIRCUIT (2) (Combined with NJU3711)



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