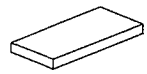
PRELIMINARY

34COMMON X 101SEGMENT
I²C-BUS BIT MAP LCD DRIVER

■ GENERAL DESCRIPTION

NJU6576 is a bit map LCD driver to display graphics or characters. It contains 3,434-bit display data RAM, microprocessor interface circuits, instruction decoder, 101-segment and 34-common drivers.
NJU6576 is supported by the first-mode I²C-Bus, and the bit image display data are transferred to the display data RAM through SDA line.
NJU6576 possesses two display modes selected by a command. It displays 33-common/101-segment graphics in the normal display mode. And it displays 101 Static-icons, keeping low power consumption, in the icon mode.
NJU6576 includes internal oscillator and realizes low operating current, wide operating voltage from 2.2V to 5.5V. Therefore it is useful for small size battery items.

■ PACKAGE OUTLINE



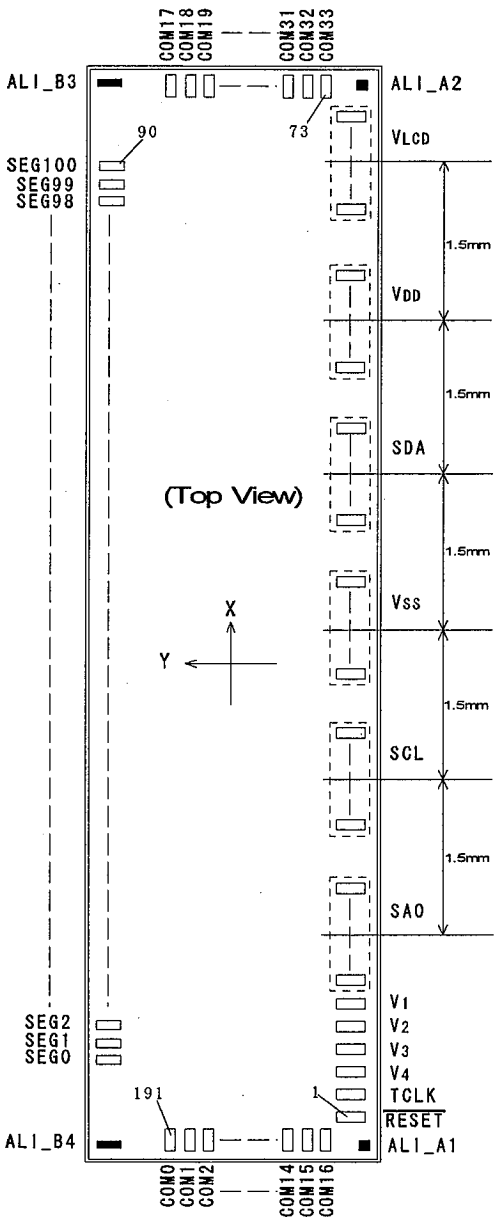
NJU6576CH

■ FEATURES

● Display Data RAM	3,434-bit	
●LCD Driving outputs	34-common X 101-segment	(in normal display mode: Bit Map Display)
	1-common X 101-segment	(in icon mode: Static-icon Display)
●Direct Interface to the first-mode I²C-bus		
●Programmable Display mode	Normal display mode, Icon mode	
●Programmable Duty Ratio	1/34, 1/17 duty	(in normal display mode)
●Programmable Bias Ratio	1/7, 1/5 bias	(in normal display mode)
● Command List		
Display On/Off, Power Save On/Off, Icon-mode On/Off, Duty Select, Bias Select, Increment Mode Select		
Page Address Set, Column Address Set		
●LCD Power Supply Circuit	Bleeder resistor X 5, Voltage follower X 4	(in normal display mode)
●Low Operating Current	*** uA TYP.	
●Operating Voltage(V_{DD})	2.2V to 5.5V	
●LCD Driving Voltage(V_{LCD})	4V to 13.5V	(in normal display mode)
	2.5V to 13.5V	(in icon mode)
● Package Outline	TCP/Bumped Chip	
●C-MOS Technology		

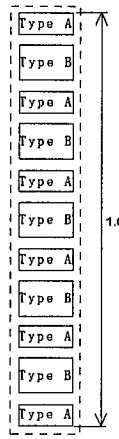
* Purchase of I²C components of New Japan Radio Co., Ltd or one of its sublicensed Associated Companies conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

■ PAD LOCATION



- MPU I/F PAD FORM -

SA0,SCL,Vss
SDA,VDD,VLCD



Type A

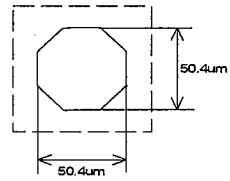
PAD size :50X100um
(Bump size :63X113um)

Type B

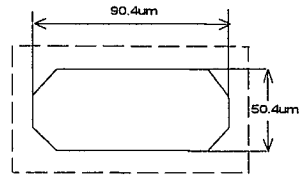
PAD size :80X100um
(Bump size :93X113um)

- Alignment Mark -

ALI_A1, A2(Alignment mark)



ALI_B3, B4(Alignment mark)



Chip Center	X=0mm, Y=0mm
Chip Size	X=9.58mm, Y=2.3mm
Chip Thickness	400um ±30um
PAD(Bump) Size	No.1 to No.6, No.73 to No.207
	PAD size :50umX100um
	(Bump size :63um X 113um)
PAD Pitch	80um MIN.
Bump Height	25um TYP.
Bump Material	Au

■ : Alignment mark for COG assembling.

■ PAD COORDINATES

Chip size 9.58mm X 2.3mm (Chip center X= 0,Y=0)

PAD No.	PAD Name	X=(um)	Y=(um)
1	$\overline{\text{RESET}}$	-4374	-999
2	TCLK	-4294	-999
3	V4	-4214	-999
4	V3	-4134	-999
5	V2	-4054	-999
6	V1	-3974	-999
7	SA0	-3893	-999
8	SA0	-3798	-999
9	SA0	-3703	-999
10	SA0	-3608	-999
11	SA0	-3513	-999
12	SA0	-3418	-999
13	SA0	-3323	-999
14	SA0	-3228	-999
15	SA0	-3133	-999
16	SA0	-3038	-999
17	SA0	-2943	-999
18	SCL	-2393	-999
19	SCL	-2298	-999
20	SCL	-2203	-999
21	SCL	-2108	-999
22	SCL	-2013	-999
23	SCL	-1918	-999
24	SCL	-1823	-999
25	SCL	-1728	-999
26	SCL	-1633	-999
27	SCL	-1538	-999
28	SCL	-1443	-999
29	VSS	-893	-999
30	VSS	-798	-999
31	VSS	-703	-999
32	VSS	-608	-999
33	VSS	-513	-999
34	VSS	-418	-999
35	VSS	-323	-999
36	VSS	-228	-999
37	VSS	-133	-999
38	VSS	-38	-999
39	VSS	57	-999
40	SDA	607	-999
41	SDA	702	-999
42	SDA	797	-999
43	SDA	892	-999
44	SDA	987	-999
45	SDA	1082	-999
46	SDA	1177	-999
47	SDA	1272	-999
48	SDA	1367	-999
49	SDA	1462	-999
50	SDA	1557	-999

PAD No.	Pad Name	X=(um)	Y=(um)
51	VDD	2107	-999
52	VDD	2202	-999
53	VDD	2297	-999
54	VDD	2392	-999
55	VDD	2487	-999
56	VDD	2582	-999
57	VDD	2677	-999
58	VDD	2772	-999
59	VDD	2867	-999
60	VDD	2962	-999
61	VDD	3057	-999
62	VLCD	3607	-999
63	VLCD	3702	-999
64	VLCD	3797	-999
65	VLCD	3892	-999
66	VLCD	3987	-999
67	VLCD	4082	-999
68	VLCD	4177	-999
69	VLCD	4272	-999
70	VLCD	4367	-999
71	VLCD	4452	-999
72	VLCD	4557	-999
73	COM33	4638	-705
74	COM32	4638	-625
75	COM31	4638	-545
76	COM30	4638	-465
77	COM29	4638	-385
78	COM28	4638	-305
79	COM27	4638	-225
80	COM26	4638	-145
81	COM25	4638	-65
82	COM24	4638	15
83	COM23	4638	95
84	COM22	4638	175
85	COM21	4638	255
86	COM20	4638	335
87	COM19	4638	415
88	COM18	4638	495
89	COM17	4638	575
90	SEG100	4026	998
91	SEG99	3946	998
92	SEG98	3866	998
93	SEG97	3786	998
94	SEG96	3706	998
95	SEG95	3626	998
96	SEG94	3546	998
97	SEG93	3466	998
98	SEG92	3386	998
99	SEG91	3306	998
100	SEG90	3226	998

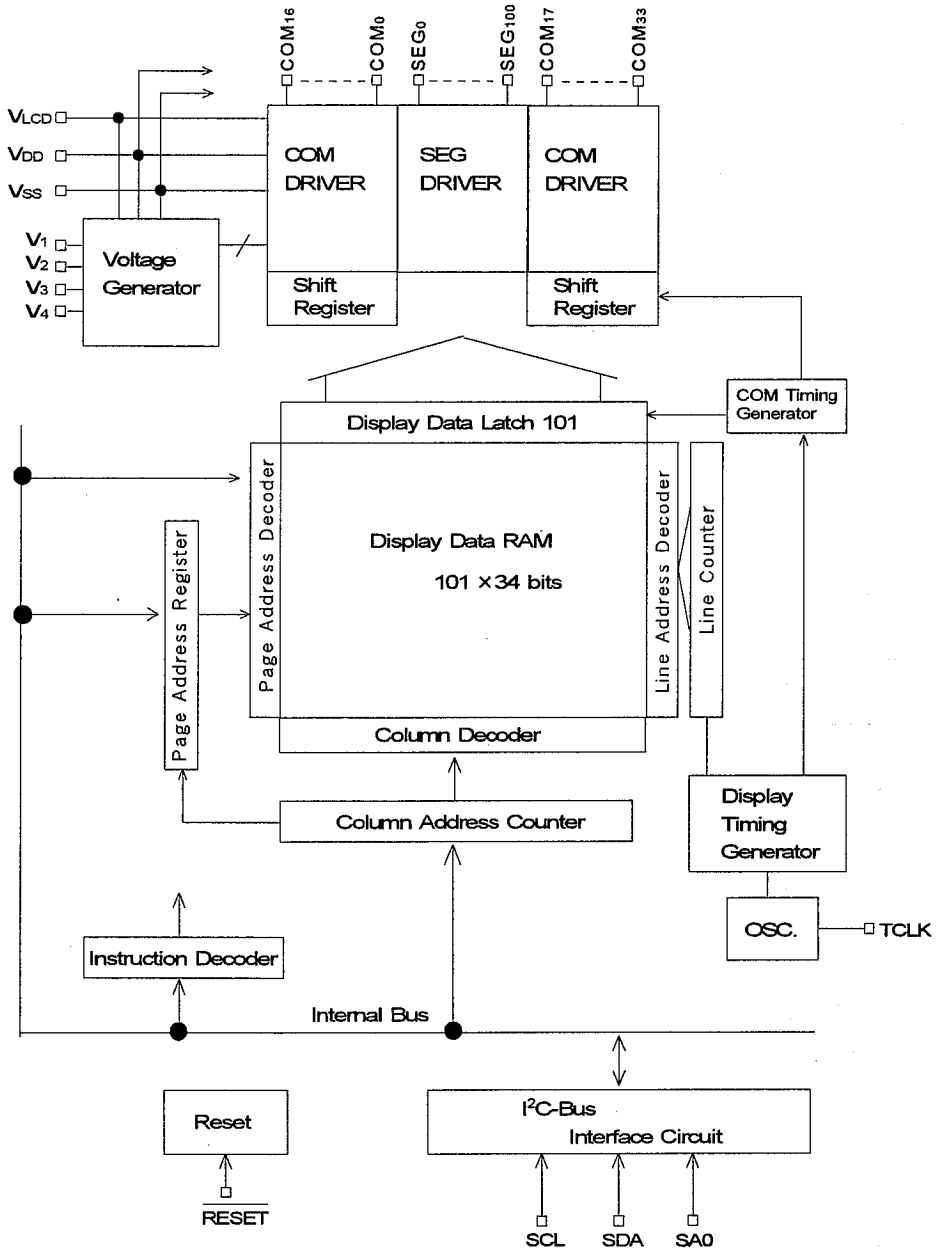
PAD No.	PAD Name	X=(um)	Y=(um)
101	SEG89	3146	998
102	SEG88	3066	998
103	SEG87	2986	998
104	SEG86	2906	998
105	SEG85	2826	998
106	SEG84	2746	998
107	SEG83	2666	998
108	SEG82	2586	998
109	SEG81	2506	998
110	SEG80	2426	998
111	SEG79	2346	998
112	SEG78	2266	998
113	SEG77	2186	998
114	SEG76	2106	998
115	SEG75	2026	998
116	SEG74	1946	998
117	SEG73	1866	998
118	SEG72	1786	998
119	SEG71	1706	998
120	SEG70	1626	998
121	SEG69	1546	998
122	SEG68	1466	998
123	SEG67	1386	998
124	SEG66	1306	998
125	SEG65	1226	998
126	SEG64	1146	998
127	SEG63	1066	998
128	SEG62	986	998
129	SEG61	906	998
130	SEG60	826	998
131	SEG59	746	998
132	SEG58	666	998
133	SEG57	586	998
134	SEG56	506	998
135	SEG55	426	998
136	SEG54	346	998
137	SEG53	266	998
138	SEG52	186	998
139	SEG51	106	998
140	SEG50	26	998
141	SEG49	-54	998
142	SEG48	-134	998
143	SEG47	-214	998
144	SEG46	-294	998
145	SEG45	-374	998
146	SEG44	-454	998
147	SEG43	-534	998
148	SEG42	-614	998
149	SEG41	-694	998
150	SEG40	-774	998

PAD No.	PAD Name	X=(um)	Y=(um)
151	SEG39	-854	998
152	SEG38	-934	998
153	SEG37	-1014	998
154	SEG36	-1094	998
155	SEG35	-1174	998
156	SEG34	-1254	998
157	SEG33	-1334	998
158	SEG32	-1414	998
159	SEG31	-1494	998
160	SEG30	-1574	998
161	SEG29	-1654	998
162	SEG28	-1734	998
163	SEG27	-1814	998
164	SEG26	-1894	998
165	SEG25	-1974	998
166	SEG24	-2054	998
167	SEG23	-2134	998
168	SEG22	-2214	998
169	SEG21	-2294	998
170	SEG20	-2374	998
171	SEG19	-2454	998
172	SEG18	-2534	998
173	SEG17	-2614	998
174	SEG16	-2694	998
175	SEG15	-2774	998
176	SEG14	-2854	998
177	SEG13	-2934	998
178	SEG12	-3014	998
179	SEG11	-3094	998
180	SEG10	-3174	998
181	SEG9	-3254	998
182	SEG8	-3334	998
183	SEG7	-3414	998
184	SEG6	-3494	998
185	SEG5	-3574	998
186	SEG4	-3654	998
187	SEG3	-3734	998
188	SEG2	-3814	998
189	SEG1	-3894	998
190	SEG0	-3974	998
191	COM0	-4639	572
192	COM1	-4639	492
193	COM2	-4639	412
194	COM3	-4639	332
195	COM4	-4639	252
196	COM5	-4639	172
197	COM6	-4639	92
198	COM7	-4639	12
199	COM8	-4639	-68
200	COM9	-4639	-148

PAD No.	PAD Name	X=(um)	Y=(um)
201	COM10	-4639	-228
202	COM11	-4639	-308
203	COM12	-4639	-388
204	COM13	-4639	-468
205	COM14	-4639	-548
206	COM15	-4639	-628

PAD No.	PAD Name	X=(um)	Y=(um)
207	COM16	-4639	-708
ALIGNMENT	ALI_A1	-4663	-1023
ALIGNMENT	ALI_A2	4662	-1023
ALIGNMENT	ALI_B3	4662	1002
ALIGNMENT	ALI_B4	-4663	1002

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

PAD No.	Symbol	I/O	Function
51 to 61	V_{DD}	POWER	Power supply
29 to 39	V_{SS}	POWER	GND
62 to 72	V_{LCD}	POWER	LCD driving voltage supply(V_{LCD})
6	V_1	POWER	LCD driving voltage supply(V_1 to V_4) In order to realize high quality display, the capacitors between V_1, V_2, V_3, V_4 and Vss are recommended. But if these capasitors are not needed, V_1, V_2, V_3, V_4 terminals should be open.
5	V_2		
4	V_3		
3	V_4		
1	$\overline{RESET}$	I	Reset When the reset signal "L" is input into this terminal, the reset operation is performed. In case this terminal is not used, it should be open or connected to V_{DD}.
18 to 28	SCL	I	Serial clock input
40 to 50	SDA	I/O	Serial data input
7 to 17	SA0	I	External input address SA0 terminal defines the slave address bit0 of NJU6576. Fix SA0 terminal to V_{DD} or Vss.
73 to 89, 191 to 207	COM_0 to COM_{33}	O	LCD driving outputs - Common outputs COM_0 to COM_{33} (Normal Display Mode: 1/34Duty) COM_0 to COM_{15}, COM_{33}(Normal Display Mode: 1/17Duty) COM_{33} (Icon Mode : 1/1Duty) - Segmnet outputs SEG_0 to SEG_{100} (Normal Display/Icon Mode)
90 to 190	SEG_0 to SEG_{100}		
2	TCLK	-	Test terminal. Normaly open.

■ Functional Description

(1-1) Line Counter

The Line Counter generates the line address of display data RAM by the count up operation synchronizing the common cycle after the reset operation at the status change of internal FR signal.

(1-2) Column Address Counter/ Page Address Register

The column address counter is a pre-settable counter addressing the of display data RAM as shown in Fig. 2. The page register gives a page address of the display data RAM. "Increment mode select" command sets "column increment mode" or "page increment mode".

In the "column increment mode", the column address is auto-incremented (+1) whenever the display data byte is transferred, as shown in Fig.1-1. After the display data byte is written in the last column(64)H, the column address returns to(00)H and the page address is auto-incremented(+1).

In the "page increment mode", the page address is auto-incremented (+1) whenever the display data byte is transferred, as shown in Fig.1-2. After the display data byte is written in the page(4)H, the page address returns to page(0)H and the column address is auto-incremented(+1).

In both case of "column increment mode" and "page address mode", after the display data byte is written in the page (4)H and column(64)H, these addresses returns to the page(0)H and column (00)H.

The "page address set" and "column address set" command are required, when access by changing the page address and column address.

D7--D0 of page(2)H and page(3), and D0 of page(4) can not be accessed by MPU in 1/17Duty.

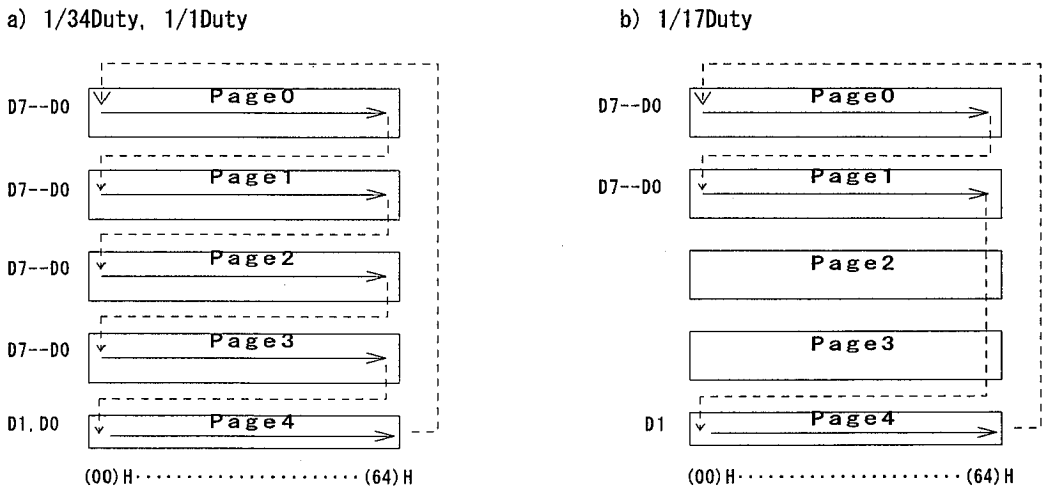
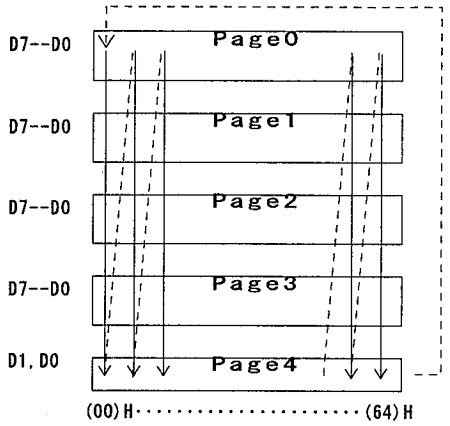


Fig.1-1 Auto-increment direction, in column increment mode.

a) 1/34Duty, 1/1Duty



b) 1/17duty

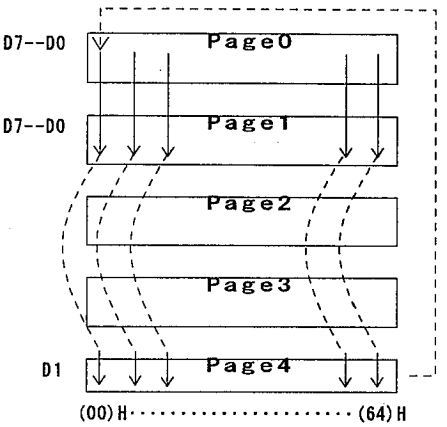


Fig.1-2 Auto-increment direction, in page increment mode.

(1-3)Display Data RAM

Display Data RAM is the bit map RAM consisting of 3,434 bits to memorize the display data corresponding to each pixel of LCD panel. The each bit in the Display Data RAM corresponds to the each pixel of the LCD panel and controls the display by following bit data.

When Normal Display : On="1" , Off="0"

When Inverse Display : On="0" , Off="1"

The Display Data RAM outputs 101-bit parallel data in the area addressed by the line counter, and these data are set into the Display Data Latch.

The access operation from MPU to the display data RAM and the data output from the display data RAM are so controlled to operate independently that the data rewriting does not influence with any malfunctions to the display.

The relation between column address and segment output terminals is shown in Fig. 2.

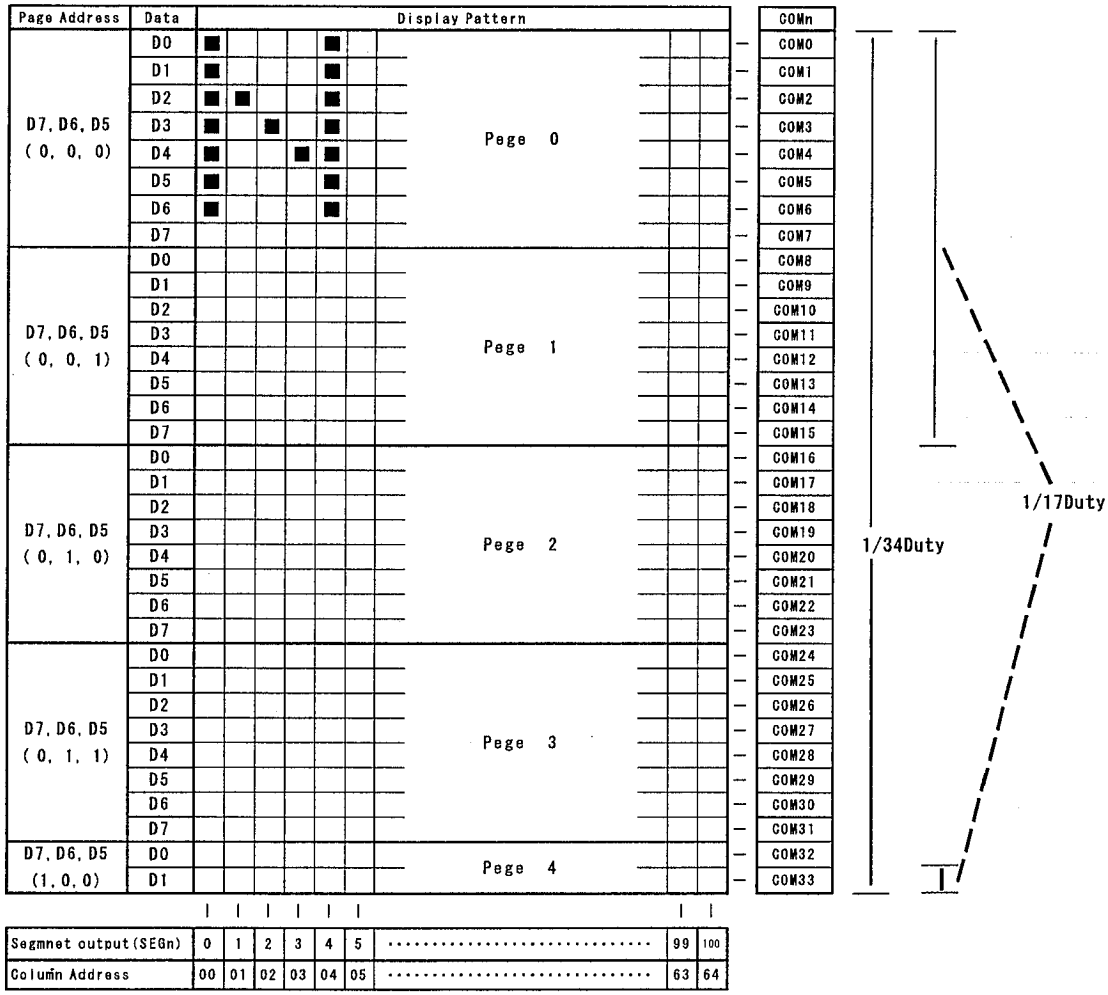


Fig.2 Correspondence with Display data RAM and address

Note1) Correspondence with Duty and COM terminals

COM0 - COM33	(Normal Display Mode	: 1/34Duty)	
COM0 - COM15, COM33	(Normal Display Mode	: 1/17Duty)	*1) D7--D0 of page(2)H, D7--D0 of page(3)H and D0 of page(4)H can not be accessed from MPU in 1/17Duty.
COM33	(Icon Mode	: 1/1Duty)	

(1-4)Reset Circuit

NJU6576 automatically executes the reset operation by the power on reset circuit when the external power supply is turned on. To work the power on reset circuit correctly, The "power supply condition" mentioned in the reset circuit characteristics should be kept.

To use the hardware reset operation after the external power supply is turned on, input the reset signal, which is "L" over than 10us, into the $\overline{\text{RESET}}$ terminal. And then the normal operation starts after 1us from the rise edge of reset signal.

Initialization (Default setting)

-Display off
-Power save on
-Icon mode off (Normal display mode)
-Duty select :1/34Duty
-Bias select :1/7Bias

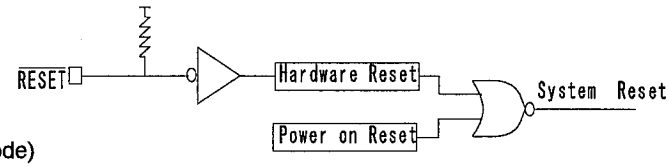


Fig.3 Reset circuit

Note2) If "power supply condition" mentioned in the reset characteristics can not be followed.....
If "power supply condition" is not followed, the above-mentioned initialization functions might not be expected. For example, if "display on" and "power save off" are set by mistake, because of unstable COM/SEG waveform output just after V_{LCD} on, LCD display might be turned on for an instant. To avoid this phenomenon, set "display off" and "power save on" command before V_{LCD} on.

(1-5) LCD Driving

(a)Oscillation Circuit

The Oscillation Circuit is a low power CR oscillator incorporating with Resistor and Capacitor. It generates clocks for display timing signal source.

(b) LCD Driving Circuits

LCD driving circuits are consisted of 135 multiplexers which operate as 101-segment drivers and 34-common drivers. 34-common drivers with the shift register scan the common display signal. The combination of the Display data, COM scan signal and FR signal forms the LCD driving output voltage. The output wave form are shown in Fig.6 - Fig.9.

(c) Display Data Latch Circuits

Display Data Latch stores 101-bit display data temporarily which is output to LCD driver circuits at a common cycle from the Display Data RAM addressed by Line Counter. The instructions of Display On/Off controls only the data in Display Data Latch, therefore, the data in the Display Data RAM is not changed.

(d) Line Counter and Latch signal of Latch Circuits

The clock to Line Counter and latch signal to the Latch Circuits are generated from the internal display clock(CL). The line address of Display Data RAM is renewed synchronizing with display clock(CL). 101-bit display data are latched in display latch circuits synchronizing with display clock, and then output to the LCD driving circuits. The display data transfer to the LCD driving circuits is executed independently with RAM access by the MPU.

(e) Display Timing Generator

Display Timing Generator generates the timing signal for the display system by combination of the master clock CL and Driving Signal FR (Refer to Fig.4). The Frame Signal FR and LCD alternative signal generate LCD driving waveform of the two frame alternative driving method.

(f) Common Timing Generation

The common timing is generated by display clock CL. Refer to Fig.4.

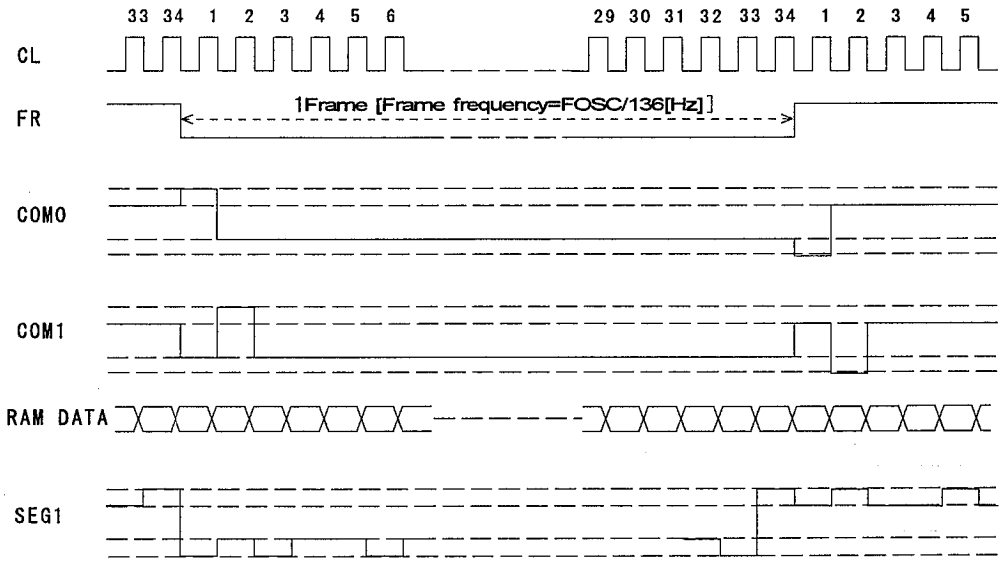


Fig.4 Display Timing in 1/34Duty

(g)Power Supply Circuit

The internal Power Supply Circuit generates the bias voltage for the LCD driving waves. This circuit condition are changed by the NJU6576 state, such as the power save mode, normal display mode and icon mode, as shown in Table.1 and Fig.5.

This circuit is designed for small size LCD, not for large size LCD. In case of large size LCD, capacitors between V_1, V_2, V_3, V_4 and V_{SS} should be connected in order to high quality display.

Table.1

	Power supply circuit condition
Power save	All components stop
Normal mode	1/7(1/5) Bias
Icon mode	1/2 Bias

*1)
NJU6576 state, such as the power save mode, normal display mode and icon mode, is selected by the command.

*2)
Input each suitable V_{LCD} voltage for the normal mode, for the icon mode. The following conditions should be maintained in each case.

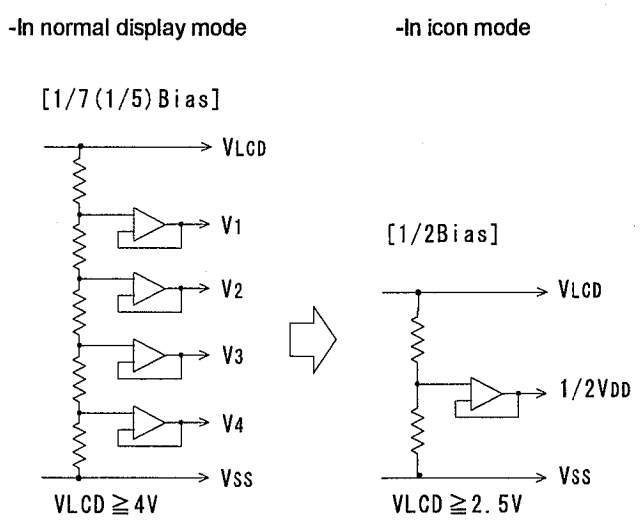


Fig.5 Power Supply Circuit

■Transferring data on the I²C-Bus

1)Transferring data format

NJU6576 transferring data can be supported by the first mode I²C-Bus. The serial data are transferred through SDA line and the serial clock is input through SCL line.

As the first byte, transfer the slave address of NJU6576 and the data direction . NJU6576 is only for slave LSI, and the data D0 in the first byte (at 8th bit timing) should be "0". As the second byte, transfer the command1 mentioned in (3-1) , as the third byte, transfer the command2 in (3-2). After the fourth byte, transfer the display data.

NJU6576 outputs the acknowledge bit (A="0") after each byte, at 9th bit timing.

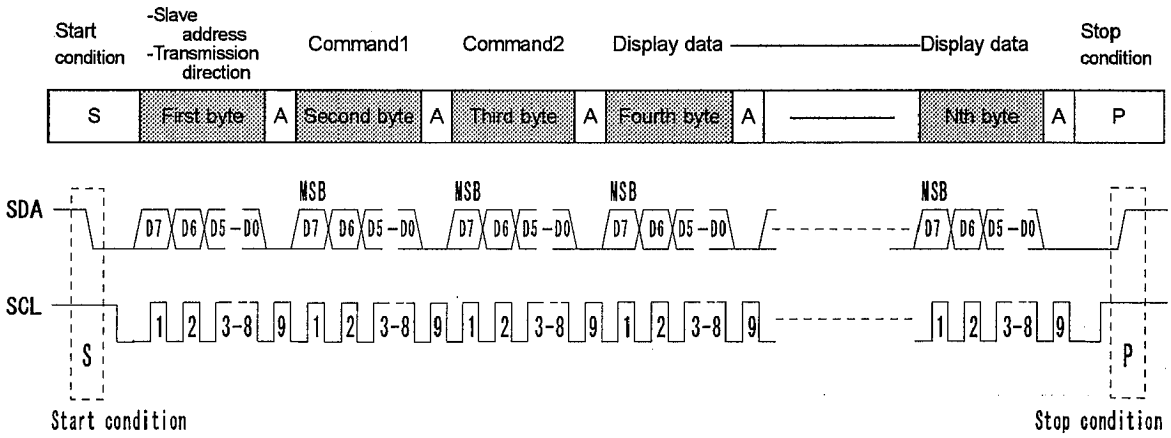


Fig.6 NJU6576 I2C-Bus Transferring Data Format

1-1)S:START condition

A rise edge of the SDA terminal while the SCL terminal is "H", which situation defines the START condition. After the START, NJU6576 starts reading the first byte.

1-2)P:STOP condition

A fall edge of the SDA terminal while the SCL terminal is "H" , which situation defines the STOP condition.

NJU6576 can read plural bytes continually until the STOP. After the STOP, it finishes reading data and holds previous state until the next START.

1-3)A:Acknowledge bit (A="0")

When NJU6576 acknowledges a coincidence its own address with the address information in the first byte, it outputs the Acknowledge just after the first byte(at 9th bit timing) through the SDA terminal.

After the second byte, whenever NJU6576 reads data correctly, it outputs the acknowledge at each 9th bit timing.

1-4)Definitions of each byte

- First byte :Slave address, Data direction
- Second byte :Command1
- Third byte :Command2
- Fourth byte :Display data
- ---------- ----------
- ---------- ----------
- Nth byte :Display data

2)Definition of the first byte :Slave address, Data direction

As the first byte, transfer the NJU6576 slave address and the data direction

The NJU6576 slave address is (D7--D1)=(0, 1, 1, 1, 0, 0, SA0). In this address, the data "D1(SA0)" is corresponded to the SA0 terminal state. NJU6576 is only for slave LSI, and the data D0(at 8th bit timing) in the first byte should be "0". If the data D0="1", NJU6576 does not output the acknowledge.

NJU6576 is not supported by the general call address. Therefore, if the data (D7--D1)=(0, 0, 0, 0, 0, 0, 0), NJU6576 does not output the acknowledge.

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	0	SA0	0
←	Slave address					→	R/W

- D7-D2 : 0,1,1,1,0,0
- D1 : SA0 (External input address)
- D0 : 0

3)Explanation of Command1,2

3-1)Definition of the second byte :Command1

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

- D7-D5 : Page address set
- D4 : Bias select
- D3 : Duty select
- D2 : Icon mode ON/OFF
- D1 : Power save ON/OFF
- D0 : Display ON/OFF

Note1)
The combination of the data, D3, D2 and D1, decides the display state and COM terminal condition. Refer to Table.2.

D0: Display ON/OFF

This command executes whole display ON/OFF, without relationship of the data in the Display Data RAM and internal condition.

D0=1:Display ON
D0=0:Display OFF

The internal state of LSI in the display off is as follows;

- The oscillation circuit and internal power supply circuit are working.
- All COM/SEG terminals are fixed to Vss level.
- The display data and operation mode are kept as before the display off.
- The display data RAM can be accessed by MPU.

D1: Power save ON/OFF

In the power save mode, the operating current can be reduced as same as the standby current.

D1=1:Power save ON
D1=0:Power save OFF

The internal state of LSI in the power save mode is as follows;

- The oscillation circuit and internal power supply circuit stop.
- All COM/SEG terminals are fixed to Vss level.
- The display data and operation mode are kept as before the power save.
- The display data RAM can be accessed by MPU.

D2: Icon mode ON/OFF

This command selects the normal display mode(bit map display) or icon mode.
In the icon mode, NJU6576 can display 101 max. static-icons.

D2=1: Icon mode (Icon mode ON)
D2=0: Normal display mode (Icon mode OFF)

In the icon mode, the internal condition of LSI is as follows;

- All SEG and icon COM terminals are valid.
- Except the icon COM terminal, the other COM terminals output 1/2 V_{LCD} level.
- The display data and operation mode are kept as before the power save.
- The display data RAM can be accessed from MPU.

Note2)
To access the DDRAM efficiently during the icon mode, set "page address(4)H" by command1, "column increment mode" and "column address" by command2.

D3: Duty select

This command sets the duty ratio in the normal display mode, and in the icon mode.

D3=1	:Normal display mode	1/34 duty	(COM_0--COM_{33})
	:Icon mode	1/1 duty	(COM_{33})
D3=0	:Normal display mode	1/17 duty	(COM_0--COM_{15}, COM_{33})
	:Icon mode	1/1 duty	(COM_{33})

Note3)Refer to table.2.

D4: Bias select

This command sets the LCD bias ratio.

D4=1 :1/7 bias
D4=0 :1/5 bias

Note4)
In the normal display mode, this command is valid.
In the icon mode, the ratio is fixed to 1/2 bias and 1/1 Duty regardless of this command.

D7-D5: Page address set

This command sets page address.

D7,D6,D5 = 0,0,0 :Page address(0)H
D7,D6,D5 = 0,0,1 :Page address(1)H
D7,D6,D5 = 0,1,0 :Page address(2)H
D7,D6,D5 = 0,1,1 :Page address(3)H
D7,D6,D5 = 1,0,0 :Page address(4)H

(Note1, 3)

The combination of the data, D3, D2 and D1, decides the display state and output terminals condition as shown in Table.2.

-Table.2- Display state and output terminals condition.

Command1			Display state	COM/SEG terminals		Duty
"D3"	"D2"	"D1"				
Duty Select	Icon mode ON/OFF	Power Save ON/OFF				
*	*	1	Power save mode			
*	1	0	Icon mode	COM33 (*1)	SEG0 --- SEG100	1/1
1	0		Normal display mode	COM0 - COM33		1/34
0				COM0 - COM15,COM33		1/17

* : Don't care.

*1)Max.101 icons

*2)Input each suitable VLCD voltage for the normal mode, for the icon mode. The following conditions should be maintained in each case.

-In normal display mode :VLCD ≧ 4V

-In icon mode :VLCD ≧ 2.5V

*3)LCD driving waveform through the COM/SEG terminals are shown in Fig.12--Fig.14.

3-2)Definition of the third byte :command2

This byte sets the "increment mode select" and "column address" in the display data RAM.

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

-D7: Increment mode select

D7=1 :Page increment mode

D7=0 :Column increment mode

Note5) Refer to functional description (1-2)

-D6-D0: Column address

D6,D5,D4,D3,D2,D1,D0 =0,0,0,0,0,0,0	:Column address (00)H
D6,D5,D4,D3,D2,D1,D0 =0,0,0,0,0,0,1	:Column address (01)H
----------	----------
----------	----------
D6,D5,D4,D3,D2,D1,D0 =1,1,0,0,0,1,1	:Column address (63)H
D6,D5,D4,D3,D2,D1,D0 =1,1,0,0,1,0,0	:Column address (64)H

4)Definition of the fourth byte :Display data

After the fourth byte, transfer the display data byte.

The column and page address auto-increment by the Display Data transfers. Therefore, NJU6576 can read plural bytes continually without these "address set" commands, until the STOP condition.

The correspondence with display data RAM and addresses are shown in Fig.2.

■ Attention to "power supply on/off" and "power save off"

In case of connecting capacitors between V_1, V_2, V_3, V_4 and Vss, execute the following timing and wait-time at the power supply on/off and power save off. Unless these executions, LCD display might be turned on for an instant because of unstable COM/SEG waveform by charging(or discharging) these capacitors just after the power supply on/off and power save off. To avoid this phenomenon. these executions are required.
In case of large size LCD panel, in spite of not connecting these capacitors, same phenomenon might be happened. In this case, execute them at the power supply on/off and power save off.

1)At the power supply on/off

Execute Fig.7 or Fig.8 at power supply on, Fig.9 or Fig.10 at power supply off.

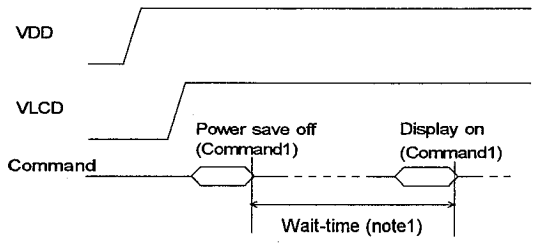


Fig.7 Power supply on timing and Wait-time Case1

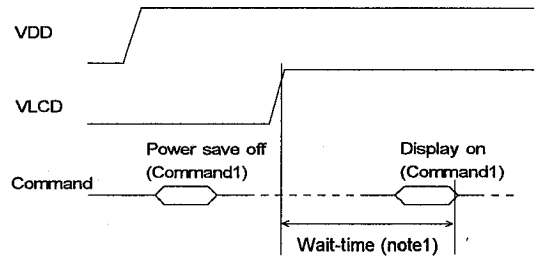


Fig.8 Power supply on timing and Wait-time Case2

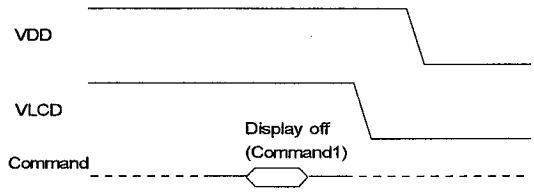


Fig.9 Power supply off timing Case1

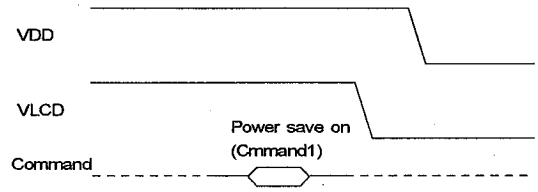


Fig.10 Power supply off timing Case2

Note1)
Wait-time is almost ***ms at capacitors C3=0.1uF, V_{DD}=3V, V_{LCD}=8V. Suitable wait-time depends on value of capacitor, V_{DD}, V_{LCD}. Therefore, practice a test with actual module.
Any commands except "display on" can be accepted during wait-time.

2)At the power save off

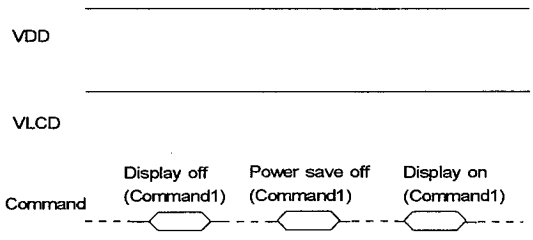


Fig.11 Power save off timing

■ ABSOLUTE MAXIMUM RATING

PARAMETER		SYMBOL	RATING	UNIT
Supply Voltage(1)		V_{DD}	−0.3 ~ +7.0	V
Supply Voltage(2)		V_{LCD}	−0.3 ~ +13.5	V
Input Voltage		V_{IN}	−0.3 ~ +7.0	V
Oparating Temperature		T_{OPR}	−30 ~ +80	℃
Storage Temperature	TCP	T_{STG}	−55 ~ +100	℃
	Chip		−55 ~ +125	℃

Note 1) All voltage values are specified as V_{SS} = 0 V.
Note 2) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.
Note 3) The relation : $V_{LCD} \geqq V_{SS}$ must be maintained.
Note 4) Decoupling capacitor should be connected between V_{DD} and V_{SS}, V_{LCD} and V_{SS} due to the stabilized operation for the voltage converter.

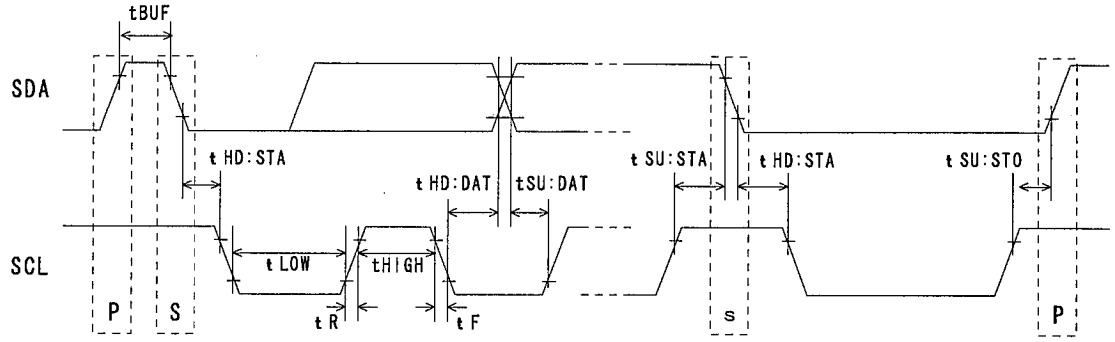
■ ELECTRICAL CHARACTERISTICS

V_{DD}=3 ± 10%, V_{SS}=0V, V_{LCD}=8V, Ta=-20 ~ +75℃

PARAMETER		SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	NOTE
Operating Voltage(1)	Recommend	V_{DD}			2.7	3.0	3.3	V	5
	Available				2.2	−	5.5	V	
Operating Voltage(2)	Available	V_{LCD}		Normal display mode	4.0	−	13.5	V	
				Icon mode	2.5	−	13.5	V	
"H" input voltage		V_{IH}	SCL, SDA terminals		0.7V_{DD}	−	V_{DD}	V	
"L" input voltage		V_{IL}	SCL, SDA terminals		V_{SS}	−	0.3V_{DD}	V	
Input leakage current		I_{IH}	SCL, SDA term.	V_{IH}=V_{DD}	−	−	5	uA	
		I_{IL}	SCL, SDA term.	V_{IL}=V_{SS}	−	−	5	uA	
"L" output voltage		V_{OL}	SDA term.	Io=3mA	−	−	V_{SS}+0.4	V	
Hysteresis voltage		V_{HYS}	SCL terminal		0.05V_{DD}	−	−	V	
Input capacitance		C_{IN}	SCL, SDA terminals		−	−	10	pF	
Driver on-resistance		R_{ON1}	COM/SEG term.	Io=*uA, V_{LCD}=13.5V	−	2.0	3.0	kΩ	6
		R_{ON2}		Io=*uA, V_{LCD}=8V	−	3.0	3.5	kΩ	
Standby current		I_{DDQ}	V_{DD} term.	Power save mode	T.B.D.			uA	7
Operating current for logic(1)		I_{DD1}	V_{DD} term.	Normal display mode V_{DD}=3V, V_{LCD}=8V	T.B.D.			uA	
Operating current for LCD driving(1)		I_{LCD1}	V_{LCD} term.		T.B.D.			uA	
Operating current for logic(2)		I_{DD2}	V_{DD} term.	Icon mode V_{DD}=3V, V_{LCD}=3V	T.B.D.			uA	
Operating current for LCD driving(2)		I_{LCD2}	V_{LCD} term.		T.B.D.			uA	
Oscillation frequency		F_{OSC}	F_{OSC} term.	V_{DD}=3V, Ta=25℃	T.B.D.			kHz	

Note5) NJU6576 operating voltage range is wide, but it is not guaranteed in immediate voltage change during access from MPU.
Note6) This characteristic is applied to resistances between V_{LCD} terminal and each output terminal, and between V_{SS} and each output terminal.
Note7) These characteristics are applied to operating current, in no access from MPU and SCL=SDA=V_{SS}.

■ I²C-BUS TIMING CHARACTERISTICS



VDD=3 ± 10%, VSS=0V, VLCD=8V, Ta=-20 ~ +75°C

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
SCL clock frequency	fSCL	0	400	kHz
Bus free time	tBUF	1.3	-	uS
START condition hold time	tHD:STA	0.6	-	uS
SCL"L" pulse width	tLOW	1.3	-	uS
SCL"H" pulse width	tHIGH	0.6	-	uS
START condition set-up time	tSU:STA	0.6	-	uS
Data hold time	tHD:DAT	0	0.9	uS
Data set-up time	tSU:DAT	100	-	nS
Rise time	tR	20+0.1Cb(*1)	300	nS
Fall time	tF	20+0.1Cb(*1)	300	nS
STOP condition set-up time	tSU:STO	0.6	-	uS

Note8)Cb= total capacitance of one line bus(unit;pF).

Note9)Each timing is specified based on 0.3xVDD and 0.7xVDD.

■ RESET CIRCUIT CHARACTERISTICS

-Input condition by hardware reset

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	NOTE
Reset time	tR	$\overline{\text{RESET}}$term.		1.0	-	-	uS	10
Reset "L" pulse width	tRW	$\overline{\text{RESET}}$term.		10	-	-	uS	11

Note10) This characteristic specifies time from the rise edge of reset signal to the internal reset circuit operating finish.

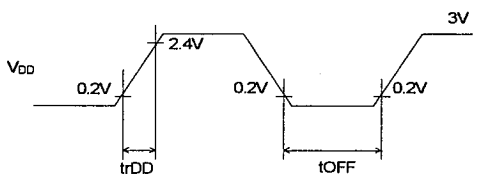
Note11) This characteristic specifies minimum pulse width of reset signal "L".

-Power supply condition by power on reset

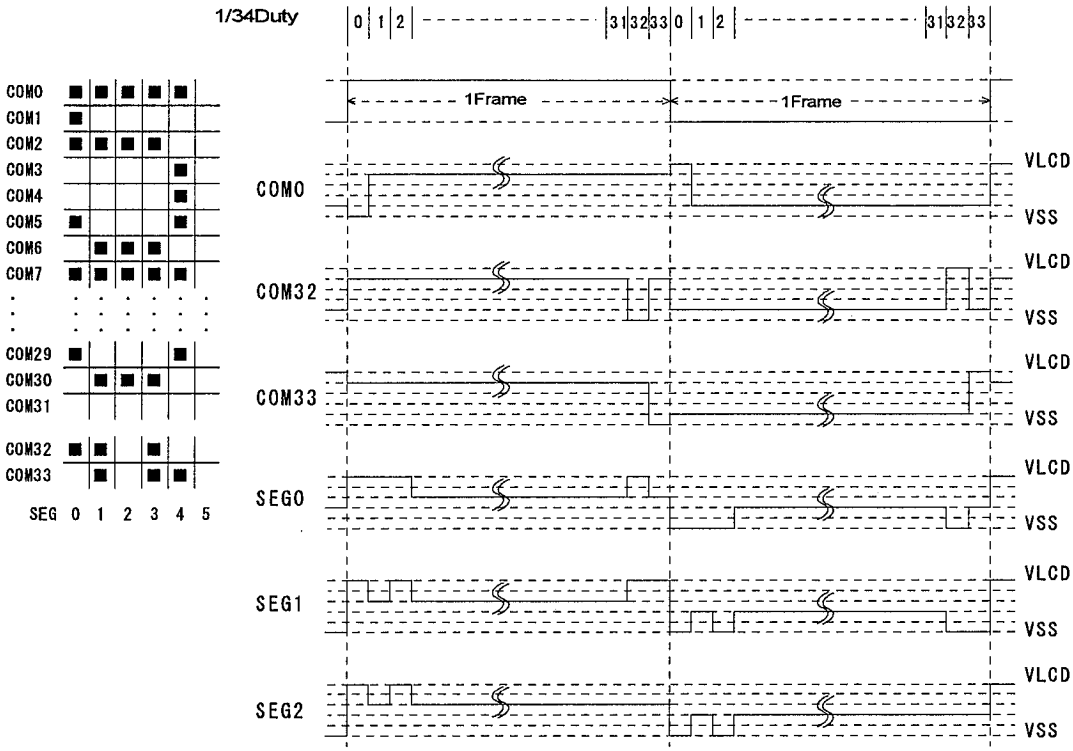
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Power supply rise time	trDD		0.5	-	5	mS	
Power supply off time	tOFF		1	-	-	mS	12

Note12)tOFF specifies the power off time in a shot period off or cycle on/off.

Note13)If power supply condition can not be followed, refer to (note2) in (1-4)Reset circuit.



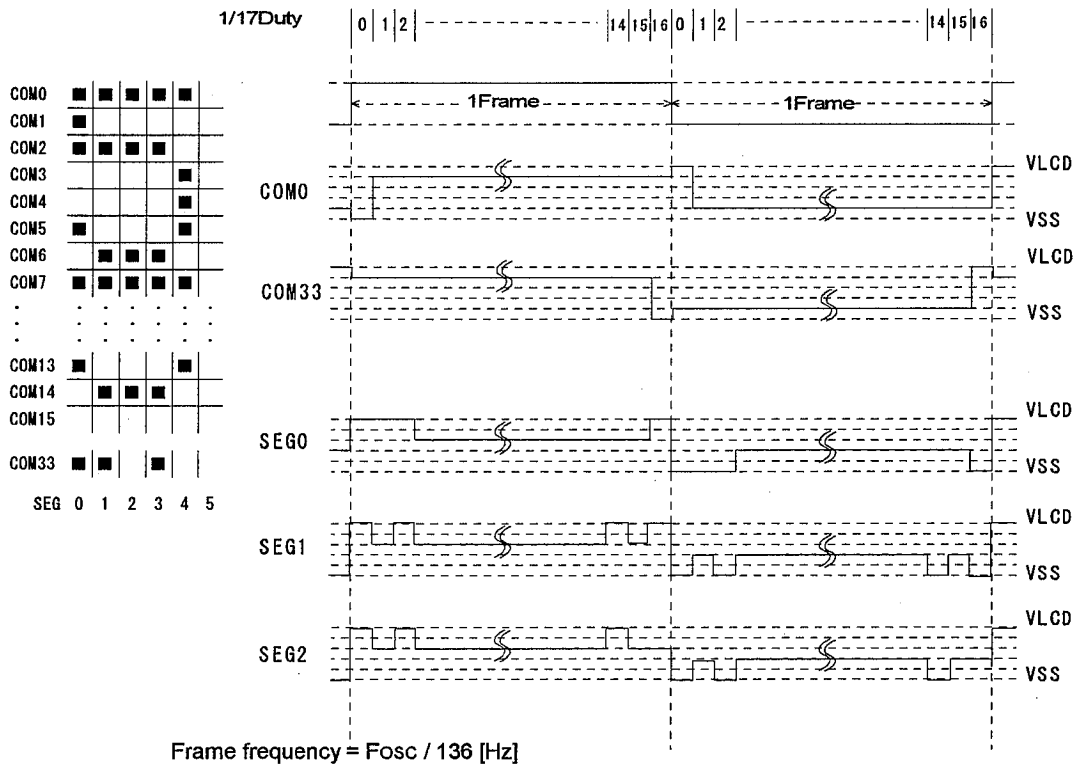
■ LCD DRIVING WAVEFORM(1)



Frame frequency = Fosc / 136 [Hz]

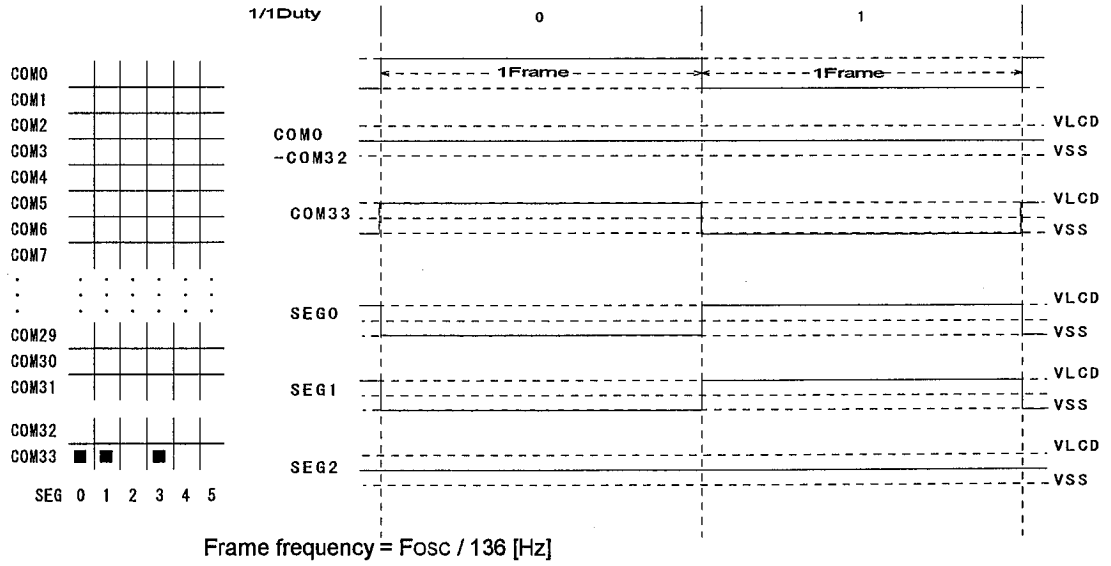
Fig.12 COM/SEG waving forms in 1/34-duty, in the normal display mode.

■ LCD DRIVING WAVEFORM(2)



Frame frequency = Fosc / 136 [Hz]

Fig.13 COM/SEG waving forms in 1/17duty, in the normal display mode.



Frame frequency = Fosc / 136 [Hz]

Fig.14 COM/SEG waving forms in 1/1-duty, in the Icon mode.

■APPLICATION CIRCUIT

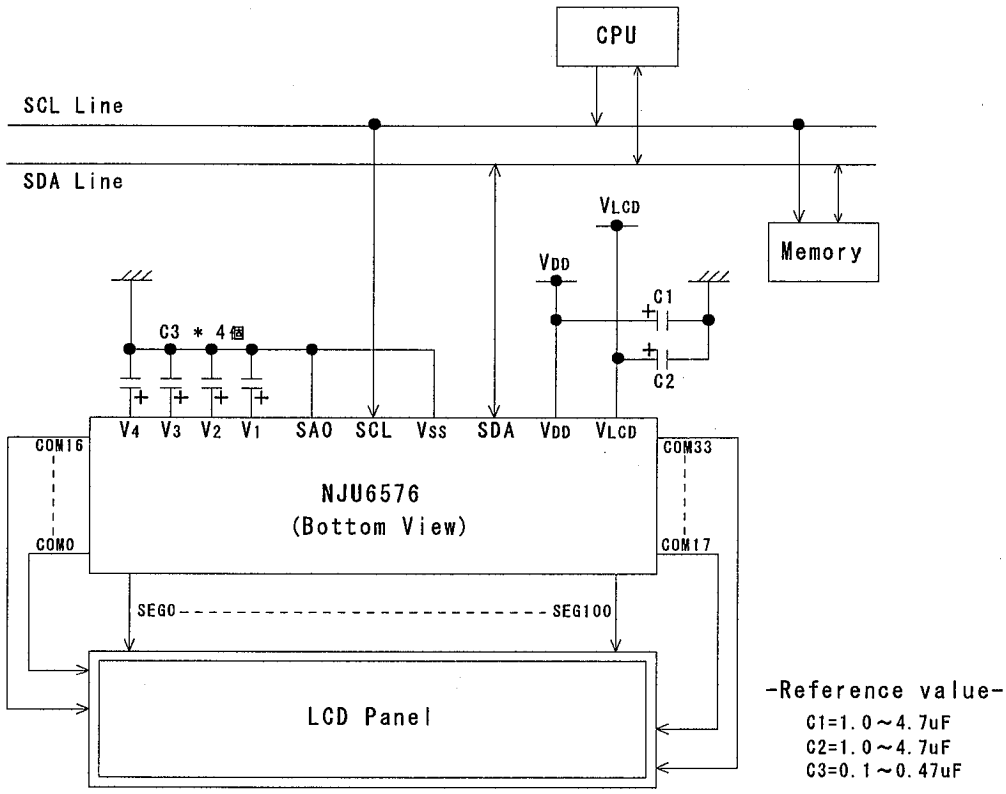


Fig.15 Typical application circuit

Note1) In order to stabilize LSI operation, the capacitors between V_{DD}-V_{SS} and between V_{LCD}-V_{SS} are required.
Note2) In order to realize high quality display, the capacitor between V_1, V_2, V_3, V_4 and V_{SS} are recommended.
In case these capacitors are not needed, V_1, V_2, V_3, V_4 terminals are open.
Note3) SA0 terminal state decides NJU6576 slave address bit0. Fix this terminal to V_{DD} or V_{SS}.

MEMO

[CAUTION]
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