

BIT MAP LCD DRIVER

■ GENERAL DESCRIPTION

The **NJU6577S** is a bit map LCD driver to display graphics or characters.

It contains 4,240 bits display data RAM, microprocessor interface circuits, instruction decoder, 80-segment and 53-common (1 out of 53-driver is prepared for icon display) drivers.

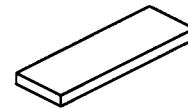
The bit image display data is transferred to the display data RAM by serial or 8-bit parallel interface mode.

53 x 80 dots graphics or 5-character 3-line by 16 x 16 dot character with icon are displayed by **NJU6577S** itself.

The wide operating voltage like as 2.4V to 5.5V and low operating current are useful to apply small sized battery operated items.

The build-in Electrical Variable Resistor is very precision, furthermore the rectangle outlook is very applicable to COG or Slim TCP.

■ PACKAGE OUTLINE

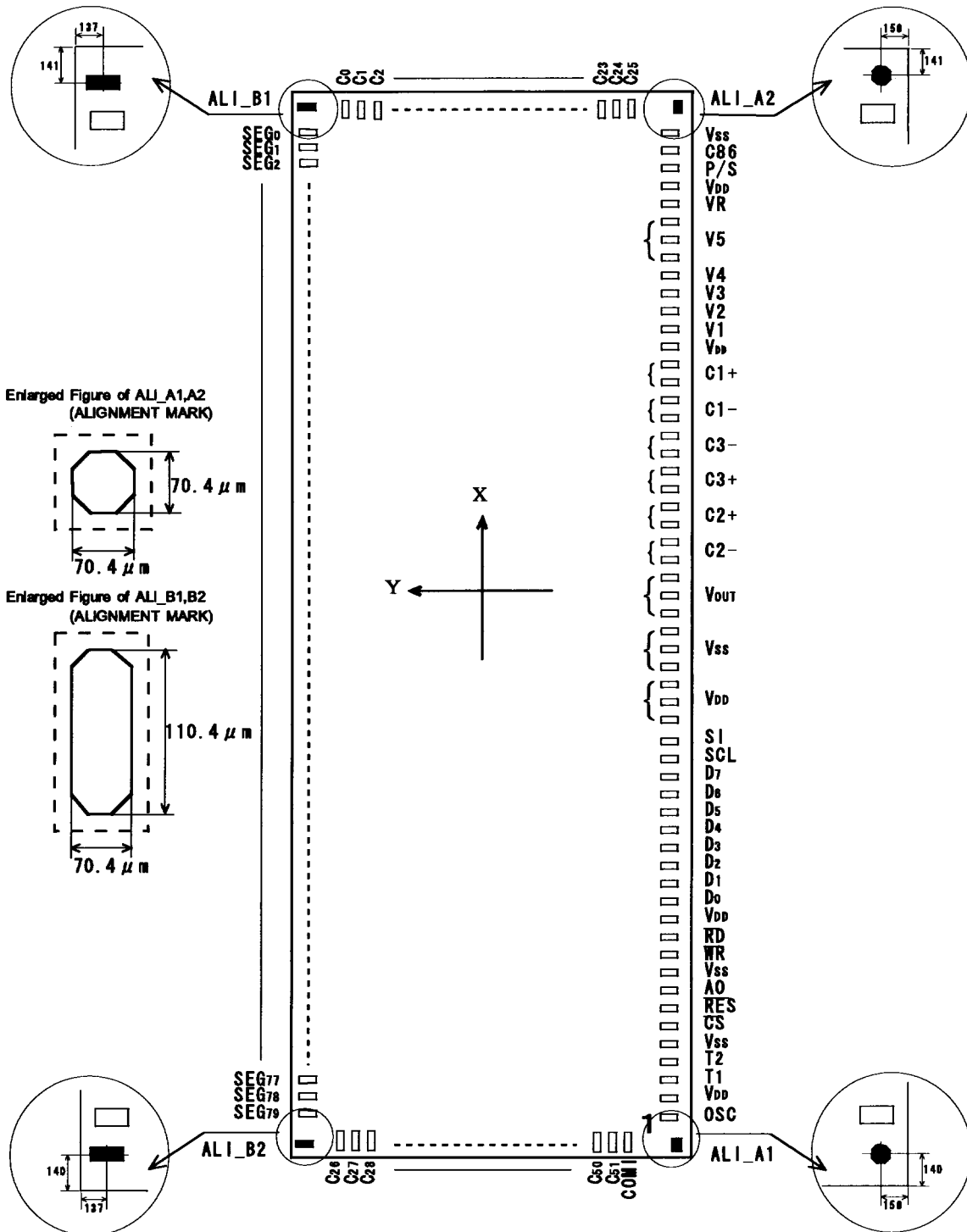


NJU6577SCH

■ FEATURES

- Direct Correspondence between Display Data RAM and LCD Pixel
- Display Data RAM - 4,240 bits
- 133 LCD Drivers - 53- common and 80-segment
- Direct Micro Processor interface for both of 68 and 80 type MPU
- Serial Interface
- Programmable Duty Ratio ; 1/52 or 1/53 Duty
- Useful Instruction Set
Display Data Read/Write, Display ON/OFF Cont, Inverse Display, Page Address Set, Display Starting Line Set, Column Address Set, Status Read, All On/Off, Icon Display, Read Modify Write
Common Driver order Assignment and Power Saving.
- Power Supply Circuits for LCD Incorporated
Voltage step up Circuits (quadrapular maximum), Regulator, Voltage Follower x 4
- Precision Electrical Variable Resistance
- Low Power Consumption
- Operating Voltage --- 2.4V to 5.5V
- LCD Driving Voltage --- 6.0V to 10V
- Package Outline --- TCP / Bumped Chip
- C-MOS Technology

■ PAD LOCATION



Chip Center X=0um, Y=0um
 Chip Size X=8.46mm, Y=2.88mm
 Chip Thickness 400um ± 30um
 PAD Pitch 80um
 Bump Size 60um x 110um
 Bump Height 25um TYP.
 Bump Material Au

■: Four PADs illustrated with this mark are the alignment marks for COG.



NJU6577S

■ PAD COORDINATES

Chip Size 8.46mm x 2.88mm(Chip Center X=0um,Y=0um)

No.	Terminal	X (μ m)	Y (μ m)
1	OSC	-3903	-1277
2	V _{DD}	-3823	-1277
3	T ₁	-3743	-1277
4	T ₂	-3663	-1277
5	V _{SS}	-3583	-1277
6	CS	-3503	-1277
7	RES	-3423	-1277
8	AO	-3343	-1277
9	V _{SS}	-3263	-1277
10	WR	-3183	-1277
11	RD	-3103	-1277
12	V _{DD}	-3023	-1277
13	D ₀	-2728	-1277
14	D ₁	-2228	-1277
15	D ₂	-1728	-1277
16	D ₃	-1228	-1277
17	D ₄	-728	-1277
18	D ₅	-228	-1277
19	D ₆	272	-1277
20	D ₇	772	-1277
21	SCL	1120	-1277
22	SI	1200	-1277
23	V _{DD}	1280	-1277
24	V _{DD}	1360	-1277
25	V _{DD}	1440	-1277
26	V _{SS}	1520	-1277
27	V _{SS}	1600	-1277
28	V _{SS}	1680	-1277
29	V _{OUT}	1760	-1277
30	V _{OUT}	1840	-1277
31	V _{OUT}	1920	-1277
32	C2 ⁻	2000	-1277
33	C2 ⁻	2080	-1277
34	C2 ⁺	2160	-1277
35	C2 ⁺	2240	-1277
36	C3 ⁺	2320	-1277
37	C3 ⁺	2400	-1277
38	C3 ⁻	2480	-1277
39	C3 ⁻	2560	-1277
40	C1 ⁻	2640	-1277
41	C1 ⁻	2720	-1277
42	C1 ⁺	2800	-1277
43	C1 ⁺	2880	-1277
44	V _{DD}	2960	-1277
45	V ₁	3040	-1277
46	V ₂	3120	-1277
47	V ₃	3200	-1277
48	V ₄	3280	-1277
49	V ₅	3360	-1277
50	V ₅	3440	-1277

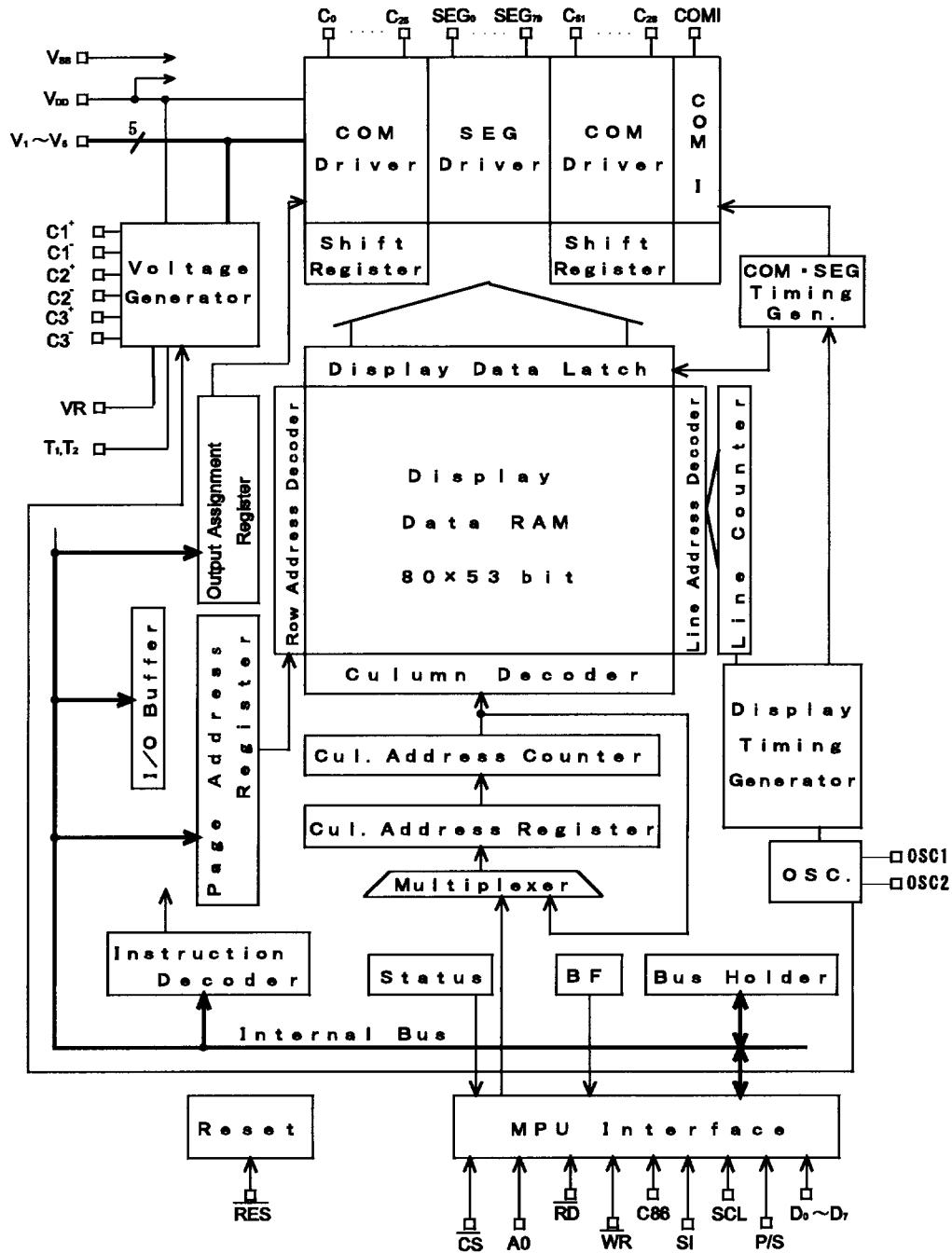
No.	Terminal	X (μ m)	Y (μ m)
51	V ₅	3520	-1277
52	VR	3600	-1277
53	V _{DD}	3680	-1277
54	P/S	3760	-1277
55	C ₈₈	3840	-1277
56	V _{SS}	3920	-1277
57	C ₂₅	4063	-880
58	C ₂₄	4063	-800
59	C ₂₃	4063	-720
60	C ₂₂	4063	-640
61	C ₂₁	4063	-560
62	C ₂₀	4063	-480
63	C ₁₉	4063	-400
64	C ₁₈	4063	-320
65	C ₁₇	4063	-240
66	C ₁₆	4063	-160
67	C ₁₅	4063	-80
68	C ₁₄	4063	0
69	C ₁₃	4063	80
70	C ₁₂	4063	160
71	C ₁₁	4063	240
72	C ₁₀	4063	320
73	C ₉	4063	400
74	C ₈	4063	480
75	C ₇	4063	560
76	C ₆	4063	640
77	C ₅	4063	720
78	C ₄	4063	800
79	C ₃	4063	880
80	C ₂	4063	960
81	C ₁	4063	1040
82	C ₀	4063	1120
83	SEG ₀	3145	1276
84	SEG ₁	3065	1276
85	SEG ₂	2985	1276
86	SEG ₃	2905	1276
87	SEG ₄	2825	1276
88	SEG ₅	2745	1276
89	SEG ₆	2665	1276
90	SEG ₇	2585	1276
91	SEG ₈	2505	1276
92	SEG ₉	2425	1276
93	SEG ₁₀	2345	1276
94	SEG ₁₁	2265	1276
95	SEG ₁₂	2185	1276
96	SEG ₁₃	2105	1276
97	SEG ₁₄	2025	1276
98	SEG ₁₅	1945	1276
99	SEG ₁₆	1865	1276
100	SEG ₁₇	1785	1276

New Japan Radio Co., Ltd.

No.	Terminal	X (μ m)	Y (μ m)
101	SEG ₁₈	1705	1276
102	SEG ₁₉	1625	1276
103	SEG ₂₀	1545	1276
104	SEG ₂₁	1465	1276
105	SEG ₂₂	1385	1276
106	SEG ₂₃	1305	1276
107	SEG ₂₄	1225	1276
108	SEG ₂₅	1145	1276
109	SEG ₂₆	1065	1276
110	SEG ₂₇	985	1276
111	SEG ₂₈	905	1276
112	SEG ₂₉	825	1276
113	SEG ₃₀	745	1276
114	SEG ₃₁	665	1276
115	SEG ₃₂	585	1276
116	SEG ₃₃	505	1276
117	SEG ₃₄	425	1276
118	SEG ₃₅	345	1276
119	SEG ₃₆	265	1276
120	SEG ₃₇	185	1276
121	SEG ₃₈	105	1276
122	SEG ₃₉	25	1276
123	SEG ₄₀	-55	1276
124	SEG ₄₁	-135	1276
125	SEG ₄₂	-215	1276
126	SEG ₄₃	-295	1276
127	SEG ₄₄	-375	1276
128	SEG ₄₅	-455	1276
129	SEG ₄₆	-535	1276
130	SEG ₄₇	-615	1276
131	SEG ₄₈	-695	1276
132	SEG ₄₉	-775	1276
133	SEG ₅₀	-855	1276
134	SEG ₅₁	-935	1276
135	SEG ₅₂	-1015	1276
136	SEG ₅₃	-1095	1276
137	SEG ₅₄	-1175	1276
138	SEG ₅₅	-1255	1276
139	SEG ₅₆	-1335	1276
140	SEG ₅₇	-1415	1276
141	SEG ₅₈	-1495	1276
142	SEG ₅₉	-1575	1276
143	SEG ₆₀	-1655	1276
144	SEG ₆₁	-1735	1276
145	SEG ₆₂	-1815	1276
146	SEG ₆₃	-1895	1276
147	SEG ₆₄	-1975	1276
148	SEG ₆₅	-2055	1276
149	SEG ₆₆	-2135	1276
150	SEG ₆₇	-2215	1276

No.	Terminal	X (μ m)	Y (μ m)
151	SEG ₆₈	-2295	1276
152	SEG ₆₉	-2375	1276
153	SEG ₇₀	-2455	1276
154	SEG ₇₁	-2535	1276
155	SEG ₇₂	-2615	1276
156	SEG ₇₃	-2695	1276
157	SEG ₇₄	-2775	1276
158	SEG ₇₅	-2855	1276
159	SEG ₇₆	-2935	1276
160	SEG ₇₇	-3015	1276
161	SEG ₇₈	-3095	1276
162	SEG ₇₉	-3175	1276
163	C ₂₆	-4064	1121
164	C ₂₇	-4064	1041
165	C ₂₈	-4064	961
166	C ₂₉	-4064	881
167	C ₃₀	-4064	801
168	C ₃₁	-4064	721
169	C ₃₂	-4064	641
170	C ₃₃	-4064	561
171	C ₃₄	-4064	481
172	C ₃₅	-4064	401
173	C ₃₆	-4064	321
174	C ₃₇	-4064	241
175	C ₃₈	-4064	161
176	C ₃₉	-4064	81
177	C ₄₀	-4064	1
178	C ₄₁	-4064	-79
179	C ₄₂	-4064	-159
180	C ₄₃	-4064	-239
181	C ₄₄	-4064	-319
182	C ₄₅	-4064	-399
183	C ₄₆	-4064	-479
184	C ₄₇	-4064	-559
185	C ₄₈	-4064	-639
186	C ₄₉	-4064	-719
187	C ₅₀	-4064	-799
188	C ₅₁	-4064	-879
189	COMI	-4064	-959
Alignment Mark	ALI_A1	-4090	-1303
Alignment Mark	ALI_A2	4089	-1303
Alignment Mark	ALI_B1	4089	1282
Alignment Mark	ALI_B2	-4090	1282

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

No.	Symbol	I/O	Function																				
2,12,23, 24,25,44, 53	V _{DD}	Power	V _{DD} =+3V. (Less than 3.3V should apply when 3-time voltage booster using.)																				
5,9,26, 27,28,56	V _{SS}	GND	V _{SS} =0V																				
45 46 47 48 49,50,51	V ₁ V ₂ V ₃ V ₄ V ₅	Power	<p>LCD Driving Voltage Supplying Terminal. When the internal tripler is not used, supply each level from outside maintained following relation. $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$</p> <p>When the internal power supply is on, the internal circuits generates and supply following LCD bias voltage from V₁ to V₄ terminals.</p> <table border="1" style="margin: 10px auto; border-collapse: collapse;"> <thead> <tr> <th>Device</th> <th>V₁</th> <th>V₂</th> <th>V₃</th> <th>V₄</th> </tr> </thead> <tbody> <tr> <td>NJU6577S</td> <td>$V_5 + 5/6V_{LCD}$</td> <td>$V_5 + 4/6V_{LCD}$</td> <td>$V_5 + 2/6V_{LCD}$</td> <td>$V_5 + 1/6V_{LCD}$</td> </tr> </tbody> </table> <p style="text-align: right; margin-right: 50px;"><small>(V_{LCD}=V_{DD}-V₅)</small></p>	Device	V ₁	V ₂	V ₃	V ₄	NJU6577S	$V_5 + 5/6V_{LCD}$	$V_5 + 4/6V_{LCD}$	$V_5 + 2/6V_{LCD}$	$V_5 + 1/6V_{LCD}$										
Device	V ₁	V ₂	V ₃	V ₄																			
NJU6577S	$V_5 + 5/6V_{LCD}$	$V_5 + 4/6V_{LCD}$	$V_5 + 2/6V_{LCD}$	$V_5 + 1/6V_{LCD}$																			
42,43 40,41 34,35 32,33 36,37 38,39	C1 ⁺ C1 ⁻ C2 ⁺ C2 ⁻ C3 ⁺ C3 ⁻	0	<p>Voltage set up capacitor connecting terminals.</p> <p>- In case of tripled voltage step up connect the capacitor between C1⁺ and C1⁻, C2⁺ and C2⁻, connect C2⁻ to C3⁻, and C3⁺ should be open (or correct the capacitors between C1⁺ and C1⁻, C3⁺ and C3⁻, connect C2⁺ to C3⁺, and C2⁻ should be open.)</p> <p>- In case of doubled voltage step up operation, connect the capacitor between C1⁺ and C1⁻, connect C1⁻ to C3⁻, and C2⁻, C2⁺, C3⁺ should be open.</p>																				
29,30,31	V _{OUT}	0	Step up voltage output terminal. Connect the voltage boost capacitor between this terminal and V _{SS} .																				
52	VR	I	Voltage adjust terminal. V ₅ level is adjusted by external bleeder resistance connect between V _{DD} and V5 terminal.																				
3 4	T ₁ T ₂	I	<p>LCD bias voltage control terminals. ※ Don't Care</p> <table border="1" style="margin: 10px auto; border-collapse: collapse;"> <thead> <tr> <th>T₁</th> <th>T₂</th> <th>Voltage Boost Circuit</th> <th>Voltage Adj.</th> <th>V/F Cir.</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>※</td> <td>Available</td> <td>Available</td> <td>Available</td> </tr> <tr> <td>H</td> <td>L</td> <td>Not Avail.</td> <td>Available</td> <td>Available</td> </tr> <tr> <td>H</td> <td>H</td> <td>Not Avail.</td> <td>Not Avail.</td> <td>Available</td> </tr> </tbody> </table>	T ₁	T ₂	Voltage Boost Circuit	Voltage Adj.	V/F Cir.	L	※	Available	Available	Available	H	L	Not Avail.	Available	Available	H	H	Not Avail.	Not Avail.	Available
T ₁	T ₂	Voltage Boost Circuit	Voltage Adj.	V/F Cir.																			
L	※	Available	Available	Available																			
H	L	Not Avail.	Available	Available																			
H	H	Not Avail.	Not Avail.	Available																			
13 ~ 20	D ₀ to D ₇	I/O	Tri-state bi-directional Data I/O terminal in 8-bit parallel operation.																				
8	A0	I	<p>Connect to the Address bus of MPU. The data on the D₀ to D₇ is distinguished between Display data and Instruction by status of A₀.</p> <table border="1" style="margin: 10px auto; border-collapse: collapse;"> <thead> <tr> <th>A0</th> <th>H</th> <th>L</th> </tr> </thead> <tbody> <tr> <td>Dist.</td> <td>Display Data</td> <td>Instruction</td> </tr> </tbody> </table>	A0	H	L	Dist.	Display Data	Instruction														
A0	H	L																					
Dist.	Display Data	Instruction																					
7	\overline{RES}	I	Reset terminal. When the \overline{RES} terminal goes to "L", the initialization is performed. Reset operation is executing during "L" state of \overline{RES} .																				
6	\overline{CS}	I	Chip select terminal. Data Input/Output are available during \overline{CS} ="L".																				

No.	Symbol	I/O	F u n c t i o n																		
11	\overline{RD} (E)	I	<p><In case of 80 type MPU> \overline{RD} signal of 80 type MPU input terminal. Active "L". During this signal "L", the data bus becomes as output terminal.</p> <p><In case of 68 type MPU> Enable signal of 68 type MPU input terminal. Active "H".</p>																		
10	\overline{WR} (R/W)	I	<p><In case of 80 type MPU> Connect to the 80 type MPU \overline{WR} signal. Active "L". The data on the data bus input synchronizing the rise edge of this signal.</p> <p><In case of 68 type MPU> Read/write control signal of 68 type MPU input terminal.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>R/W</td> <td>H</td> <td>L</td> </tr> <tr> <td>State</td> <td>Read</td> <td>Write</td> </tr> </table>	R/W	H	L	State	Read	Write												
R/W	H	L																			
State	Read	Write																			
55	C86	I	<p>MPU interface type selection terminal.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>C86</td> <td>H</td> <td>L</td> </tr> <tr> <td>Status</td> <td>68 Type</td> <td>80 Type</td> </tr> </table>	C86	H	L	Status	68 Type	80 Type												
C86	H	L																			
Status	68 Type	80 Type																			
22	SI	I	Serial data input terminal .																		
21	SCL	I	Serial data clock signal input terminal. SI data input at the rise edge of SCL in successively. It convert to the parallel data at the 8th SCL clock rise edge.																		
54	P/S	I	<p>Serial or parallel interface selection terminal.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>P/S</th> <th>Chip Select</th> <th>Data/Command</th> <th>Data</th> <th>Read/Write</th> <th>Serial CLK</th> </tr> </thead> <tbody> <tr> <td>"H"</td> <td>\overline{CS}</td> <td>A0</td> <td>D₀~D₇</td> <td>\overline{RD}、\overline{WR}</td> <td>—</td> </tr> <tr> <td>"L"</td> <td>\overline{CS}</td> <td>A0</td> <td>SI</td> <td>Write only</td> <td>SCL</td> </tr> </tbody> </table> <p>*RAM data and status read operation do not work in mode of the serial interface.</p> <ul style="list-style-type: none"> • In case of select the parallel interface (P/S="H"), SI and SCL must be fixed "H" or "L". • In case of select the serial interface (P/S="L"), \overline{RD} and \overline{WR} must be fix "H" or "L", and D₀~D₇ are high impedance . 	P/S	Chip Select	Data/Command	Data	Read/Write	Serial CLK	"H"	\overline{CS}	A0	D ₀ ~D ₇	\overline{RD} 、 \overline{WR}	—	"L"	\overline{CS}	A0	SI	Write only	SCL
P/S	Chip Select	Data/Command	Data	Read/Write	Serial CLK																
"H"	\overline{CS}	A0	D ₀ ~D ₇	\overline{RD} 、 \overline{WR}	—																
"L"	\overline{CS}	A0	SI	Write only	SCL																
1	OSC1	I	System clock input terminal for Maker testing.. This terminal should be open.																		

No.	Symbol	I/O	F u n c t i o n																																	
57 ~ 82	C ₂₅ ~ C ₀	O	<p>LCD driving signal output terminals. Segment output terminals : SEG₀ to SEG₇₉ Common output terminals :C₀ to C₅₁</p> <p>• Segment output terminal Segment driving output terminals. The following output voltages are selected by the combination of FR and data in the RAM.</p> <table border="1"> <thead> <tr> <th rowspan="2">RAM Data</th> <th rowspan="2">FR</th> <th colspan="2">Output Voltage</th> </tr> <tr> <th>Normal</th> <th>Reverse</th> </tr> </thead> <tbody> <tr> <td rowspan="2">H</td> <td>H</td> <td>V_{DD}</td> <td>V₂</td> </tr> <tr> <td>L</td> <td>V₅</td> <td>V₃</td> </tr> <tr> <td rowspan="2">L</td> <td>H</td> <td>V₂</td> <td>V_{DD}</td> </tr> <tr> <td>L</td> <td>V₃</td> <td>V₅</td> </tr> </tbody> </table> <p>• Common Output Terminal Common driving output terminals. The following output voltages are selected by the combination of FR and status of common .</p> <table border="1"> <thead> <tr> <th>Status of Common</th> <th>FR</th> <th>Output Voltage</th> </tr> </thead> <tbody> <tr> <td rowspan="2">H</td> <td>H</td> <td>V₅</td> </tr> <tr> <td>L</td> <td>V_{DD}</td> </tr> <tr> <td rowspan="2">L</td> <td>H</td> <td>V₁</td> </tr> <tr> <td>L</td> <td>V₄</td> </tr> </tbody> </table>	RAM Data	FR	Output Voltage		Normal	Reverse	H	H	V _{DD}	V ₂	L	V ₅	V ₃	L	H	V ₂	V _{DD}	L	V ₃	V ₅	Status of Common	FR	Output Voltage	H	H	V ₅	L	V _{DD}	L	H	V ₁	L	V ₄
RAM Data	FR					Output Voltage																														
				Normal	Reverse																															
H	H			V _{DD}	V ₂																															
	L	V ₅	V ₃																																	
L	H	V ₂	V _{DD}																																	
	L	V ₃	V ₅																																	
Status of Common	FR	Output Voltage																																		
H	H	V ₅																																		
	L	V _{DD}																																		
L	H	V ₁																																		
	L	V ₄																																		
83 ~ 162	SEG ₀ ~ SEG ₇₉																																			
163 ~ 189	C ₂₆ ~ C ₅₁																																			
	COM1	O	<p>Icon common output terminal. Icon common output when Icon Display instruction execution.</p> <table border="1"> <thead> <tr> <th></th> <th>Icon Display ON</th> <th>Icon Display OFF</th> </tr> </thead> <tbody> <tr> <td>State</td> <td>COM₅₂</td> <td>V₁ or V₄</td> </tr> </tbody> </table>		Icon Display ON	Icon Display OFF	State	COM ₅₂	V ₁ or V ₄																											
	Icon Display ON	Icon Display OFF																																		
State	COM ₅₂	V ₁ or V ₄																																		

■ Functional Description

(1) Description for each blocks

(1-1) Busy Flag (BF)

While the internal circuits are operating, the busy flag (BF) is "1", and any instruction excepting for the status read are inhibited.

The busy flag output from D₇ terminal when status read instruction is executed.

When enough cycle time over than t_{cyc} indicated in "BUS TIMING CHARACTERISTICS" is ensured, no need to check the busy flag for reduction of the MPU load.

(1-2) Line Counter

The Line Counter generates the line address of display data RAM by the count up operation synchronizing the common cycle after the reset operation at the status change of internal FR signal.

(1-3) Column Address Counter

The column address counter is 8-bit presettable counter which addressing the column address as shown in Fig. 1. This counter increments (+1) up to (A0)_H when the Display Data Read/Write instruction is executed. This counter auto-increment up to (4F)_H, but accessing to the display data RAM over than (4F)_H is forbidden.

Furthermore, this counter is independent with the Page Register.

By the Address Inverse Instruction, the column address decoder inverse the column address of Display Data RAM corresponding to the Segment Driver.

(1-4) Page Register

The page register gives a page address of Display Data RAM as shown in Fig. 1. When the MPU accesses the data with the page change, the page address set instruction is required. Page address "7" (D₂, D₁, D₀ = "H") is Icon RAM area, the data only for the D₀ is valid.

(1-5) Display Data RAM

Display Data RAM is the bit map RAM consisting of 4,240 bits memorize the display data corresponding to each pixel of LCD panel. The each bit in the Display Data RAM corresponds to the each pixel of the LCD panel and controls the display by following bit data.

When Normal Display : On="1" , Off="0"

When Inverse Display : On="0" , Off="1"

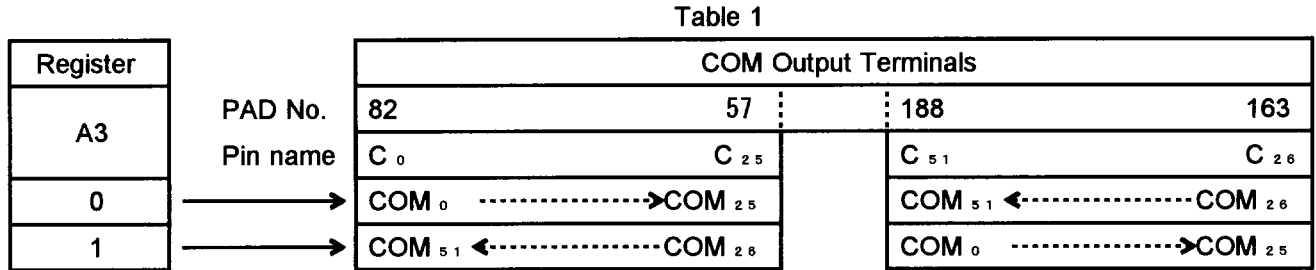
The Display Data RAM outputs 80-bit parallel data in the area addressed by the line counter, and these data are set into the Display Data Latch.

The access operation from MPU to the display data RAM and the data output from the display data RAM are so controlled to operate independently that the data rewriting does not influence with any malfunctions to the display.

The relation between column address and segment output can inverse by the Address Inverse Instruction ADC as shown in Fig. 1.

(1-6) Common Driver Assignment

The scanning order can be assigned by setting A₃ of the Output Assignment Register as shown on Table 1.



The Icon display is regardless with this function, therefore the Icon Display instruction must be executed when the Icon display is needed. In this time, the Icon display driver COM₁ is fixed to COM₅₂ timing regardless the other Common Driver assignment.

(1-7) Reset Circuit

Reset circuit operates the following initializations when the condition of \overline{RES} terminals goes to "L" level..

Initialization

- ① Display Off
- ② Normal Display (Non-inverse display)
- ③ Icon Display Reset
- ④ ADC Select : Normal (ADC Instruction D₀="0")
- ⑤ Read Modify Write Mode Off
- ⑥ Internal Power supply (Step up) circuits Off
- ⑦ Clear the serial interface register
- ⑧ Set the address (00)_H to the Column Address Counter
- ⑨ Set the page "0" to the Page Address Register
- ⑩ Select the D₃ of the Output Assignment Register to "0"
- ⑪ Set the EVR register to (00)_H

The \overline{RES} terminal should be connected to the Reset terminal of MPU for the initialization at the mean time with MPU as shown in "MPU Interface Example". The period of reset signal requires over than 10us \overline{RES} ="L" level input as shown in "Electrical Characteristics". After 1us from the rise edge of \overline{RES} signal, the operation goes to normal.

When the internal LCD power supply is not used, the external LCD power supply into the NJU6577 must be turned on during \overline{RES} = "L". Although the condition of \overline{RES} ="L" clear each registers and initialize as above, the oscillation circuit and output terminal conditions (D₀ ~ D₇) are no influenced. The initialization must be performed using \overline{RES} terminal at the power on, to prevent hung up or incorrect operations.

The reset Instruction performs the initialization procedures from No.8 to No.11 as shown in above.

Caution) The noise into the \overline{RES} terminal should be eliminated to avoid the error on the application with the careful design.

(1-8) LCD Driving

(a) LCD Driving Circuits

LCD driving circuits are consisted of 133 multiplexers which operate as 80 Segment drivers, 52 Common drivers and 1 Icon common driver. 52 Common drivers with the shift register scan the common display signal. The combination of the Display data, COM scan signal and FR signal form the define the LCD driving output voltage. The output wave form is mentioned in the Fig. 7.

(b) Display Data Latch Circuits

Display Data Latch stores 80-bit display data temporarily which is output to LCD driver circuits at a common cycle from Display Data RAM addressed by Line Counter. The instructions of Display On/Off, Display inverse ON/OFF and Static Drive On/Off control only the data in Display Data Latch, therefore, the data in the Display Data RAM is not changed.

(c) Line Counter and Latch signal of Latch Circuits

The clock to Line Counter and latch signal to the Latch Circuits are generated from the internal display clock (CL). The line address of Display Data RAM is renewed by synchronizing with display clock (CL). 80 bits display data are latched into display latch circuits synchronizing with display clock, and then output to the LCD driving circuits. The display data transfer to the LCD driving circuits is executed independently with RAM access by the MPU.

(d) Display Timing Generator

Display Timing Generator generates the timing signal for the display system by combination of the master clock CL and Driving Signal FR (refer to Fig.2). The Frame Signal FR and LCD alternative signal generate LCD driving waveform of two frame alternative driving method I.

(e) Common Timing Generation

The common timing is generated by display clock CL (refer to Fig.2).

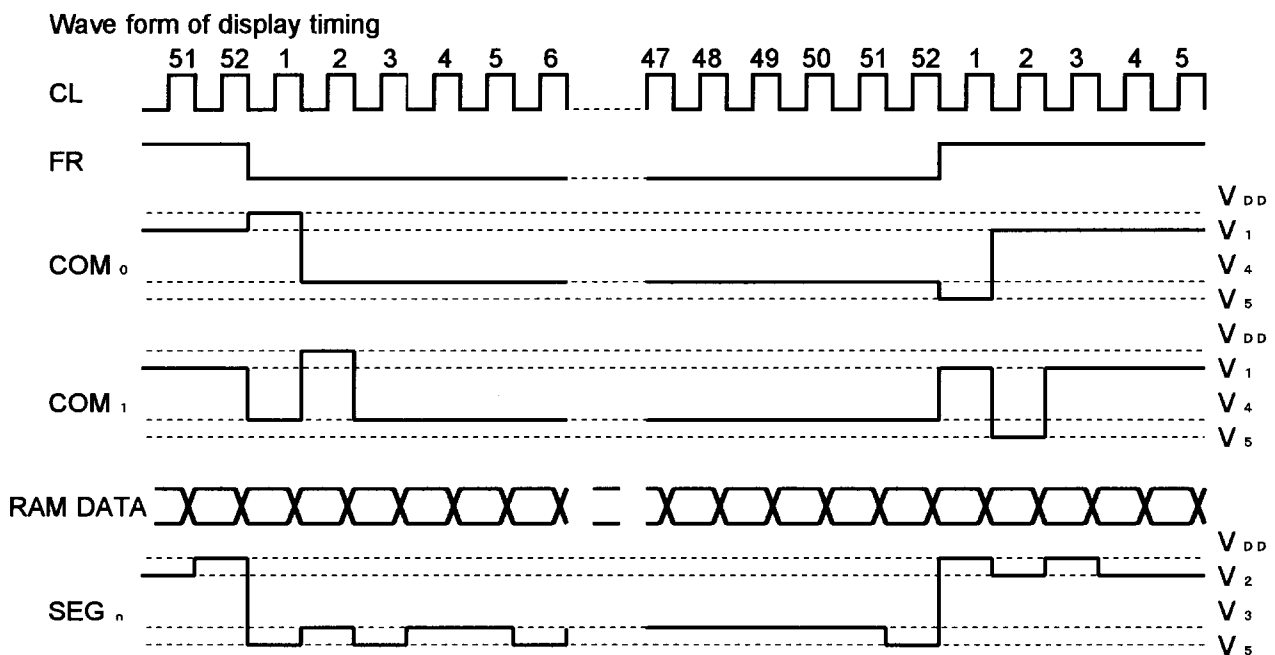


Fig. 2 Waveform of Display Timing

(f) Oscillation Circuit

The Oscillation Circuit is a low power CR oscillator incorporating with a Resistor and a Capacitor. It generates clocks for display timing signal source and the clock for step up circuits for LCD driving. The oscillation circuit output frequency is divided by 4 which is used as display clock CL.

(g) Power Supply Circuits

Internal Power Supply Circuit generate the High voltage and Bias voltage for the LCD. The power Supply Circuit consists of Voltage step up circuit(Tripler maximum) Circuits, Regulator Circuits, and Voltage Followers. The internal Power Supply is designed for small size LCD panel, therefore it is not suitable for the large size LCD panel application. If the contrast is no good the large size LCD panel application, please supply the external.

The suitable values of the capacitors connecting to the V1 to V5 terminals and the step up circuit, and the feedback resistors for V5 operational amplifier depend on the LCD panel. And the power consumption with the LCD panel is depending on the display pattern. Please evaluation with actual modules.

The operation of internal Power Supply Circuits is controlled by the Internal Power Supply On/Off Instruction. When the Internal Power Supply Off Instruction is executed, all of the Voltage booster circuits, regulator circuits, voltage follower circuits are turned off. In this time, the bias voltage of V₁, V₂, V₃, V₄, and V₅ for the LCD should be supplied from outside, terminals C1⁺, C1⁻, C2⁺, C2⁻, C3⁺, C3⁻ and VR should be open. The status of internal power supply is selected by T₁ and T₂ terminal. Furthermore the external power supply operates with some of internal power supply function.

Table 3.

(*:Don't Care)

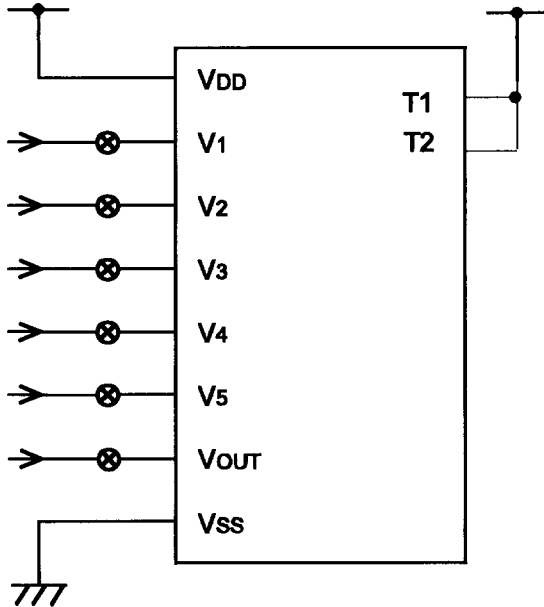
T ₁	T ₂	Step up	Voltage Adj.	Buffer (V/F)	Ext. Pow Supply	C1+,C1-,C2+,C2-	VR Term.
L	*	○	○	○	-		
H	L	×	○	○	V _{OUT}	OPEN	
H	H	×	×	○	V _S , V _{OUT}	OPEN	OPEN

When (T1, T2)=(H, L), C1+, C1-, C2+, C2-,C3+, C3-, C4+, C4- terminals for voltage booster circuits are open because the voltage booster circuits doesn't operate. Therefore LCD driving voltage to the VOUT terminal should be supplied from outside.

When (T1, T2)=(H, H), terminals for voltage booster circuits and VR are open, because the voltage booster circuits and Voltage adjust circuits do not operate.

○ Power Supply application.

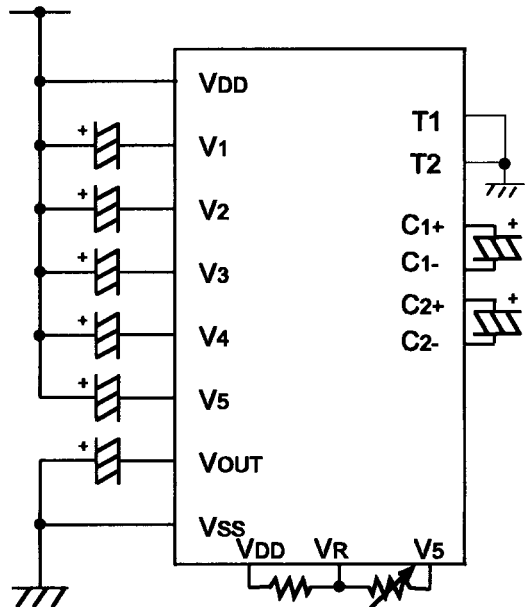
(1) External power supply operation.



(2) Internal power supply operation.

(Step up, Voltage Adj., Buffer(V/F))

Internal power supply ON(instruction) (T1,T2)=(L,L)

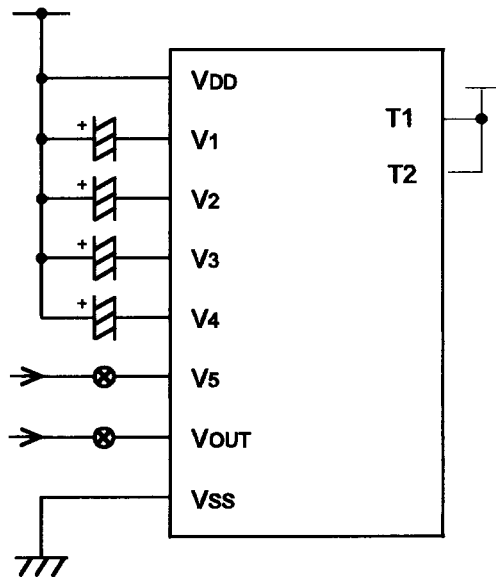
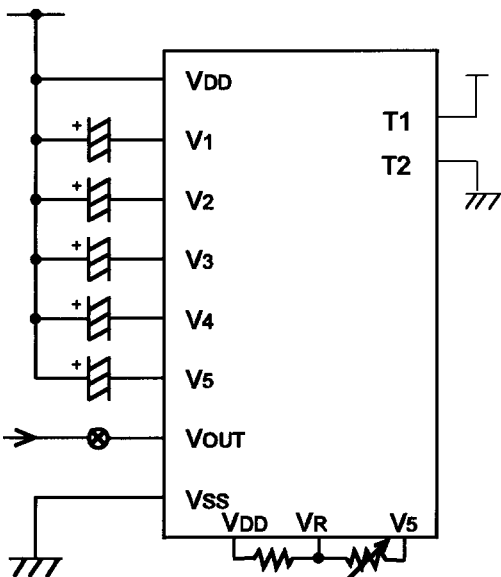


(3) External power supply operation with Voltage Adjustment, Buffer(V/F)

Internal power supply ON (Instruction) (T1,T2)=(H,L)

(4) External power supply operation adjusted Voltage to V5. Buffer(V/F)

Internal power supply (Instruction) (T1,T2)=(H,H)



* ⊗ : These switches should be open during the power save mode.

(2) Instruction

The NJU6577S distinguishes the signal on the data bus by combination of A_0 , \overline{RD} and \overline{WR} . Normally, the busy check is not required as the NJU6577S is operating so first because of the decode of the instruction and execution are performed only depending on the internal timing only neither the external clock. In case of serial interface, the data input as MSB first serially.

The Table. 4 shows the instruction codes of the NJU6577S.

Table 4. Instruction Code

Instruction	Code											Description	
	A0	\overline{RD}	\overline{WR}	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0	1	LCD Display ON/OFF 0:OFF 1:ON
(2) Page Address Set	0	1	0	1	0	1	1	*	Page Address			Set the page of DD RAM to the Page Add. Register	
(3) Column Address Set High Order 4bit	0	1	0	0	0	0	1	High Order Column Add.			Set the Higher order 4 bits Column Address to the Reg.		
(4) Column Address Set Lower Order 4bit	0	1	0	0	0	0	0	Lower order Column Add.			Set the Lower order 4 bits Column Address to the Reg.		
(5) Status Read	0	0	1	Status				0	0	0	0	Read out the internal Status	
(6) Write Display Data	1	1	0	Write Data							Write the data into the Display Data RAM		
(7) Read Display Data	1	0	1	Read Data							Read the Data from the Display Data RAM		
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0	1	Set the DD RAM vs Segment 0:Normal 1:Inverse
(9) Normal or Inverse of On/Off Set	0	1	0	1	0	1	0	0	1	1	0	1	Inverse the On and Off Display 0:Normal 1:Inverse
(10) Whole Display On /Normal Display	0	1	0	1	0	1	0	0	1	0	0	1	Whole Display Turns On 0:Normal 1:Whole Disp. On
(11) Icon Display	0	1	0	1	0	1	0	1	0	1	0	1	Set the Duty Ratio 0:No Icon 1:With Icon
(12) Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	0	Increment the Column Add. Register when writing but no-change when reading
(13) End	0	1	0	1	1	1	0	1	1	1	0	0	Release from the Read Modify Write Mode
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	0	Initialize the internal Circuits
(15) Output Assignment Register Set	0	1	0	1	1	0	0	A ₃	*	*	*	*	Set the scanning order of common drivers to the Register
(16) Internal Power Supply On/Off	0	1	0	0	0	1	0	0	1	0	0	1	0:Int. Power Supply Off 1:Int. Power Supply On
(17) LCD Driving Voltage Set	0	1	0	1	1	1	0	1	1	0	1	1	Set LCD Driving Voltage after after the internal (external) power supply is turned on
(18) EVR Register Set	0	1	0	1	0	0	0	Setting Data			Set the V _s output level to the EVR register		
(19) Power Save (Dual Command)	0	1	0	1	0	1	0	1	1	1	0	0	Set the Power save Mode
	0	1	0	1	0	1	0	0	1	0	1	1	

(*:Don't Care)

(3) Explanation of Instruction Code

(a) Display On/Off

This instruction executes whole display On/Off no relation with the data in the Display Data RAM and internal conditions.

A0	\overline{RD}	\overline{WR}	D ₇ _____							D ₀
0	1	0	1	0	1	0	1	1	1	D

D 0: Display Off
1: Display On

(b) Page Address Set

When MPU accesses the Display Data RAM, the page address must be selected before the data writing. The access to the Display Data RAM is available by setting the page and column addresses set (Refer the Fig. 1.). The page address change does not influence with the display.

A0	\overline{RD}	\overline{WR}	D ₇ _____							D ₀
0	1	0	1	0	1	1	*	A ₂	A ₁	A ₀

(*:Don't Care)

A ₂	A ₁	A ₀	Page
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

(c) Column Address

When MPU accesses the Display Data RAM, the page address set(refer(b) in front page) and column address set are required before the data writing. The column address set requires twice address set which are higher order 4 bits address set and lower order 4 bits. When the MPU accesses the Display Data RAM sequentially, the column address is increase one by one automatically, therefore, the MPU can access only the data sequentially without address set

This counter auto-increment up to (A0)_H, but accessing to the display data RAM over than (4F)_H is forbidden.

After writing 1 page data, page address setting is required due to page address doesn't increase automatically.

	A0	\overline{RD}	\overline{WR}	D ₇ _____				D ₀			
Higher Order	0	1	0	0	0	0	1	A7	A6	A5	A4
Lower Order	0	1	0	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Column Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
								⋮
0	1	0	0	1	1	1	1	4F

(d) Status Read

This instruction reads out the internal status of "BUSY", "ADC", "ON/OFF" and "RESET".

	A0	\overline{RD}	\overline{WR}	D ₇ _____				D ₀			
	0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY : BUSY=1 indicate the operating or the Reset cycle.

The instruction can be input after the BUSY status change to "0".

ADC : Indicate the output correspondence of column(segment) address and segment driver.

0 : Counterclockwise Output (Inverse) Column Address 79-n ↔ Segment Driver n

1 : Clockwise Output (Normal) Column Address n ↔ Segment Driver n

(Note) The data "0=Inverse" and "1=Normal" of ADC is inverted with the ADC select Instruction of "1=Inverse" and "0=Normal".

ON/OFF : Indicate the whole display On/Off status.

0 : Whole Display "On"

1 : Whole Display "Off"

(Note) The data "0=On" and "1=Off" of Display On/Off status read out is inverted with the Display On/Off instruction data of "1=On" and "0=Off".

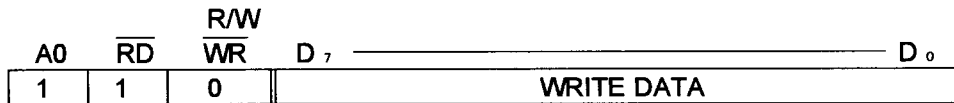
RESET : Indicate the initializing period by \overline{RES} signal or reset instruction.

0 : —

1 : Initialization Period

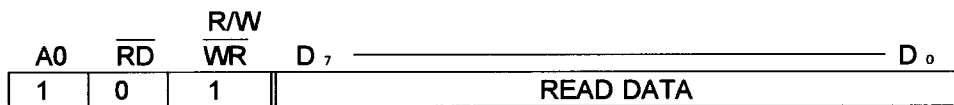
(e) Write Display Data

This instruction writes the 8-bit data on the data bus into the Display Data RAM. The column address increases "1" automatically after data writing, therefore, the MPU can write the 8-bit data into the Display Data RAM continuously without any address setting after the start address setting.



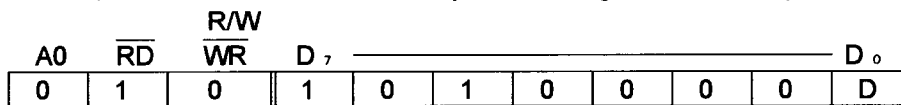
(f) Read Display Data

This instruction reads out the 8-bit data from Display Data RAM addressed by the column and page address. The column address increase "1" automatically after data reading out, therefore, the MPU can read out the 8-bit data from the Display Data RAM without any address setting after the start address setting. One time of dummy read must operate after column address set as the explanation in "(5-5) Access to the Display Data RAM and Internal Register". In the serial interface mode, the display data is not readout.



(g) ADC Select

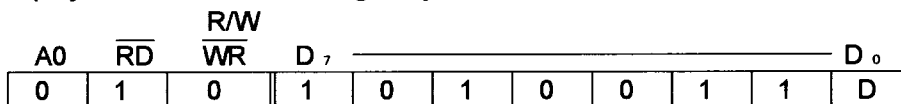
This instruction set the correspondence of column address in the Display Data RAM and segment driver output. (See Fig. 1.) By this instruction, the order of segment output can be changed by the software, and no restriction of the LSI placement against the LCD panel.



D 0: Clockwise Output (Normal)
1: Counterclockwise Output (Inverse)

(h) Normal or Inverse On/Off Set

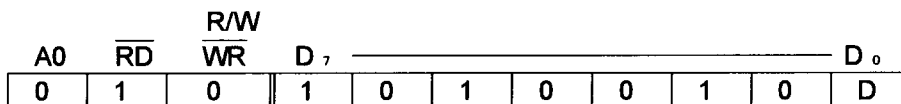
This instruction changes the condition of display turn on and off as normal or inverse. The contents of Display Data RAM is not changed by this instruction execution.



D 0: Normal RAM data "1" correspond to "On"
1: Inverse RAM data "0" correspond to "On"

(i) Whole Display On

This instruction turns on the all pixels independent of the contents of Display Data RAM. In this time, the contents of Display Data RAM is not changed and is kept. This instruction takes over precedence over the "Normal or Inverse On/Off Set Instruction".

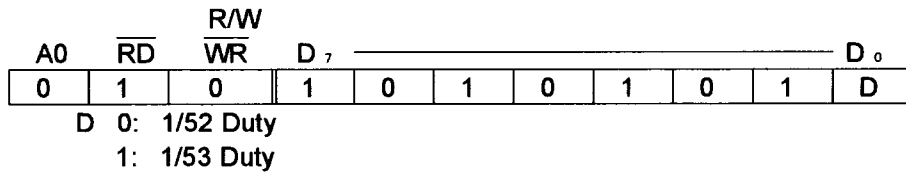


D 0: Normal Display
1: Whole Display turns on

When Whole Display On Instruction is executed in the Display Off status, the internal circuits go to the power save mode (refer to the (s) Power Save).

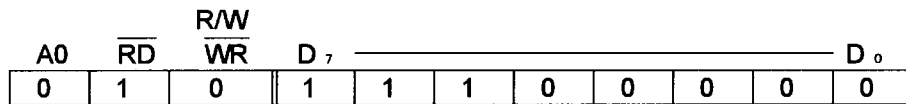
(j) Icon Display

This instruction set the 1/53 duty for the Icon Display. The COM1 terminal operate as COM₅₂ and output the icon display data stored in D₀ of Display Data RAM page 8 (refer to the Fig. 1).



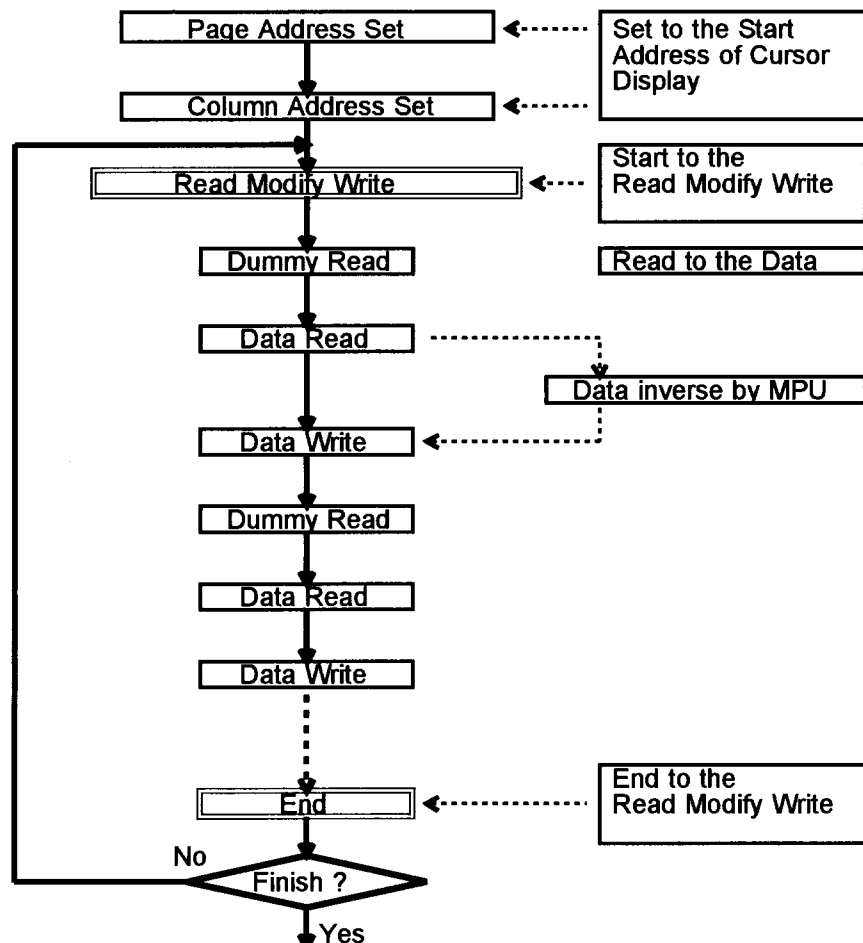
(k) Read Modify Write

This instruction sets the Read Modify Write Mode for the column address increment control. In mode of the Read Modify Write, the column address increases "1" automatically when the Display Data Write Instruction is executed, but the address does not change when the Display Data Read Instruction is executed. This status is continued until End instruction execution. This function reduces the load of MPU for repeating the display data change in the fixed area (ex. cursor blink).



Note) In mode of the Read Modify Write mode, any instructions except for Column Address Set can execute.

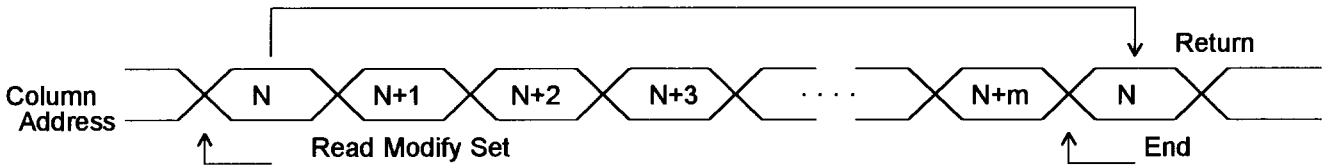
(l) Sequence of inverse display



(m) End

This instruction release the Read Modify Write mode and the column address back to the address where the read modify write mode setting.

A0	\overline{RD}	\overline{WR}	D ₇								D ₀
0	1	0	1	1	1	0	1	1	1	0	



(n) Reset

This instruction executes the following initialization.

Initialization

- ① Set the Address (00)_H into the Column Address Counter.
- ② Set the page "0" into the Page Address Register.
- ③ Select the D3 of the Output Assignment Register to "0".
- ④ Set 0 to the EVR Register to (00)_H.

In this time, there is no influence to the Display Data RAM.

A0	\overline{RD}	\overline{WR}	D ₇								D ₀
0	1	0	1	1	1	0	0	0	1	0	

The reset signal input to the \overline{RES} terminal (hardware reset) must be input for the power on initialization. when the power terns on. Reset Instruction for the reset signal input to the \overline{RES} terminal is not allowed.

(o) Output Assignment Register

This instruction sets the common driver scanning order .

A0	\overline{RD}	\overline{WR}	D ₇								D ₀
0	1	0	1	1	0	0	A3	*	*	*	

(*:Don't Care)

A3: Set the scanning order .(Refer to 1-6)

(p) Internal Power Supply

This instruction set the condition of internal Power Supply On/Off. Step up circuits, Voltage Regulator and Voltage Follower operate at On. To operate the step up circuits, the operation of oscillation circuits must be operating.

A0	\overline{RD}	\overline{WR}	D ₇								D ₀
0	1	0	0	0	1	0	0	1	0	D	

- D 0: Internal Power Supply Off
- 1: Internal Power Supply On

The internal Power Supply must be Off when external power supply using.

(q) LCD Driving Voltage Set

This instruction control LCD driving voltage V1 to V4 and output LCD driving waveform output through the COM/SEG terminals.

A0	RD	WR	R/W	D ₇ ~ D ₀							
0	1	0		1	1	1	0	1	1	0	1

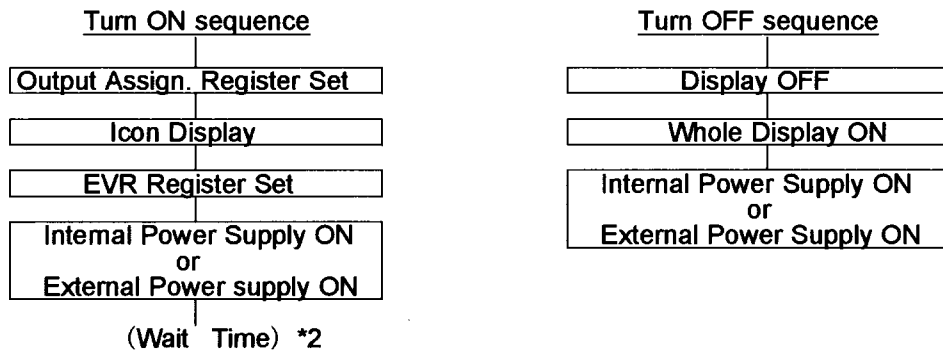
NJU6577S contains operational amplifiers for LCD bias voltage V1 to V4. These amplifiers current are reduced in order to realize low power consumption. Because of this reduction, LCD driving voltage V1 to V4 might be unstable just after the internal power supply is turned on.

LCD Driving Voltage Set instruction is prepared for this unstableness.

● LCD driving power supply ON/OFF sequences

The following sequences are required when the power supply is tuned on/of.

When the power supply is tuned on again after the turn off (by the power save instruction), the power save release sequence (s) is required.

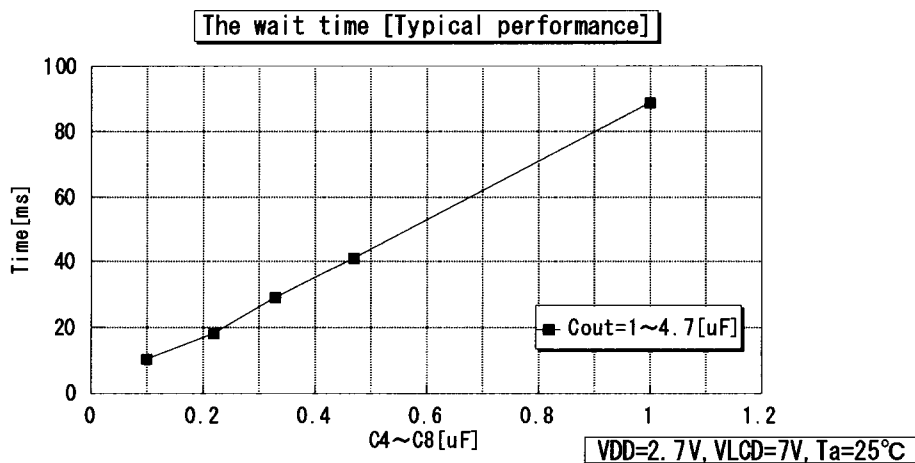


*1 This instruction is required in both cases of the internal and external power supply.

Until "LCD driving voltage Set" execution, NJU6577S operating current is higher than usual state and all COM/ SEG do not output LCD driving waveform output V_{DD} level continuously.

*2 The wait time depends on the C₄, C₅, C₆, C₇, C₈ and C_{OUT} capacitors ((4) (d) Fig.4), V_{DD} and V_{LCD} voltage.

Therefore it requires the actual evaluation using the LCD module to get the correct time. (Refer to the following graph)



(r) EVR Register Set

This instruction controls voltage adjustment circuits of internal LCD power supply and changes LCD driving voltage V₅. Finally, it adjusts the contrast of LCD display. By setting a data into EVR register, V₅ output voltage selects one condition out of 16-voltage conditions. The range of V₅ voltage is adjusted by setting external resistors as mentioned in "(4) (b) Voltage Adjust Circuits."

R/W										
A0	\overline{RD}	\overline{WR}	D ₇							D ₀
0	1	0	1	0	0	0	A3	A2	A1	A0

A4	A3	A2	A1	A0	V _{LCD}
0	0	0	0	0	High
		⋮			⋮
		⋮			⋮
1	1	1	1	1	Low

$$V_{LCD} = V_{DD} - V_5$$

When EVR doesn't use, set the EVR register to (0,0,0,0,0).

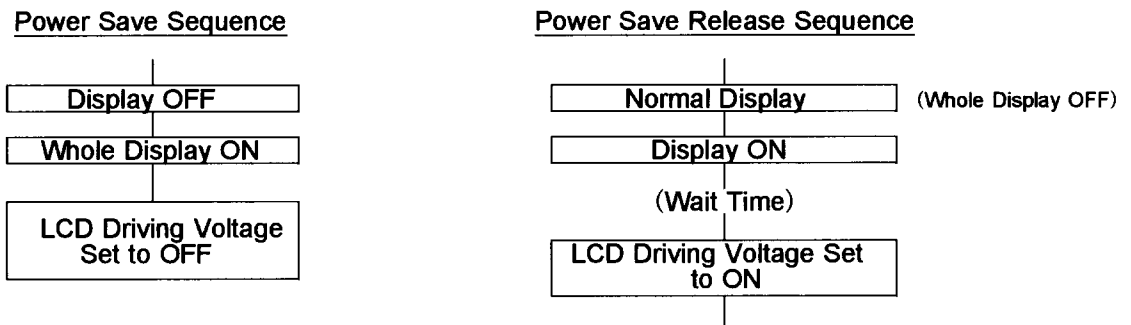
(s) Power Save (Dual Command)

When both of Display Off and Whole Display On are executed, the internal circuit go to the power save mode and the operating current is reduced as same as the stand by current.

The internal status in the Power Save Mode is shown follows;

- ① Stop the Oscillation Circuits and Internal Power Supply Circuits operation.
- ② Stop the LCD driving. Segment and Common drivers output V_{DD} level.
- ③ Keep the display data and operating mode just before the power save mode.
- ④ All of LCD driving bias voltage fix to the V_{DD} level.

The power save and its release should be performed according to the following sequences.

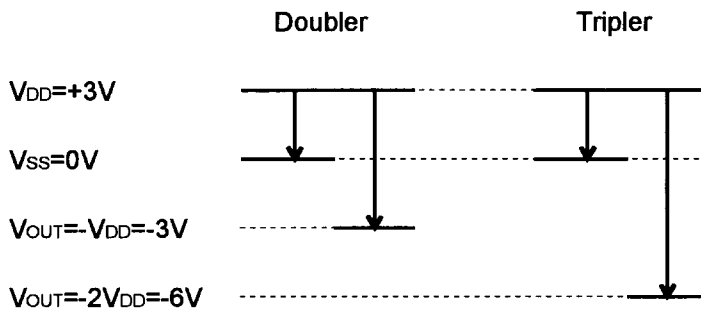


- *1 In the power save sequence, The power save mode is started after the second the instruction "Whole Display ON".
- *2 In the power save release sequence, The power save mode is released after the Normal Display instruction (Whole Display OFF).
- *3 Until "LCD driving voltage set to ON" execution, NJU6577S operating current is higher than usual state and all COM/SEG terminals output V_{DD} level continuously.
- *4 In case of the external power supply for LCD driving, it should be turned off and made condition like as disconnection or connection to V_{DD} before the power save mode or at the same time, In this time, V_{OUT} terminal should be made condition like as unconnection or connection to the lowest voltage of the system. (V₅ level from the external power supply).

(4) Internal Power Supply

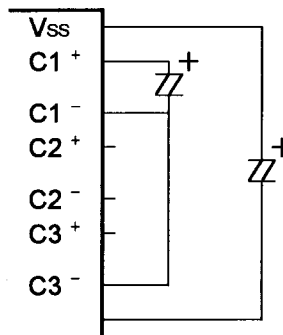
(a) Quadruple voltage step up circuit

Three times negative voltage (V_{DD} common) of the voltage $V_{DD}-V_{SS}$ is output from V_{OUT} terminal when connecting three capacitor between $C1^+$ and $C1^-$, $C2^+$ and $C2^-$, Connect $C2^-$ to $C3^-$ and $C3^+$, should be open. (or connect the capacitor between $C1^+$ and $C1^-$, $C3^+$ and $C3^-$, connect $C2^+$ to $C3^+$, and $C2^-$ should be open.) V_{SS} and V_{OUT} voltage booster circuits like as Voltage Tripler or Doubler using an oscillation circuit output as its clock signal, therefore, the oscillation circuit operation is required when voltage boost operation. The voltage relation regarding the step up circuits is shown in below. When voltage quadrupler operation, the operation voltage V_{DD} should be less than 3.3V.

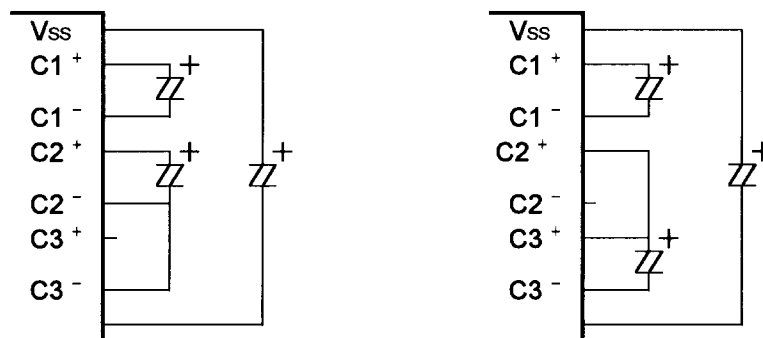


• Examples for connecting the capacitors

2-times voltage



3-times voltage



(b) Voltage Adjust Circuits

The step up voltage of V_{OUT} output from V_5 through the voltage adjust circuits for LCD driving.

The output voltage of V_5 is adjusted by changing the R_a and R_b within the range of $|V_5| < |V_{OUT}|$.

The output voltage is calculated by the following formula.

$$V_{LCD} = V_{DD} - V_5 = (1 + R_b/R_a) \cdot V_{REG} \dots\dots \textcircled{1}$$

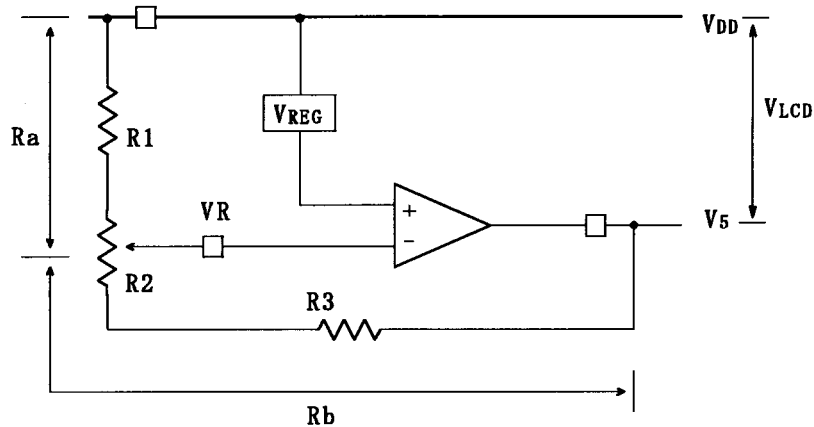


Fig. 3

Where, the V_{REG} is a constant voltage in the NJU6577S like as $V_{REG} = 2.0V$.

To adjust the output voltage from V_5 , connect the variable resistance among VR , V_{DD} and V_5 as shown in Fig. 3. When fine tuning for V_5 is needed, combine with the fixed resistance of R_1 , R_3 and variable resistance of R_2 is recommended as shown in Fig. 3.

[Design example for R_1 , R_2 and R_3 ; $V_{DD} = 3V$ / reference]

- $R_1 + R_2 + R_3 = 5M \Omega$ (Determined by the current flown between $V_{DD} - V_5$)
- Variable voltage range by the R_2 . $-4V \sim -6V$ ($V_{LCD} = V_{DD} - V_5 \rightarrow 7V \sim 9V$)
(Determined by the LCD electrical characteristics)
- R_1 , R_2 and R_3 are calculated by above conditions and the formula of $\textcircled{1}$ to mentioned below;
 - $R_1 = 1.111M \Omega$
 - $R_2 = 0.318M \Omega$
 - $R_3 = 3.571M \Omega$

The voltage adjust circuits has a temperature coefficient against the V_{REG} output. If necessary, please connect the thermistor to the voltage adjust circuits serially.

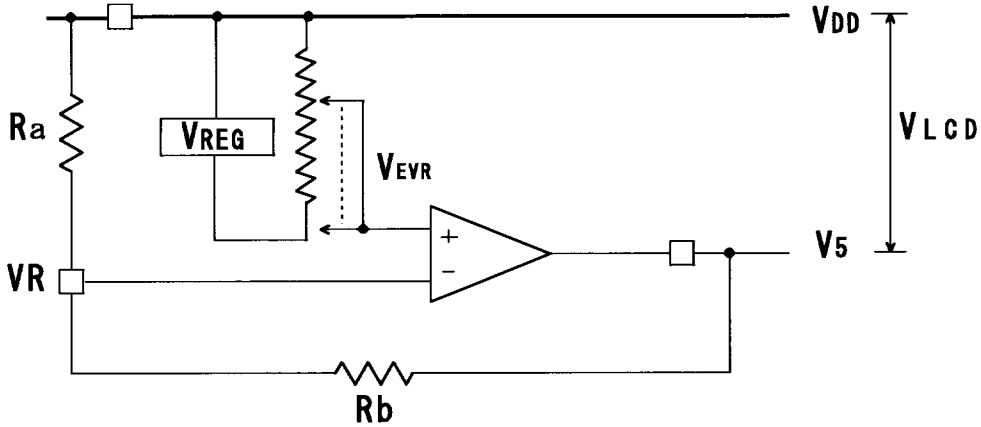
To avoid the noise trouble, short wiring or sealed wiring is required for VR terminal input due to the VR terminal is high impedance.

(c) Contrast Adjustment by using the EVR function

The EVR controls voltage of VREG by instruction and changes voltage of V5.

As result ,LCD display contrast is adjusted by V5.The EVR selects a voltage of VREG in the following 32conditions by setting 6bits data into the EVR register.

In case of EVR operation ,T1 terminal and T2.require to set couples of value as(L,L),(L,H)and(H,L)excepting for (H,H)and the internal power supply must turn on by instruction.



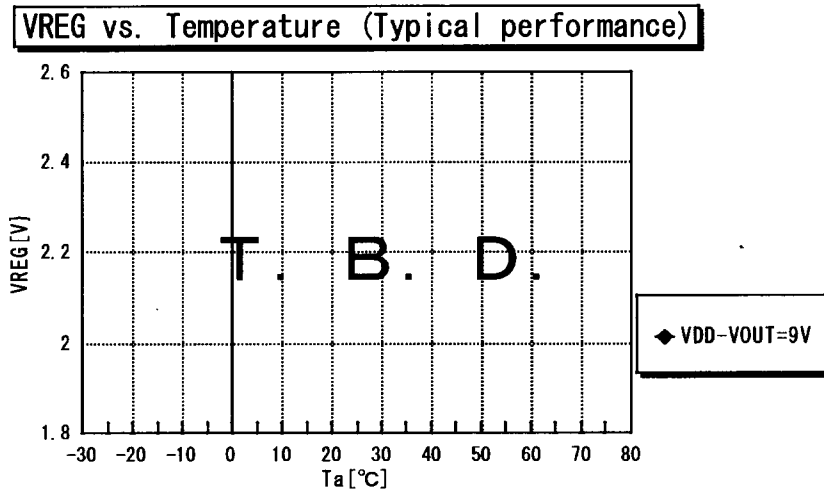
$$V_{LCD} = V_{DD} - V_5 = (1 + R_b/R_a) \cdot V_{EVR} \dots\dots ②$$

$$[: V_{EVR} = V_{REG} - n \cdot (V_{REG}/164)]$$

EVR register		$n \cdot (V_{REG}/164)$	V_{LCD}
(00) _H	(0,0,0,0,0)	$0 \cdot (V_{REG}/164)$	<div style="text-align: center;"> High ↑ ↓ Low </div>
(01) _H	(0,0,0,0,1)	$1 \cdot (V_{REG}/164)$	
(02) _H	(0,0,0,1,0)	$2 \cdot (V_{REG}/164)$	
(03) _H	(0,0,0,1,1)	$3 \cdot (V_{REG}/164)$	
⋮	⋮	⋮	
⋮	⋮	⋮	
(1E) _H	(1,1,1,1,0)	$30 \cdot (V_{REG}/164)$	
(1F) _H	(1,1,1,1,1)	$31 \cdot (V_{REG}/164)$	

When EVR function doesn't use, (D₄, D₃, D₂, D₁, D₀) of EVR register set to (0, 0, 0, 0, 0) by the \overline{RES} signal or "EVR Register Set" instruction.

*) V_{REG} , depends on the voltage between V_{DD} and V_{OUT} , the operating temperature. Please refer to the following graphs.



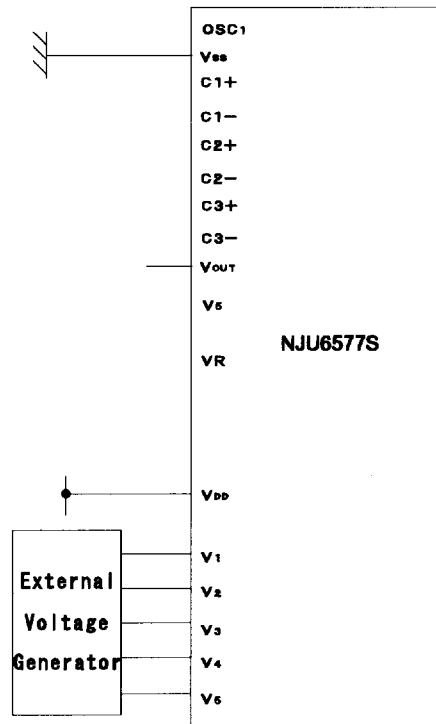
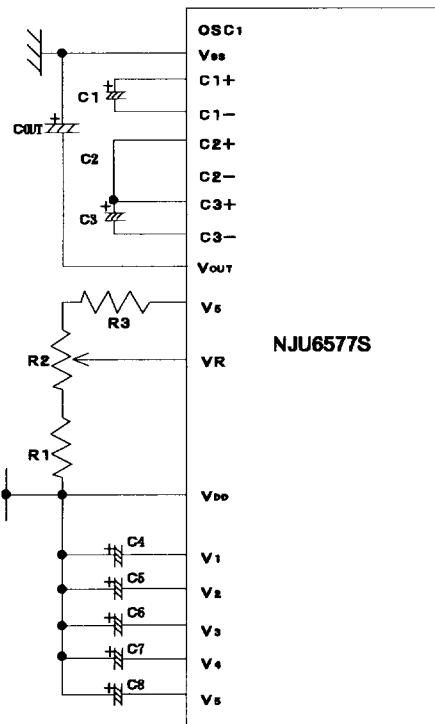
(d) LCD Driving Voltage Generation Circuits

The LCD driving bias voltage of V_1, V_2, V_3, V_4 are generated internally by dividing the V_5 voltage with internal bleeder resistance. And it is supplied to the LCD driving circuits after the impedance conversion with voltage follower circuit.

As shown in Fig. 4, Five capacitors are required for each LCD driving voltage terminal as a voltage stabilizing. And the value of capacitors C4, C5, C6, C7 and C8 are determined depending on the actual LCD panel display evaluation.

Using the internal Power Supply

Using the external Power Supply



Reference set up value
 $V_{LCD} = V_{DD} - V_5 \approx 7 \sim 9V$ Changed

Item	Value
C _{OUT}	4.7 ~ 10 μ F
C ₁ , C ₂ , C ₃	4.7 ~ 10 μ F
C ₄ to C ₈	0.1 ~ 0.47 μ F
R ₁	1.111M Ω
R ₂	0.318M Ω
R ₃	3.571M Ω

Fig. 4

*1 Short wiring or sealed wiring to the VR terminal is required for the VR terminal due to the high impedance of VR terminal.

*2 Following connection of V_{OUT} is required when external power supply using.

When $V_{SS} > V_5$ -- $V_{OUT} = V_5$

When $V_{SS} \leq V_5$ -- $V_{OUT} = V_{SS}$

(5) MPU Interface

(5-1) Interface type selection

NJU6577S interfaces with MPU by using both of 8-bit bi-directional data bus (D_7 to D_0) or serial interface (SI). The 8 bit parallel or serial interface is determined by a condition of the P/S terminal connecting to "H" or "L" level as shown in Table 5. In case of the serial interface, status and RAM data read out operation is impossible.

Table 5

P/S	Type	\overline{CS}	A0	\overline{RD}	\overline{WR}	C86	SI	SCL	$D_0 \sim D_7$
H	Parallel	\overline{CS}	A0	\overline{RD}	\overline{WR}	C86	-	-	$D_0 \sim D_7$
L	Serial	\overline{CS}	A0	-	-	-	SI	SCL	OPEN

(5-2) Parallel Interface

The NJU6577S interfaces both of 68 or 80 type MPU directly when the parallel interface (P/S="H") is selected. 68 type MPU or 80 type MPU is determined by the condition of C86 terminal connecting to "H" or "L" as shown in table 6.

Table 6

C86	Type	\overline{CS}	A0	\overline{RD}	\overline{WR}	$D_0 \sim D_7$
H	68 type MPU	\overline{CS}	A0	E	R/W	$D_0 \sim D_7$
L	80 type MPU	\overline{CS}	A0	\overline{RD}	\overline{WR}	$D_0 \sim D_7$

(5-3) Discrimination of Data Bus Signal

The NJU6577S discriminates the mean of signal on the data bus by the combination of A0, E, R/W, and (\overline{RD} , \overline{WR}) signals as shown in Table 7.

Table 7

Common	68 type		80 type		Function
	A0	R/W	\overline{RD}	\overline{WR}	
1	1	0	1	1	Read Display Data
1	0	1	1	0	Write Display Data
0	1	0	1	1	Status Read
0	0	1	1	0	Write into the Register(Instruction)

(5-4) Serial Interface.(P/S="L")

Serial interface circuits consist of 8 bits shift register and 3 bits counter. SI and SCL input are activated when the chip select terminal \overline{CS} set to "L" and P/S terminal set to "L". The 8 bits shift register and 3 bits counter are reset to the initial condition when the chip is not selected. The data input from SI terminal is MSB first like as the order of D_7, D_6, \dots, D_0 . and the data are entered into the shift register synchronizing with the rise edge of the serial clock SCL. The data in the shift register are converted to parallel data at the 8th serial clock rise edge input. discrimination of the display data or instruction of the serial input data is executed by the condition of A0 at the 8th serial clock rise edge. A0="H" is display data and A0="L" is instruction. When \overline{RES} terminal becomes "L" or \overline{CS} terminal becomes "H" before 8th serial clock rise edge, NJU6577S recognizes them as a instruction data incorrectly. Therefore a unit of serial data must be structured by 8-bit. The time chart for the serial interface is shown in Fig. 5. To avoid the noise trouble, the short wiring is required for the SCL input.

Note) The read out function, such as the status or RAM data read out, is not supported in this serial interface.

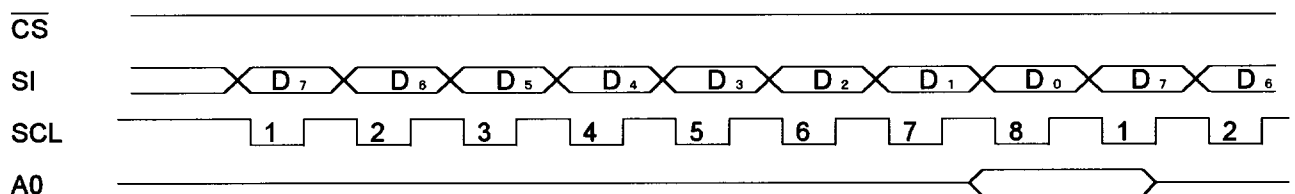


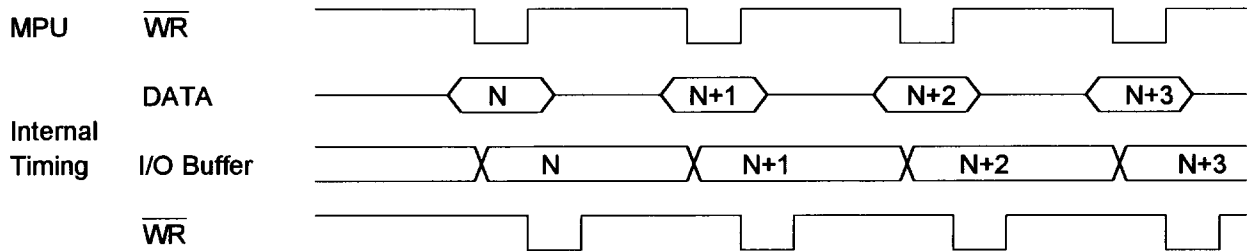
Fig. 5

(5-5) Access to the Display Data RAM and Internal Register.

The NJU6577S is operating as one of pipe-line processor by the bus-holder connecting to the internal data bus to adjust the operation frequency between MPU and the Display Data RAM or Internal Register. For example, When the MPU reads out the data from the Display Data RAM, the data read out in the data read cycle(dummy read) is held in the bus-holder at once then read out from the bus-holder to the system bus at the next data read cycle. When the MPU writes the data into the Display Data RAM, the data is held in the bus-holder, then it is written into the Display Data RAM by the next data write cycle. Therefore high speed data transmission between MPU and NJU6577S is available because of it is not limited by the tACC and tDS as display data RAM access time and is limited by the system cycle time (R) or (W). If the cycle time is not be kept in the MPU operation, NOP should be inserted to system instead of the waiting operation.

Please note that the read out data is a address data when the read out execution just after the address The read out operation does not read the data in the pointed address just after the address set operation. And second read out operation can read out the data correctly from the pointed address. Therefore, one dummy read is required after address setting or write cycle as shown in Fig. 6.

● Write Operation



● Read Operation

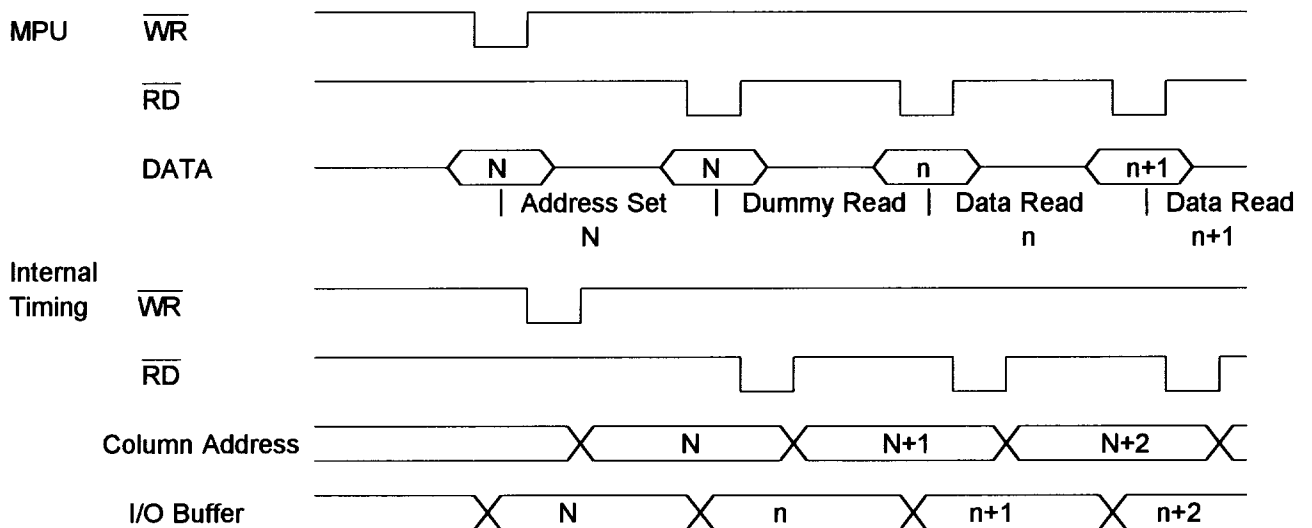


Fig.6

(5-6) Chip Select

\overline{CS} is Chip Select terminal. The Chip Select is executed by the setting of $\overline{CS}="L"$. Only the select mode, the interface with MPU is available. In the non select period, the D_0 to D_7 are high impedance and A_0 , \overline{RD} , \overline{WR} , \overline{SI} and \overline{SCL} input are put on the disable state. If the serial interface is selected in the non select period, the shift register and counter are reset. The reset input is regardless with the condition of \overline{CS} .

ABSOLUTE MAXIMUM RATINGS (Ta=25 °C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (1)	V _{DD}	- 0.3 ~ + 7.0 - 0.3 ~ + 3.3 (used Tripler)	V
Supply Voltage (2)	V ₅	V _{DD} - 10.8 ~ V _{DD} + 0.3	V
Supply Voltage (3)	V ₁ ~ V ₄	V ₅ ~ V _{DD} + 0.3	V
Input Voltage	V _{IN}	- 0.3 ~ V _{DD} + 0.3	V
Operating Temperature	T _{opr}	- 30 ~ + 80	°C
Storage Temperature	T _{stg}	- 55 ~ + 125(Chip) - 55 ~ + 100(TCP)	°C

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 2) All voltage values are specified as V_{SS} = 0 V.

Note 3) The relation : V_{DD} ≥ V₁ ≥ V₂ ≥ V₃ ≥ V₄ ≥ V₅ ; V_{DD} > V_{SS} ≥ V_{OUT} must be maintained.

Note 4) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the voltage converter.

ELECTRICAL CHARACTERISTICS (1) (V_{DD}=3V ± 10%, V_{SS}=0V, Ta=-20 ~ +75 °C)

PARAMETER		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	Note
Operating Voltage(1)	Recommend	V _{DD}			2.7	3.0	3.3	V	5
	Available				2.4		5.5		
Operating Voltage(2)	Recommend	V ₅			V _{DD} - 10		V _{DD} - 3.5	V	
	Available				V _{DD} - 10				
	Available	V ₁ , V ₂	V _{LCD} = V _{DD} - V ₅	V _{DD} - 0.6xV _{LCD}		V _{DD}			
	Available	V ₃ , V ₄		V ₅		V _{DD} - 0.4xV _{LCD}			
Input Voltage	High Level	V _{IHC}	D0, D1...D7, A0, CS, RES, RD, WR, C86, SI, SCL, P/S Terminals	V _{DD} = 2.7V	0.8xV _{DD}		V _{DD}	V	
	Low Level	V _{ILC}			V _{SS}		0.2xV _{DD}		
Output Voltage	High Level	V _{OHC}	D0, D1...D7, Terminals	I _O = -0.5mA	0.8xV _{DD}		V _{DD}	V	
	Low Level	V _{OLC}			V _{SS}		0.2xV _{DD}		
Input Leakage Current		I _{LI}	All input terminals		-1.0		1.0	uA	6
		I _{LO}	All I/O term.(D0...D7)		-3.0		3.0		
Driver On-resistance		R _{ON1}	Ta=25 °C ext. power supply	V _{LCD} = 10V		2.0	3.0	kΩ	7
		R _{ON2}		V _{LCD} = 8.0V		3.0	4.5		
Stand-by Current		I _{DDQ1}	during stand by Mode			0.05	5	uA	8



■ ELECTRICAL CHARACTERISTICS (2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	Note
Operating Current	I _{DD1}	Display	V _{DD} =2.7V, V _{LCD} =8V		20	40	uA	8
	I _{DD2}	Accessing f _{cy} c=200kHz	V _{DD} =2.7V		120	240	uA	9
Input Terminal Capacitance	C _{IN}	A0,CS,RES,RD,WR,C86,SI, SCL,P/S,T1,T2,D ₀ ~D ₇ Ta=25°C			10		pF	
Oscillation Frequency	fosc	Ta=25°C	V _{DD} =3.0V	13.1	16	18.9	kHz	

Voltage Tripler	Input Voltage	V _{DD1}	V _{DD} -V _{SS}	2.4		5.5	V	10	
		V _{DD2}	V _{DD} -V _{SS} , used Tripler	2.4		3.3	V		
	Output Volt.	V _{OUT}	V _{SS} -V _{LCD} ,used Tripler	-6.6			V		
	ON-Resistance	R _{STEP}	V _{DD} =3V, C=4.7uF used Tripler		600	1000	Ω		
	Adjustment range of LCD Driving Volt	V _{OUT}	Tripler Circuit "OFF"	V _{DD} -10		V _{DD} -5.0	V	11	
	Voltage Follower	V ₅	Voltage Adjustment Circuit "OFF"	V _{DD} -10		V _{DD} -5.0	V		
	Operating Current	I _{OUT1}	V _{DD} =3.3V, V _{LCD} =7.4V			80	160	uA	12
		I _{OUT2}	COM/SEG Term. Open, No Access			30	60		
I _{OUT3}		Display check. pattern			25	50			
Voltage Reg.	V _{REG}	V _{DD} =3.0V, Ta=25°C				3.0	%	13	

Note 5) NJU6577S can operate wide operating range, but it is not guarantee immediate voltage changing during the accessing of the MPU.

Note 6) Apply to the High-impedance state of D₀ to D₇ terminals.

Note 7) R_{ON} is the resistance values between power supply terminals(V₁,V₂,V₃,V₄) and each output terminals of common and segment supplied by 0.1V. This is specified within the range of supply voltage (2).

Note 8,9,12) Apply to current after "LCD Driving Voltage Set"

Note 8) Apply to the external display clock operation in no access from the MPU and no use internal power supply circuits.

Note 9) Apply to the condition of cyclic (tcyc) inverted data input continuously in no use internal power supply circuits. The operating current during the accessing is proportionate to the access frequency. In the no accessing period, it is as same as I_{DD1X}.

Note 10) Supply voltage (V_{DD}) range for internal Voltage Tripler operation.

Note 11) LCD driving voltage V₅ can be adjusted within the voltage follower operating range.

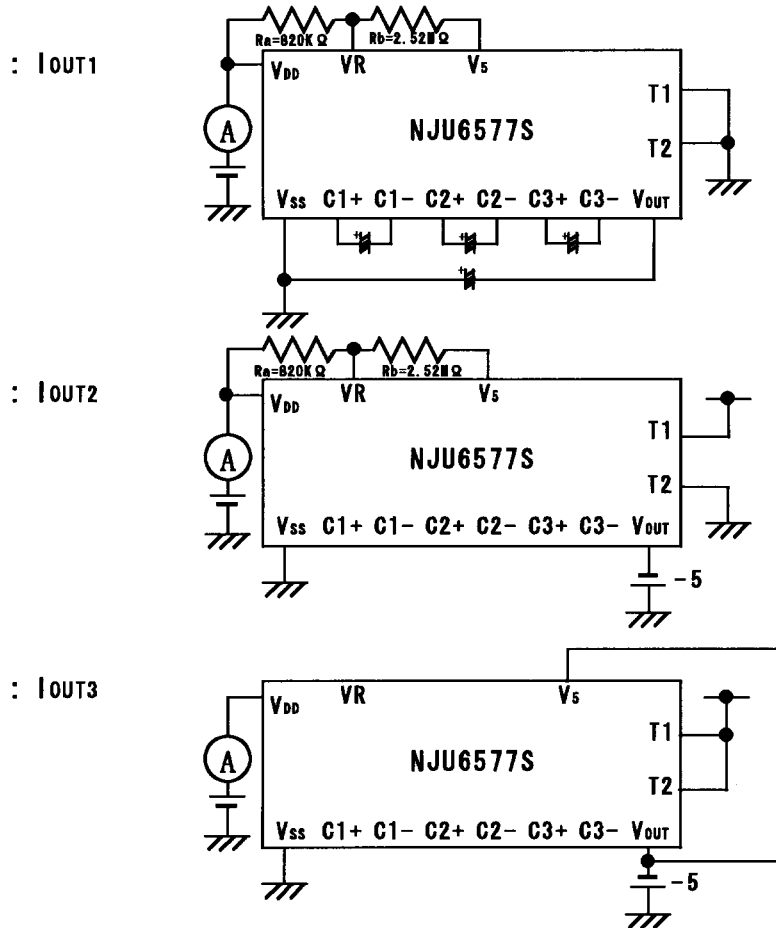
Note 12) Each operating current of voltage supply circuits block is specified under below table conditions. (V_{DD}=3.3V ; V_{LCD}=8V ; COM/SEG Terminals Open ; No Access ; display checkered pattern)

SYMBOL	Status		Operating Condition				External Voltage Supply (Input Terminal)
	T ₁	T ₂	Internal Oscillator	Voltage Tripler	Voltage Adjustment	Voltage Follower	
I _{OUT1}	L	*	Validity	Validity	Validity	Validity	Unuse
I _{OUT2}	H	L	Validity	Invalidity	Validity	Validity	Use(V _{OUT})
I _{OUT3}	H	H	Validity	Invalidity	Invalidity	Validity	Use(V _{OUT} ,V ₅)

* = Don't Care

Note 13) Apply to the precision of the voltage between V_{DD} and V₅ with EVR function.

MEASUREMENT BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (3)

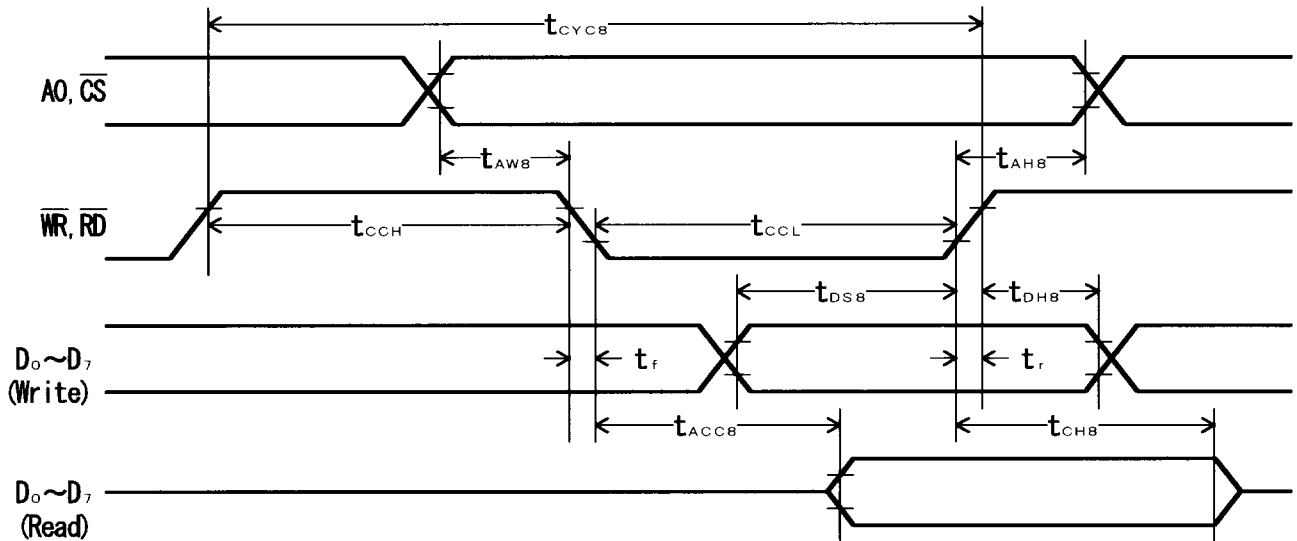
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
Reset time	t_R	$\overline{\text{RES}}$ Terminal	1.0			us	14
Reset "L" Level Pulse Width	t_{RW}	$\overline{\text{RES}}$ Terminal	10			us	15

Note 14) Specified from the rising edge of $\overline{\text{RES}}$ to finish the internal circuit reset.

Note 15) Specified minimum pulse width of $\overline{\text{RES}}$ signal. Over than t_{RW} "L" input should be required for correct reset operation.

BUS TIMING CHARACTERISTICS

• Read/Write operation sequence (80 Type MPU)



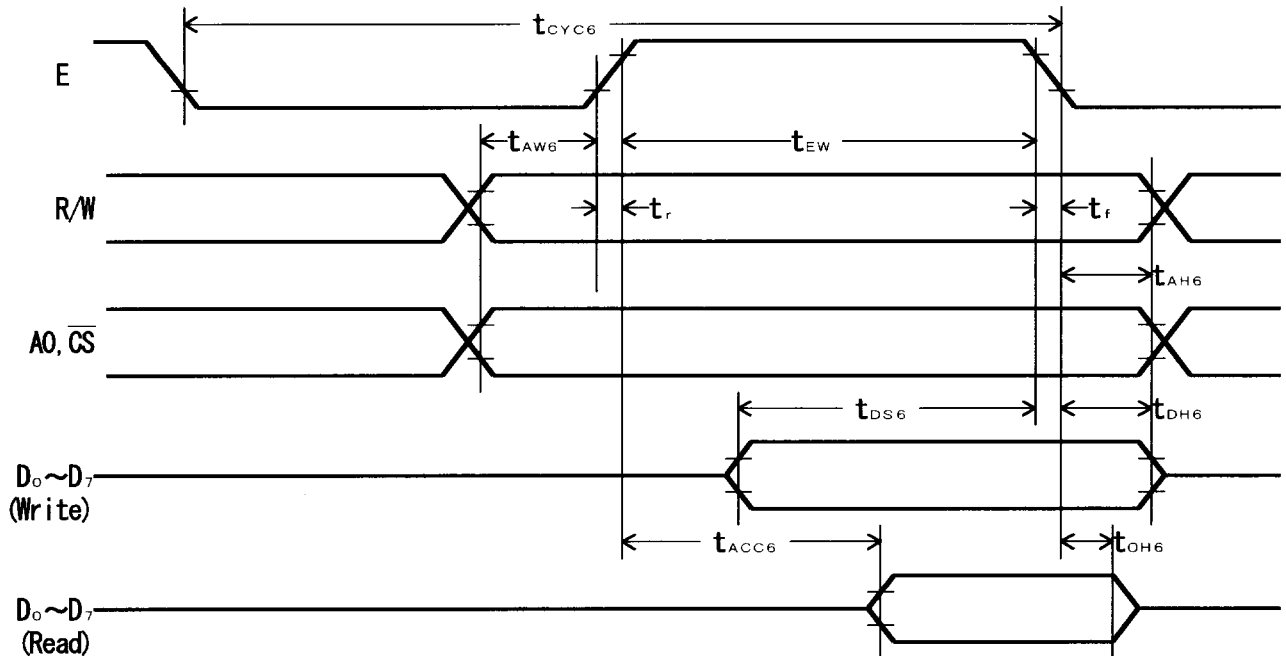
($V_{DD}=3.0V \pm 10\%$, $T_a=-20 \sim 75^\circ C$)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT	
Address Hold Time	A0, \overline{CS}	t_{AHB}	25			ns	
Address Set Up Time	Terminals	t_{AWB}	25				
System Cycle Time	$\overline{WR}, \overline{RD}$	t_{CYCB}	450				
Control Pulse Width	\overline{WR} , "L"	Terminals	$t_{CCL}(W)$	50			
			\overline{RD} , "L"	$t_{CCL}(R)$	200		
			"H"	t_{CCH}	220		
Data Set Up Time	$D_0 \sim D_7$	Terminals	t_{DS8}	120			
Data Hold Time			t_{DH8}	35			
RD Access Time			t_{ACCB}		140		CL=100pF
Output Disable Time	t_{CH8}	0	35				
Rise Time, Fall Time	$\overline{CS}, \overline{WR}, \overline{RD}$ A0, $D_0 \sim D_7$	t_r, t_f		15			

Note 16) Rise time(t_r) and fall time(t_f) of input signal should be less than 15ns.

Note 17) Each timing is specified based on $0.2 \times V_{DD}$ and $0.8 \times V_{DD}$.

• Read/Write operation sequence (68 Type MPU)



($V_{DD}=3.0V \pm 10\%$, $T_a=-20 \sim 75^\circ C$)

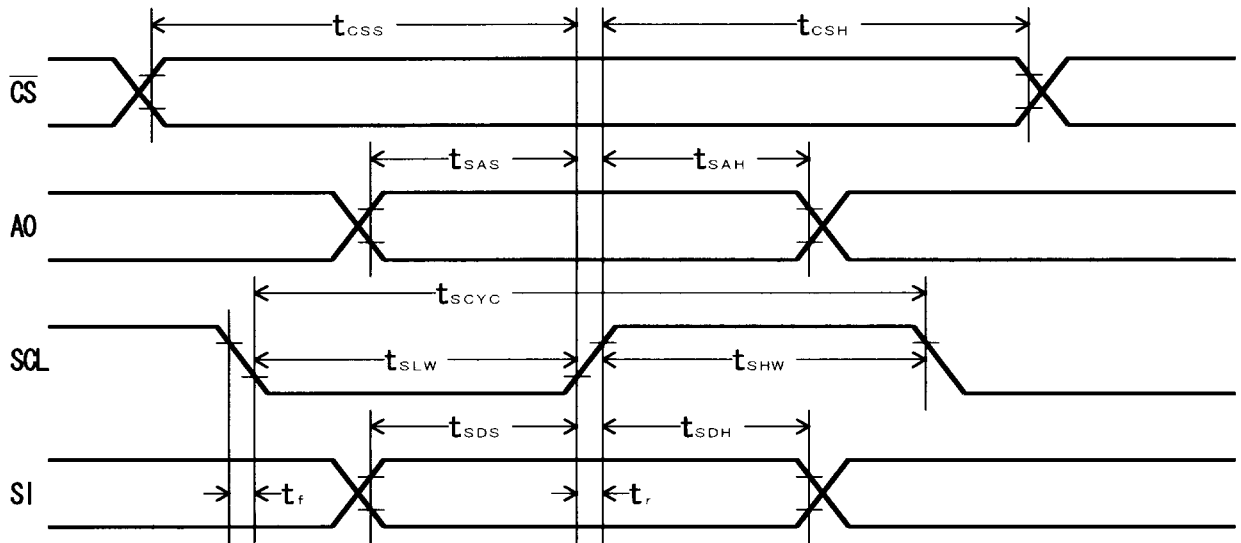
PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time	A0, \overline{CS} , R/W Terminals	t_{AH6}	25		CL=100pF	ns
Address Set Up Time		t_{AW6}	25			
System Cycle Time		t_{CYC6}	450			
Enable Pulse Width	E Terminal	t_{EW}	200			
			50			
Data Set Up Time	D ₀ ~D ₇ Terminals	t_{DS6}	120			
Data Hold Time		t_{DH6}	40			
Access Time		t_{ACC6}		140		
Output Disable Time		t_{OH6}	0	45		
Rise Time, Fall Time	A0, \overline{CS} , R/W E, D ₀ ~D ₇ Terminals	t_r, t_f		15		

Note 18) t_{CYC6} indicates the E signal cycle during the \overline{CS} activation period. The System Cycle Time must be required after \overline{CS} becomes active.

Note 19) Rise time(t_r) and fall time(t_f) of input signal should be less than 15ns.

Note 20) Each timing is specified based on $0.2 \times V_{DD}$ and $0.8 \times V_{DD}$.

• Write operation sequence (Serial Interface)



($V_{DD}=3.0V\pm 10\%$, $T_a=-20\sim 75^\circ C$)

PARAMETER	SYMBOL	MIN	MAX	CONDITION	UNIT
Serial Clock cycle	t_{SCYC}	1000			ns
SCL "H" pulse width	t_{SHW}	300			
SCL "L" pulse width	t_{SLW}	300			
Address Set Up Time	t_{SAS}	250			
Address Hold Time	t_{SAH}	400			
Data Set Up Time	t_{SDS}	250			
Data hold Time	t_{SDH}	100			
\overline{CS} -SCL Time	t_{CSS}	60			
	t_{CSh}	800			
Rise Time, Fall Time	t_r, t_f		15		

Note 21) Rise time(t_r) and fall time(t_f) of input signal should be less than 15ns.

Note 22) Each timing is specified based on $0.2 \times V_{DD}$ and $0.8 \times V_{DD}$.

■ LCD DRIVING WAVEFORM

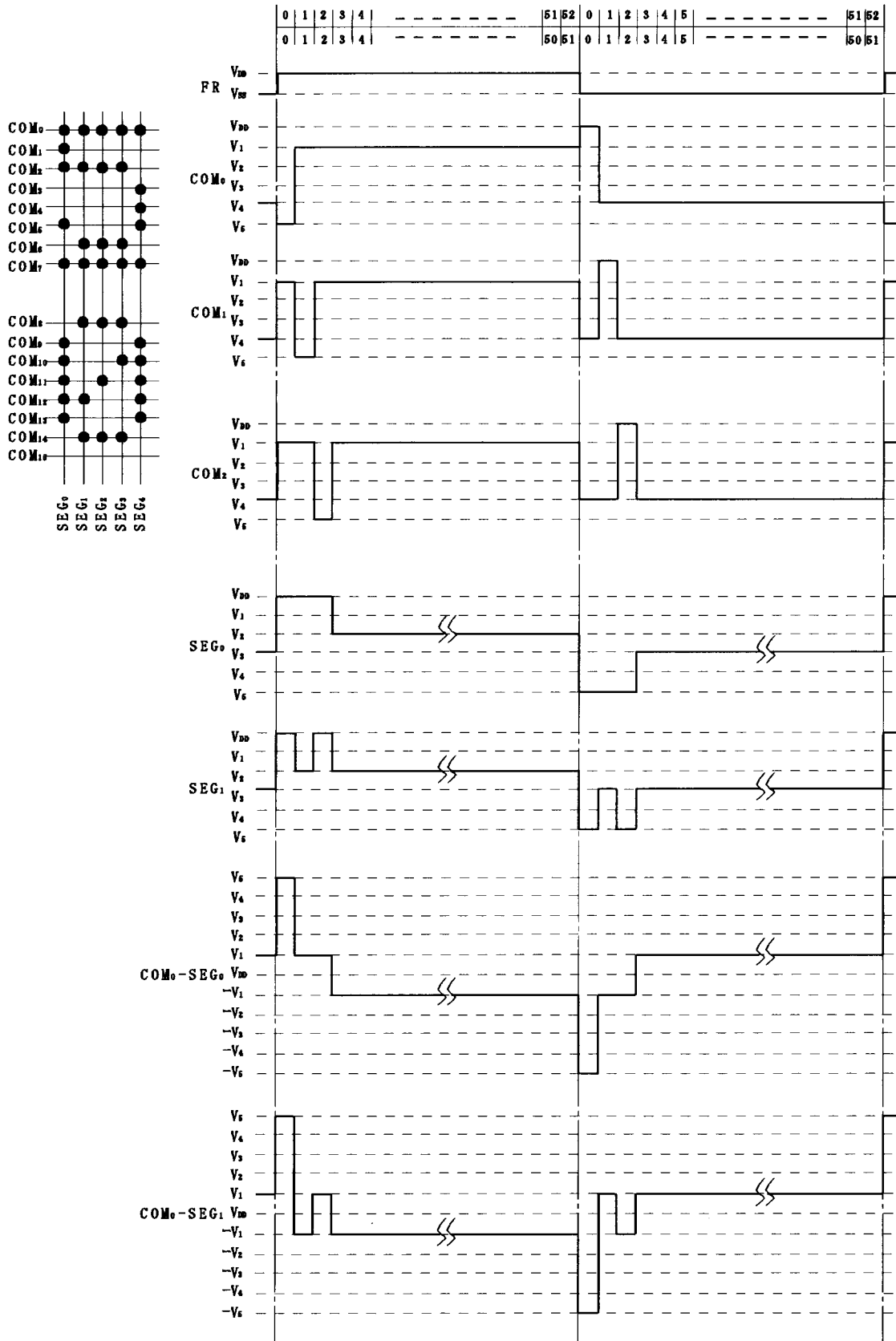


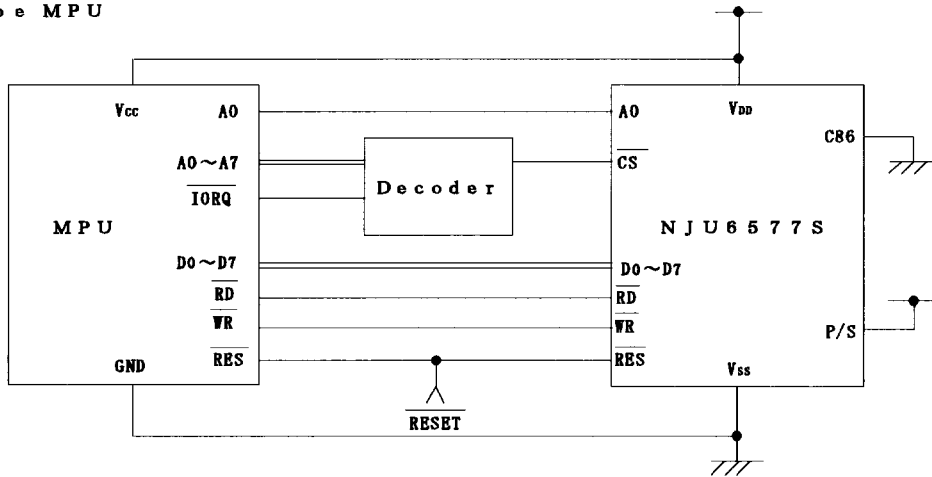
Fig. 7

APPLICATION CIRCUIT

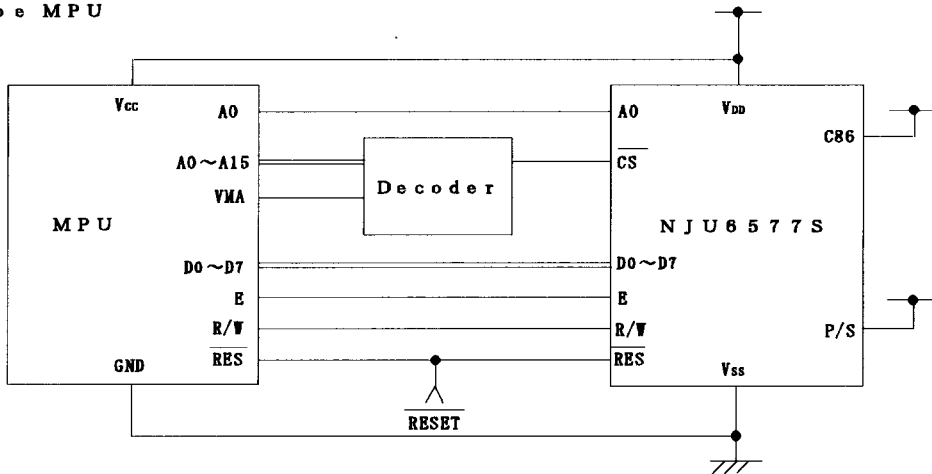
Microprocessor Interface Example

The NJU6577S can interface with both of 80 type and 68 type MPU by the serial format directly. Therefore minimum wiring for the MPU interface is available.

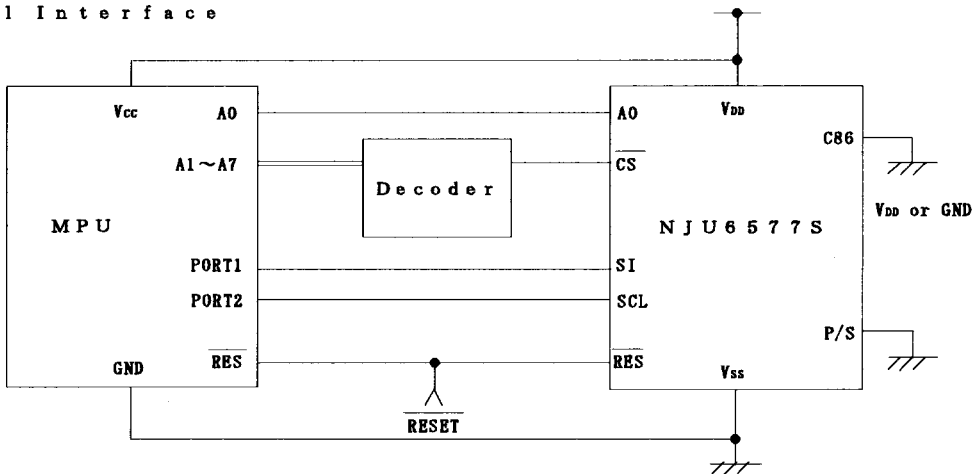
● 80 Type MPU



● 68 Type MPU



● Serial Interface



MEMO

[CAUTION]

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