PRELIMINARY

12-CHARACTER 2-LINE DOT MATRIX LCD CONTROLLER DRIVER

■ GENERAL DESCRIPTION

The NJU6461 is a Dot Matrix LCD controller driver for 12-character 2-line with icon display in single chip.

It contains voltage converter, bleeder resistance, CR oscillator, microprocessor interface circuits, instruction decoder controller, character generator ROM/RAM, high voltage operation common and segment drivers.

The voltage tripler and bleeder resistance generates about triple voltage(8V) and bias voltage for LCD driving waveform internally from single power supply (3V). Consequently, high-contrast display can be performed though the simple power supply circuits.

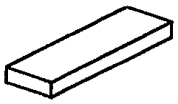
The microprocessor interface circuits which operate by 1MHz, can be selected serial, 4 or 8bit bus.

The character generator consists of 9,600 bits ROM and 32 x 5 bits RAM.

The NJU6461 has two versions regarding the oscillation circuits, version A incorporates C and R, and version B incorporates only C.

The 18-common (16 for character, 2 for icon) and 60-segment drivers are operated up to 13.5V drives 12-character 2-line with 60 icons LCD display.

■ PACKAGE OUTLINE



NJU6461XCH

■ FEATURES

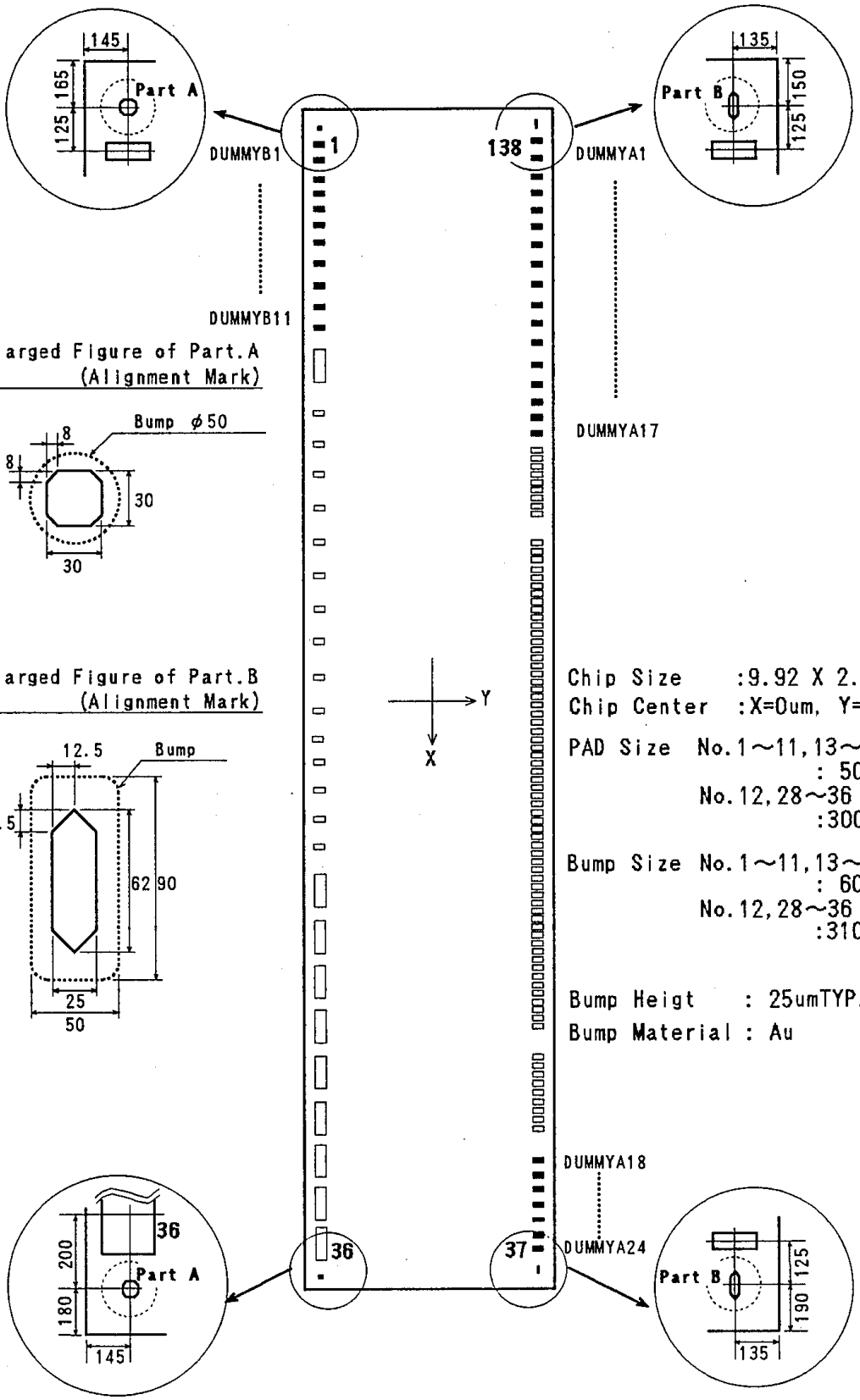
- 12-character 2-line Dot Matrix LCD Controller Driver
- Maximum 60 icon Display (Using COMMK1 and COMMK2)
- Serial, 4 or 8 Bit parallel Direct Interface with Microprocessor
- Display Data RAM - 24 x 8 bits : Maximum 12-character 2-line Display
- Character Generator ROM - 9,600 bits : 240 Characters for 5 x 7 Dots
- Character Generator RAM - 32 x 5 bits : 4 Patterns(5 x 7 Dots)
- High Voltage LCD Driver : 18-common / 60-segment
- Maximum Display Character Number (1/18 Duty):

Device	Display Character	Position of COMMK	Oscillation Circuits	Duty of COMMK
NJU6461AX	12-Character 2-Line + Max.60 Icon Disp.	Upper Side or Lower Side	Internal C and R (Osc Freq.=80kHz)	2/18
NJU6461BX			External R and internal C	2/18
NJU6461CX			Internal C and R (Osc Freq.=80kHz)	1/18
NJU6461DX			External R and internal C	1/18

* When other Oscillation Frequency is required, please use version B and fix the Ext. R

- Useful Instruction Set : Clear Display, Return Home, Display ON/OFF Cont, Cursor ON/OFF Cont, Display Blink, Cursor Shift, Character Shift
- Power On Initialization / Hardware Reset
- Voltage converter and Bleeder Resistance On-chip
- Oscillation Circuit On-chip
- Low Power Consumption
- Operating Voltage --- 2.4 to 3.6 V (Except LCD Driving Voltage)
- Package Outline --- Bumped Chip / TCP
- C-MOS Technology

■ PAD LOCATION



Chip Size : 9.92 X 2.00 mm
Chip Center : X=0um, Y=0um

PAD Size No.1～11,13～27,37～138
: 50um X 90um
No.12,28～36
:300um X 90um

Bump Size No.1～11,13～27,37～138
: 60um X100um
No.12,28～36
:310um X100um

Bump Heigt : 25umTYP.
Bump Material : Au

Unit : um

■ PAD COORDINATES

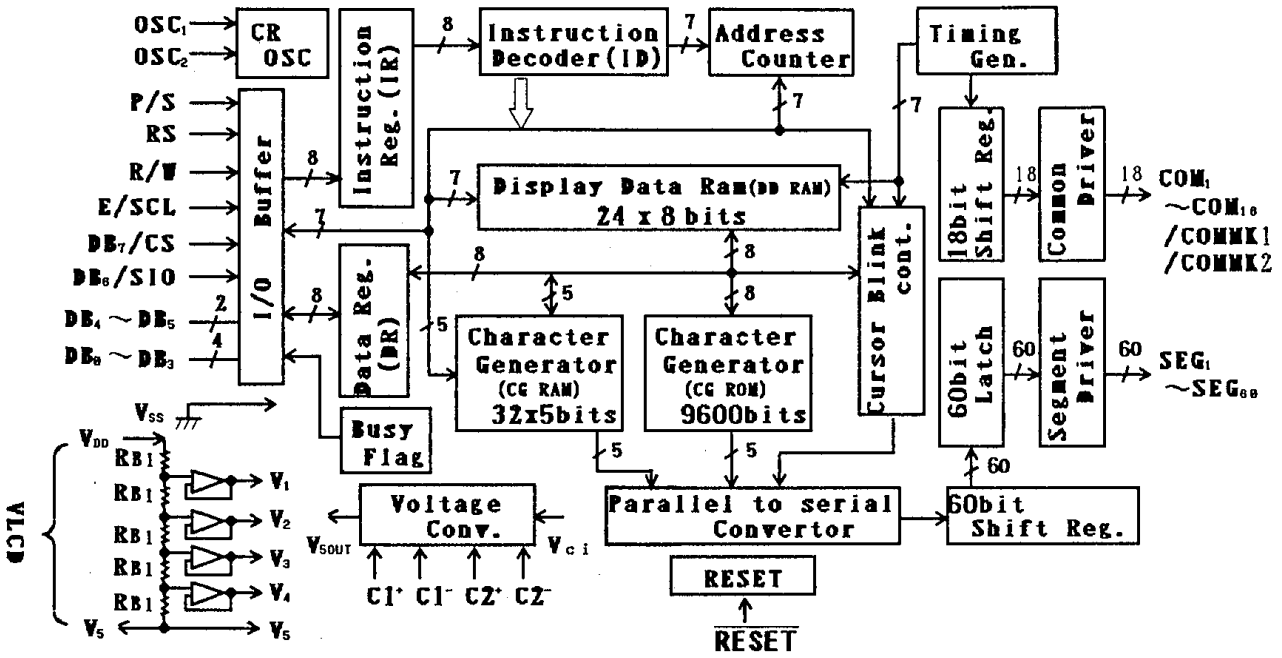
CHIP SIZE 9.92mm x 2.00mm
(CHIP CENTER X=0μm, Y=0μm)

PAD No	PAD NAME	X=(μm)	Y=(μm)
1	$DUMMYB_1$	-4645	- 830
2	$DUMMYB_2$	-4525	- 830
3	$DUMMYB_3$	-4405	- 830
4	$DUMMYB_4$	-4285	- 830
5	$DUMMYB_5$	-4165	- 830
6	$DUMMYB_6$	-4045	- 830
7	$DUMMYB_7$	-3925	- 830
8	$DUMMYB_8$	-3805	- 830
9	$DUMMYB_9$	-3685	- 830
10	$DUMMYB_{10}$	-3565	- 830
11	$DUMMYB_{11}$	-3445	- 830
12	V_{SS}	-3125	- 830
13	DB_7/CS	-2805	- 830
14	DB_6/SIO	-2485	- 830
15	DB_5	-2165	- 830
16	DB_4	-1845	- 830
17	DB_3	-1525	- 830
18	DB_2	-1205	- 830
19	DB_1	- 885	- 830
20	DB_0	- 565	- 830
21	E/SCL	- 245	- 830
22	R/W	75	- 830
23	RS	395	- 830
24	P/S	715	- 830
25	RESET	1035	- 830
26	OSC_2	1355	- 830
27	OSC_1	1675	- 830
28	V_{DD}	1995	- 830
29	V_{CI}	2315	- 830
30	$C1^+$	2635	- 830
31	$C1^-$	2955	- 830
32	$C2^+$	3275	- 830
33	$C2^-$	3595	- 830
34	V_{5OUT}	3915	- 830
35	V_{SS}	4235	- 830
36	V_5	4555	- 830
37	$DUMMYA_{24}$	4620	840
38	$DUMMYA_{23}$	4500	840
39	$DUMMYA_{22}$	4380	840
40	$DUMMYA_{21}$	4260	840
41	$DUMMYA_{20}$	4140	840
42	$DUMMYA_{19}$	4020	840
43	$DUMMYA_{18}$	3900	840
44	$COMMK_1$	3780	840
45	COM_1	3700	840
46	COM_2	3620	840
47	COM_3	3540	840
48	COM_4	3460	840
49	COM_5	3380	840
50	COM_6	3300	840

PAD No	PAD NAME	X=(μm)	Y=(μm)
51	COM_7	3220	840
52	COM_8	3140	840
53	SEG_1	2900	840
54	SEG_2	2820	840
55	SEG_3	2740	840
56	SEG_4	2660	840
57	SEG_5	2580	840
58	SEG_6	2500	840
59	SEG_7	2420	840
60	SEG_8	2340	840
61	SEG_9	2260	840
62	SEG_{10}	2180	840
63	SEG_{11}	2100	840
64	SEG_{12}	2020	840
65	SEG_{13}	1940	840
66	SEG_{14}	1860	840
67	SEG_{15}	1780	840
68	SEG_{16}	1700	840
69	SEG_{17}	1620	840
70	SEG_{18}	1540	840
71	SEG_{19}	1460	840
72	SEG_{20}	1380	840
73	SEG_{21}	1300	840
74	SEG_{22}	1220	840
75	SEG_{23}	1140	840
76	SEG_{24}	1060	840
77	SEG_{25}	980	840
78	SEG_{26}	900	840
79	SEG_{27}	820	840
80	SEG_{28}	740	840
81	SEG_{29}	660	840
82	SEG_{30}	580	840
83	SEG_{31}	500	840
84	SEG_{32}	420	840
85	SEG_{33}	340	840
86	SEG_{34}	260	840
87	SEG_{35}	180	840
88	SEG_{36}	100	840
89	SEG_{37}	20	840
90	SEG_{38}	- 60	840
91	SEG_{39}	- 140	840
92	SEG_{40}	- 220	840
93	SEG_{41}	- 300	840
94	SEG_{42}	- 380	840
95	SEG_{43}	- 460	840
96	SEG_{44}	- 540	840
97	SEG_{45}	- 620	840
98	SEG_{46}	- 700	840
99	SEG_{47}	- 780	840
100	SEG_{48}	- 860	840

PAD No	PAD NAME	X=(μm)	Y=(μm)
101	SEG_{49}	- 940	840
102	SEG_{50}	-1020	840
103	SEG_{51}	-1100	840
104	SEG_{52}	-1180	840
105	SEG_{53}	-1260	840
106	SEG_{54}	-1340	840
107	SEG_{55}	-1420	840
108	SEG_{56}	-1500	840
109	SEG_{57}	-1580	840
110	SEG_{58}	-1660	840
111	SEG_{59}	-1740	840
112	SEG_{60}	-1820	840
113	$COMMK_2$	-1980	840
114	COM_{16}	-2060	840
115	COM_{15}	-2140	840
116	COM_{14}	-2220	840
117	COM_{13}	-2300	840
118	COM_{12}	-2380	840
119	COM_{11}	-2460	840
120	COM_{10}	-2540	840
121	COM_9	-2620	840
122	$DUMMYA_{17}$	-2740	840
123	$DUMMYA_{16}$	-2860	840
124	$DUMMYA_{15}$	-2980	840
125	$DUMMYA_{14}$	-3100	840
126	$DUMMYA_{13}$	-3220	840
127	$DUMMYA_{12}$	-3340	840
128	$DUMMYA_{11}$	-3460	840
129	$DUMMYA_{10}$	-3580	840
130	$DUMMYA_9$	-3700	840
131	$DUMMYA_8$	-3820	840
132	$DUMMYA_7$	-3940	840
133	$DUMMYA_6$	-4060	840
134	$DUMMYA_5$	-4180	840
135	$DUMMYA_4$	-4300	840
136	$DUMMYA_3$	-4420	840
137	$DUMMYA_2$	-4540	840
138	$DUMMYA_1$	-4660	840

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

PAD NO.	SYMBOL	I/O	F U N C T I O N
28	V_{DD}		Power Source (+ 3V)
12	V_{SS}		Power Source (0V)
36	V_5		LCD Driving Voltage Output An alignment pattern is placed beside this terminal.
27 26	OSC_1 OSC_2	I	Version A -Oscillation Frequency Adjust Terminals. Normally Open For external clock operation, the clock should be input on OSC_1. Version B -Connect the External Resistance.
24	P/S	I	Parallel or serial Interface select input Terminal. "0" : Serial Interface, "1" : Parallel Interface
23	RS	I	Register selection signal input Terminal. (Pull-up) "0" : Instruction Register (Writing) Busy Flag, Address Counter (Reading) "1" : Data Register (Writing/Reading)
22	R/W	I	Read/Write selection signal input Terminal.(Pull-up) "0" : Write , "1" : Read
21	E	I	Read/Write activation signal input in Parallel input mode.
	SCL	I	Shift Clock Input in Serial input mode.
13	DB_7	I/O	3-state Data Bus for Upper bit to transfer the data between MPU and NJU6461 in Parallel operation mode. DB_7 is also used for the Busy Flag reading in Parallel op. mode.
	CS	I	Chip select signal input in Serial operation mode.
14	DB_6	I/O	3-state Data Bus for Upper bit to transfer the data between MPU and NJU6461 in Parallel operation mode.
	SIO	I/O	Serial data I/O in Serial operation mode.
15 16	DB_5 DB_4	I/O	3-state Data Bus for Upper bit to transfer the data between MPU and NJU6461 in Parallel operation mode. When the Serial operation mode, these terminal should be open.
17~20	DB_3~DB_0	I/O	3-state Data Bus for Lower bit to transfer the data between MPU and NJU6461 in Parallel operation mode. These bus are not used in the Serial and 4-bit operation (open).
45~52 121~114	COM 1~COM 8 COM 9~COM_{16}	O	LCD Common Driving Signal output terminals.
44 113	COMMK1 COMMK2	O	Icon Common Driving Signal output terminals.
53~112	SEG 1~SEG_{60}	O	LCD Segment Driving Signal output terminals.
30,31 32,33	C_1^+, C_1^- C_2^+, C_2^-	I/O	Step up Capacitor Connecting Terminals. Connect the step up capacitor between C_1^+ and C_1^- , C_2^+ and C_2^- respectively.
29	V_{ci}	I	Input Terminal for Voltage converter. (Normally $V_{ci} = V_{DD}$)
34	V_{5OUT}	O	Step up voltage Output Terminal.
25	$\overline{RESET}$	I	Reset Terminal. When the "L" level input over then 1.2ms to this terminal, the system will be reset(f_{OSC}=80kHz)
2~11 137~122 43~38	$DUMMYB_2$~ $DUMMYB_{11}$ $DUMMYA_2$~ $DUMMYA_{23}$		DUMMY Terminals. These terminals are electrically open.
1 138 37	$DUMMYB_1$ $DUMMYA_1$ $DUMMYA_{24}$		DUMMY Terminals. These terminals are electrically open and an alignment pattern is placed beside each terminal.

5

■ FUNCTIONAL DESCRIPTION

(1) Description for each blocks

(1−1) Register

The NJU6461 incorporates two 8-bit registers, an Instruction Register (IR) and a Data Register(DR). The Register(IR) stores instruction codes such as "Clear Display" and "Cursor Shift", and address data for Display Data RAM(DD RAM) and Character Generator RAM(CG RAM).

The MPU can write the instruction code and address data to the Register(IR), but it cannot read out from the Register(IR).

The Register(DR) is a temporary stored register, the data stored in the Register(DR) is written into the DD RAM or CG RAM and read out from the DD RAM or CG RAM.

The data in the Register(DR) written by the MPU is transferred automatically to the DD RAM or CG RAM by internal operation.

When the address data for the DD RAM or CG RAM is written into the Register(IR), the addressed data in the DD RAM or CG RAM is transferred to the Register(DR). By the MPU read out the data in the Register(DR), the data transmitting process is performed completely.

After reading the data in the Register(DR) by the MPU, the next address data in the DD RAM or CG RAM is transferred automatically to the Register(DR) to provide for the next MPU reading.

These two registers are selected by the selection signal RS as shown below.

Table 1. shows register operation controlled by RS and R/W signals.

Table 1. Register Operation

RS	R/W	Selected Register	Operation
0	0	IR	Write
0	1		Read busy flag(DB_7) and address counter(DB_0～DB_6)
1	0	DR	Write (Register(DR) to DD RAM or CG RAM)
1	1		Read (DD RAM or CG RAM to Register(DR))

(1−2) Busy Flag (BF)

When the internal circuits are in the operation mode, the busy flag (BF) is "1", and any instruction reading is inhibited.

The busy flag (BF) is output at DB_7 when RS="0" and R/W="1" as shown in Table 1.

The next instruction should be written after the busy flag(BF) goes to "0".

(1−3) Address Counter (AC)

The address counter(AC) addressing the DD RAM and CG RAM.

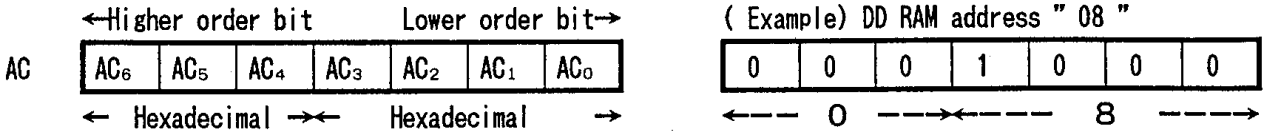
When the address setting instruction is written into the Register(IR), the address information is transferred from Register(IR) to the Counter(AC). The selection of either the DD RAM or CG RAM is also determined by this instruction.

After writing (or reading) the display data to (or from) the DD RAM or CG RAM, the Counter (AC) increments (or decrements) automatically.

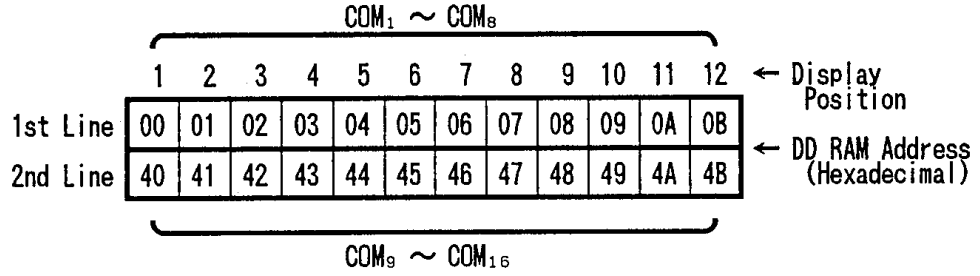
The address data in the Counter(AC) is output from DB_6～DB_0 when RS="0" and R/W="1" as shown in Table 1.

(1−4) Display Data RAM (DD RAM)

The display data RAM (DD RAM) consists of 24 x 8 bits stores up to 24-character display data represented in 8-bit code.
The DD RAM address data set in the address counter(AC) is represented in Hexadecimal.



The relation between DD RAM address and display position on the LCD is shown below.



Note : In the 2 lines display mode, the 1st and 2nd line address are defined as $(00)_H$ to $(0B)_H$ and $(40)_H$ to $(4B)_H$. Please note that the end of 1st line address and the beginning of 2nd line address are not consecutive.

When the display shift is performed, the DD RAM address changes as follows:

(Left Shift Display)

	1	2	3	4	5	6	7	8	9	10	11	12
(00)←	01	02	03	04	05	06	07	08	09	0A	0B	00
(40)←	41	42	43	44	45	46	47	48	49	4A	4B	40

(Right Shift Display)

1	2	3	4	5	6	7	8	9	10	11	12	
0B	00	01	02	03	04	05	06	07	08	09	0A	→(0B)
4B	40	41	42	43	44	45	46	47	48	49	4A	→(4B)

(1−5) Character Generator ROM (CG ROM)

The Character Generator ROM (CG ROM) generates 5 x 7 dots character pattern represented in 8-bit character codes.
The storage capacity is up to 240 kinds of 5 x 7 dots character pattern.
The correspondence between character code and standard character pattern of NJU6461 is shown in Table 2-1.
User-defined character patterns (Custom Font) are also available by mask option.

Table 2-1. CG ROM Character Pattern (ROM version -02)

Lower 4-bit (Hexadecimal)	Upper 4-bit (Hexadecimal) 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM (01)															
1	(02)															
2	(03)															
3	(04)															
4	(01)															
5	(02)															
6	(03)															
7	(04)															
8	(01)															
9	(02)															
A	(03)															
B	(04)															
C	(01)															
D	(02)															
E	(03)															
F	(04)															

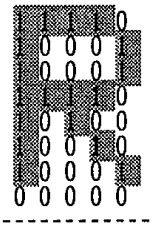
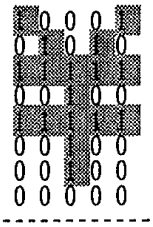
(1－6) Character Generator RAM (CG RAM)

The character generator RAM (CG RAM) can store any kind of character pattern in 5 x 7 dots written by the user program to display user's original character pattern and icon data. The CG RAM can store 4 kind of character in 5 x 7 dots mode or 2 kind of character in 5 x 7 dots mode and icon data.

To display user's original character pattern stored in the CG RAM, the address data $(00)_H$ - $(03)_H$ should be written to the DD RAM as shown in Table 2-1.

Table 3. show the correspondence among the character pattern, CG RAM address and Data.

Table 3. Correspondence of CG RAM address, DD RAM character code and CG RAM character pattern(5 x 7 dots).

Character Code (DD RAM Data)	CG RAM Address	Character Pattern (CG RAM Data)	
7 6 5 4 3 2 1 0 ←— —→ Upper bit Lower bit	4 3 ←— —→ Upper bit	2 1 0 ←— —→ Lower bit	4 3 2 1 0 ←— —→ Upper bit Lower bit
0 0 0 0 * * 0 0	0 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	 Character Pattern Example(1) ←Cursor Position
0 0 0 0 * * 0 1	0 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	 Character Pattern Example(2) ←Cursor Position
		0 0 0 0 0 1	
0 0 0 0 * * 1 1	1 1	1 0 0 1 0 1 1 1 0 1 1 1	* : Don't Care

Notes : 1. Character code bit 0, 1 correspond to the CG RAM address 3, 4(2bits:4 patterns).
2. CG RAM address 0 to 2 designate character pattern line position. The 8th line is the cursor position and the display is performed by logical OR with cursor. Therefore, in case of the cursor display, the 8th line should be "0". If there is "1" in the 8th line, the bit "1" is always displayed on the cursor position regardless of cursor existence.
3. Character pattern row position correspond to the CG RAM data bits 0 to 4 are shown above.
4. CG RAM character patterns are selected when character code bits 4 to 7 are all "0" and it is addressed by character code bits 0 and 1. Therefore, the address $(00)_H$, $(04)_H$, $(08)_H$ and $(0C)_H$ select the same character pattern as shown in Table 2-1.
5. "1" for CG RAM data corresponds to display On and "0" to display Off.
6. CG RAM address $(14)_H$ to $(1F)_H$ are using for both of character pattern memory and icon data memory.

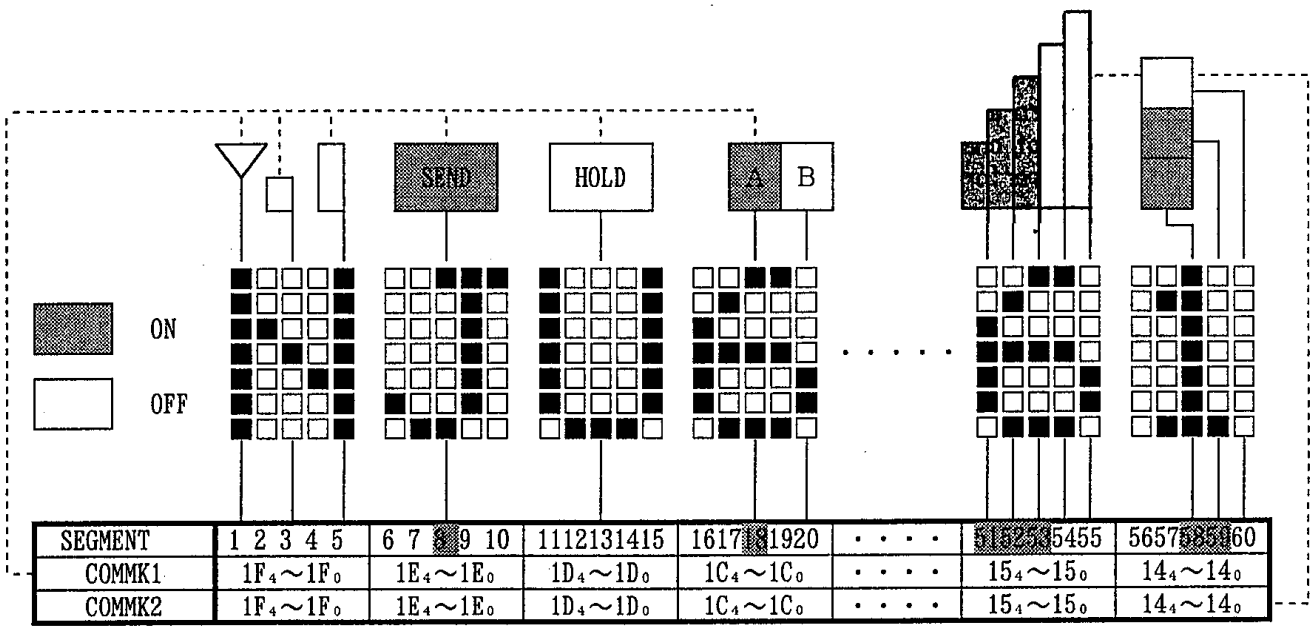
(1－7) Icon Display Function

The NJU6461 can display not only 5 x 7 bits character pattern but also maximum 60 icons.

The icon can display by writing bit "1" to each data bit 0 to 4 in the address $(14)_H$ ~ $(1F)_H$ of CG RAM.

The fixed character display code is not affected except CG RAM writing and display ON/OFF instruction.

The relation between CG RAM address and icon display position on the LCD is fixed even if the display shift is executed. The relation is shown below:



SEGMENT	1 2 3 4 5	6 7 8 9 10	1112131415	1617181920	・・・・	5152535455	5657585960
COMMK1	$1F_4$~$1F_0$	$1E_4$~$1E_0$	$1D_4$~$1D_0$	$1C_4$~$1C_0$	・・・・	15_4~15_0	14_4~14_0
COMMK2	$1F_4$~$1F_0$	$1E_4$~$1E_0$	$1D_4$~$1D_0$	$1C_4$~$1C_0$	・・・・	15_4~15_0	14_4~14_0

NOTE) The $1F_4$ corresponds bit 4 of $(1F)_H$ in CG RAM.

< CG RAM vs. SEG terminal for icon display >

CG RAM address	data 43210	SEG terminal
14	00110	56~60
15	11100	51~55
16	.....	46~50
17	.....	41~45
18	.....	36~40
19	.....	31~35
1A	.....	26~30
1B	.....	21~25
1C	00100	16~20
1D	00000	11~15
1E	00100	6~10
1F	00000	1~5

Maximum Character Number and Icon Display Number in CG RAM

Icon Disp. Number	Max. Chara Number	Note
No Use	4 Chara.	The CG RAM can store 4 kind of Character
40 Icons	3 Chara.	$(03)_H$,$(07)_H$,$(0B)_H$ and $(0F)_H$ can not use for Character Memory.
60 Icons	2 Chara.	$(02)_H$,$(03)_H$,$(06)_H$,$(07)_H$,$(0A)_H$,$(0B)_H$,$(0E)_H$ and $(0F)_H$ can not use for Character Memory.

NOTE) When the icon display function using, the system should be initialized by the software initialization because of the CG RAM does not initialize except the software initialization.

(1−8) Timing Generator

The timing generator generates a timing signals for the DD RAM, CG RAM, CG ROM and other internal circuits.

RAM read timing for the display and internal operation timing for MPU access are separately generated, so that they may not interfere with each other.

Therefore, when the data write to the DD RAM for example, there will be no undesirable influence, such as flickering, in areas other than the display area.

(1−9) LCD Driver

LCD driver consist of 18-common driver and 60-segment driver.

When the line number is selected by a program, the required common drivers output the common driving waveform and the other common drivers output non-selection waveform automatically.

The 60 bits of character pattern data are shifted in the shift-register and latched when the 60 bits shift performed completely. This latched data controls display driver to output LCD driving waveform.

(1−10) Cursor Blinking Control Circuit

This circuits controls cursor On/Off and the cursor position character blinks.

The cursor or blinks appear in the digit residing at the DD RAM address set in the address counter (AC).

When the address counter is $(08)_H$, a cursor position is shown as follows:

	AC_6	AC_5	AC_4	AC_3	AC_2	AC_1	AC_0
(AC)	0	0	0	1	0	0	0

1	2	3	4	5	6	7	8	9	10	11	12	← Display position
00	01	02	03	04	05	06	07	08	09	0A	0B	← DD RAM address (Hexadecimal)
40	41	42	43	44	45	46	47		49	4A	4B	

Cursor position

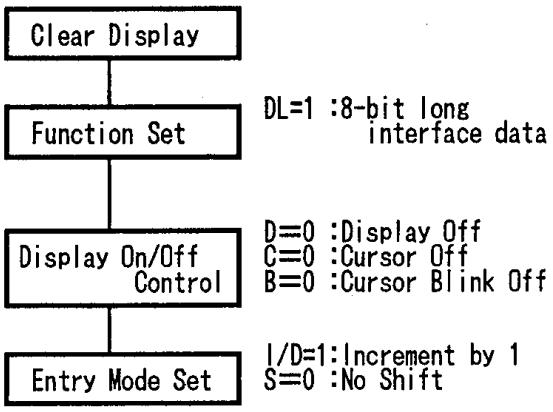
(Note) The cursor or blinks also appear when the address counter (AC) selects the CG RAM. But the displayed cursor and blink are meaningless.
If the AC storing the CG RAM address data, the cursor and blink are displayed in the meaningless position.

(2) Power on Initialization by internal circuits

(2−1) Initialization By Internal Reset Circuits

The NJU6461 is automatically initialized by internal power on initialization circuits when the power is turned on. In the internal power on initialization, following instructions are executed. During the Internal power on initialization, the busy flag (BF) is "1" and this status is kept 10 ms after V_{DD} rises to 2.4V.

Initialization flow is shown below:



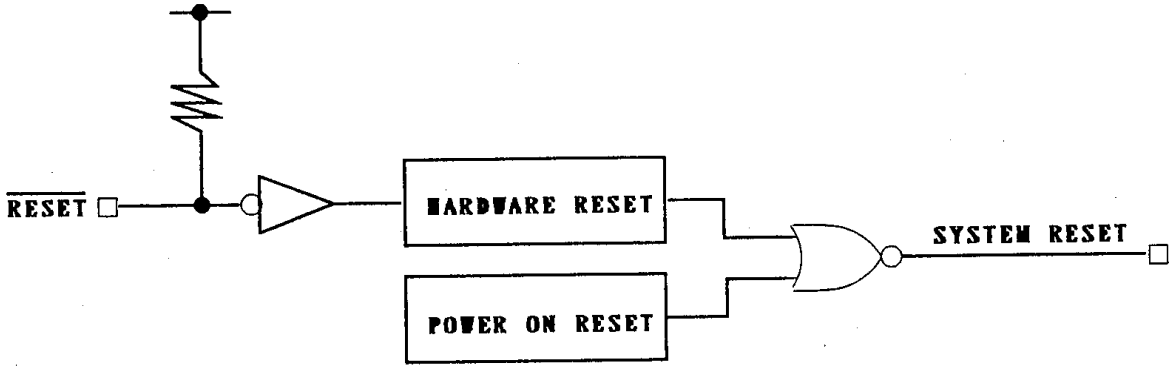
NOTE
If the condition of power supply rise time described in the Electrical Characteristics is not satisfied, the internal Power On Initialization Circuits will not operated and initialization will not performed.
In this case the initialization by MPU software is required.

5

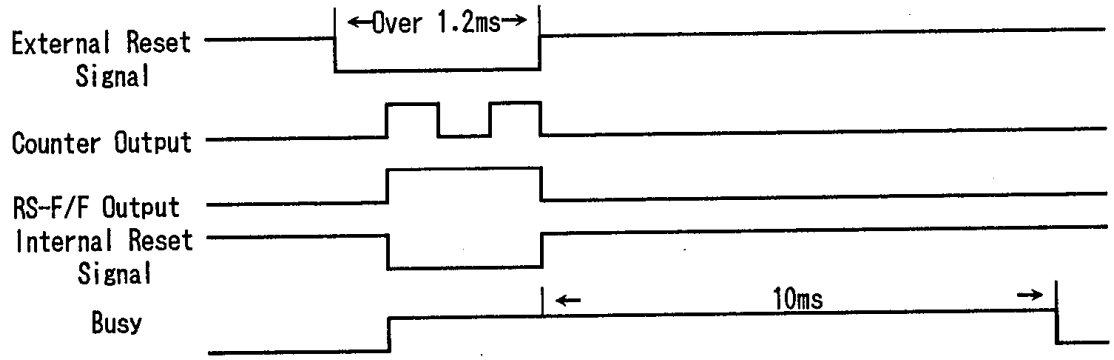
(2-2) Initialization By Hardware

The NJU6461 incorporates $\overline{\text{RESET}}$ terminal to initialize the all system. When the "L" level input over than 1.2ms to the $\overline{\text{RESET}}$ terminal, reset sequence is executed. In this time, busy signal output during 10ms after $\overline{\text{RESET}}$ terminal goes to "H".

• Reset Circuit



• Timing Chart



5

(3) Instructions

The NJU6461 incorporates two registers, an Instruction Register (IR) and a Data Register(DR). These two registers store control information temporarily to allow interface between NJU6461 and MPU or peripheral ICs operating different cycles. The operation of NJU6461 is determined by this control signal from MPU. The control information includes register selection signals (RS), read/write signals (R/W) and data bus signals (DB_0 to DB_7).

Table 4. shows each instruction and its operating time.

Note 1) The execution time mentioned in Table 4. based on fcp or fosc=80kHz.
If the oscillation frequency is changed, the execution time is also changed.

Table 4. Table of Instructions

INSTRUCTIONS	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	EXEC TIME
			C	O	D	E						
Maker Testing	0	0	0	0	0	0	0	0	0	0	All "0" code is using for maker testing.	
Clear Display	0	0	0	0	0	0	0	0	0	1	Display clear and sets DD RAM address 0 in AC.	1.63ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 in AC and returns display being shifted to original position. DD RAM contents remain unchanged	125us
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display are performed in data read/write. I/D=1:Increment, I/D=0:Decrement S=1:Accompanies display shift	125us
Display On/Off Control	0	0	0	0	0	0	1	D	C	B	Sets of display On/Off(D), cursor On/Off(C) and blink of cursor position character(B).	125us
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents S/C=1 : Display shift S/C=0 : Cursor shift R/L=1 : Shift to the right R/L=0 : Shift to the left	175us
Function Set	0	0	0	0	1	DL	1	*	*	*	Sets interface data length(DL). DL=1 : 8 bits , DL=0 : 4 bits Note: DB3 must be input "1".	125us
Set CG RAM Address	0	0	0	1	*	←	A_{CG}			→	Sets CG RAM address. After this instruction, the data is transferred to/from CG RAM.	125us
Set DD RAM Address	0	0	1	←			A_{DD}			→	Sets DD RAM address. After this instruction, the data is transferred to/from DD RAM.	125us
Read Busy Flag & Address	0	1	BF	←			AC_{DD}			→	Reads busy flag and AC contents. BF=1 : Internally operating BF=0 : Can accept instruction	0us
	0	1	BF	*	*	←		AC_{CG}		→		
Write Data to CG & DD RAM	1	0	←	Write Data (DD RAM)						→	Writes data into DD or CG RAMs.	125us
	1	0	*	*	*	←	Write Data (CG RAM)			→		
Read Data from CG or DD RAM	1	1	←	Read Data (DD RAM)						→	Reads data from DD or CG RAMs.	175us
	1	1	*	*	*	←	Read Data (CG RAM)			→		
Explanation of Abbreviation	DD RAM : Display data RAM , CG RAM : Character generator RAM A_{CG} : CG RAM address , A_{DD} : DD RAM address, Corresponds to cursor address AC : Address counter used for both of DD and CG RAMs											

* Don't care

5

(3−1) Description of each instructions

(a) Maker Testing

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	0	0

All "0" code in 4-bit length is using for device testing mode (only for maker). Therefore, please avoid all "0" input or no meaning Enable signal input at data "0". (Especially please pay attention the output condition of Enable signal when the power turns on.)

(b) Clear Display

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	0	1

Clear display instruction is executed when the code "1" is written into DB_0. When this instruction is executed, the space code $(20)_H$ is written into every DD RAM address, the DD RAM address $(00)_H$ is set into the address counter and entry mode is set increment.

If the cursor or blink are displayed, they are returned to the left end of the 1st-line in the LCD.

The S of entry mode does not change.

Note: The character pattern for character code $(20)_H$ must be blank code in the user-defined character pattern(Custom font).

(c) Return Home

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	0	0	0	0	0	0	0	0	1	*	* = Don't care

Return home instruction is executed when the code "1" is written into DB_1. When this instruction is executed, the DD RAM address 0 is set into the address counter. Display is returned its original position if shifted, the cursor or blink are returned to the left end of the LCD, (the left end of the 1st line in the 2-line display mode) if the cursor or blink are on the display.

The DD RAM contents do not change.

(d) Entry Mode Set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

Entry mode set instruction which sets the cursor moving direction and display shift On/Off, is executed when the code "1" is written into DB_2 and the codes of (I/D) and (S) are written into DB_1(I/D) and DB_0(S), as shown below.

(I/D) sets the address increment or decrement, and the (S) sets the entire display shift in the DD RAM writing.

I/D	Function
1	Address increment: The address of the DD RAM or CG RAM increment (+1) when the read/write, and the cursor or blink move to the right.
0	Address decrement: The address of the DD RAM or CG RAM decrement (-1) when the read/write, and the cursor or blink move to the left.

S	Function
1	Entire display shift. The shift direction is determined by I/D.: shift to the left at I/D=1 and shift to the right at the I/D=0. The shift is operated only for the character, so that it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM and writing/reading into/from CG RAM.
0	The display does not shifting.

5

(e) Display On/Off Control

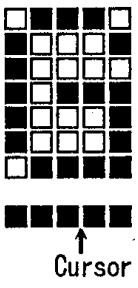
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	1	D	C	B

Display On/Off control instruction which controls the whole display On/Off, the cursor On/Off and the cursor position character blink, is executed when the code "1" is written into DB_3 and the codes of (D), (C) and (B) are written into DB_2(D), DB_1(C) and DB_0(B), as shown below.

D	Function
1	Display On.
0	Display Off. In this mode, the display data remains in the DD RAM so that it is retrieved immediately on the display when the D change to 1.

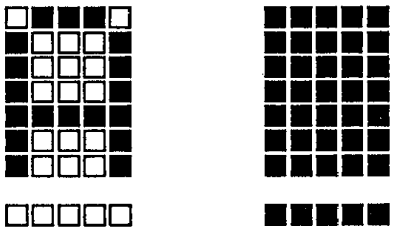
C	Function
1	Cursor On. The cursor is displayed by 5 dots on the 8th line.
0	Cursor Off. Even if the display data write, the I/D etc does not change.

B	Function
1	The cursor position character is blinking. Blinking rate is 540ms at f_{OSC}=80kHz for 12-character 2-line. The cursor and the blink can be displayed simultaneously.
0	The character does not blink.



Character Font 5 x 7 dots

(1) Cursor display example



Alternating display

(2) Blink display example

(f) Cursor/Display Shift

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	0	0	0	0	0	1	S/C	R/L	*	*	* = Don't care

The Cursor/Display shift instruction shifts the cursor position or display to the right or left without writing or reading display data. This function is used to correct or search the display. In the 2-line display, the cursor moves to the 2nd line when it passes the 12th digit of the 1st line. Notice that the 1st and 2nd line displays will shift at the same time. When the displayed data are shifted repeatedly, each line moves only horizontally.

The 2nd line display does not shift into the 1st line.

The contents of address counter(AC) does not change by operation of the display shift only.

This instruction is executed when the code "1" is written into DB_4 and the codes of (S/C) and (R/L) are written into DB_3(S/C) and DB_2(R/L) as shown below.

S/C	R/L	Function
0	0	Shifts the cursor position to the left ((AC) is decremented by 1)
0	1	Shifts the cursor position to the right ((AC) is incremented by 1)
1	0	Shifts the entire display to the left and the cursor follows it.
1	1	Shifts the entire display to the right and the cursor follows it.

(g) Function Set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	0	0	0	0	1	DL	1	*	*	*	* = Don't care

Function set instruction which sets the interface data length is executed, when the code "1" is written into DB_3, DB_5 and the code of (DL) is written into DB_4(DL), as shown below. Note that the DB_3 is must be "1" always.

In the serial interface operation mode, the DL is no meaning.

Note

This function set instruction must be performed at the head of the program prior to all other existing instructions(except Busy flag/Address read). This function set instruction can not be executed afterwards unless the interface data length change.

DL	Function
1	Set the interface data length of 8-bit (using from DB_7 to DB_0) in the parallel operation mode only.
0	Set the interface data length of 4-bit (using from DB_7 to DB_4) in the parallel operation mode only. The data must be sent or received twice in this mode.

(h) Set CG RAM Address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	0	0	0	1	*	A	A	A	A	A	* don't care
						←Higher order bit			Lower order bit →		

Set CG RAM address set instruction is executed when the code "1" is written into DB_6 and the address is written into DB_4 to DB_0 as shown above.

The address data mentioned by binary code " AAAAA " is written into the address counter (AC) together with the CG RAM addressing condition. After this instruction execution, the data writing/reading is performed into/from the CG RAM.

(i) Set DD RAM Address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	1	A	A	A	A	A	A	A
				←Higher order bit				Lower order bit→		

Set DD RAM address instruction is executed when the code "1" is written into DB_7 and the address is written into DB_6 to DB_0 as shown above.

The address data mentioned by binary code " AAAAAAA " is written into the address counter (AC) together with the DD RAM addressing condition. After this instruction execution, the data writing/reading is performed into/from the DD RAM.

Note : The 「AAAAAAA」 is $(00)_H$ to $(0B)_H$ for the 1st line and $(40)_H$ to $(4B)_H$ for the 2nd line.

(j) Read Busy Flag & Address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	1	BF	A	A	A	A	A	A	A
				←Higher order bit				Lower order bit→		

This instruction reads out the internal status of the NJU6461. When this instruction is executed, the busy flag (BF) stored in DB_7 and the address of the CG RAM or DD RAM stored in DB_6 to DB_0 are read out.

The (BF)="1" indicates that internal operation is in progress. The next instruction is inhibited when (BF)="1". Check the (BF) status before the next write operation.

(k) Write Data to CG RAM or DD RAM

・Write Data to DD RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	D	D	D	D	D	D	D	D
			←Higher order bit						Lower order bit→	

Write Data to DD RAM instruction is executed when the code "1" is written into (RS) and code "0" is written into (R/W).

By the execution of this instruction, the binary 8 bit data " DDDDDDDD " are written into the DD RAM. The selection of the DD RAM is determined by the previous instruction (DD RAM must be selected before). After this instruction execution, the address increment(+1) or decrement (-1) is performed automatically according to the entry mode set. And the display shift is also executed according to the previous entry mode set.

・Write Data to CG RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	1	0	*	*	*	D	D	D	D	D	* don't care
						←Higher order bit			Lower order bit→		

Write Data to CG RAM instruction is executed when the code "1" is written into (RS) and code "0" is written into (R/W).

By the execution of this instruction, the binary 5 bit data " DDDDD " are written into the CG RAM. The selection of the CG RAM is determined by the previous instruction (CG RAM must be selected before). After this instruction execution, the address increment(+1) or decrement (-1) is performed automatically according to the entry mode set. And the display shift is also executed according to the previous entry mode set.

5

(I) Read Data from CG RAM or DD RAM

• Read Data from DD RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	1	D	D	D	D	D	D	D	D

←Higher order bit Lower order bit→

Read Data from DD RAM instruction is executed when the code "1" is written into (RS) and (R/W).

By the execution of this instruction, the binary 8 bit data " DDDDDDDD " are read out from the DD RAM.

• Read Data from CG RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	1	1	*	*	*	D	D	D	D	D	* don't care

←Higher order bit Lower order bit →

Read Data from CG RAM instruction is executed when the code "1" is written into (RS) and (R/W).

By the execution of this instruction, the binary 5 bit data " DDDDD " are read out from the CG RAM.

5

The CG RAM or DD RAM is determined by previous instruction.

Before executing this instruction, either the CG RAM address set or DD RAM address set must be executed, otherwise the first read out data are invalidated.

When this instruction is serially executed, the next address data is normally read from the second read.

The address set instruction is not required if the cursor shift instruction is executed just beforehand (only DD RAM reading).

The cursor shift instruction has same function as the DD RAM address set, so that after reading the DD RAM, the address increment or decrement is executed automatically according to the entry mode.

But display shift does not occur regardless of the entry mode.

Note: The address counter(AC) is automatically incremented or decremented by 1 after write instruction to either of the CG RAM or DD RAM. Even if the read instruction is executed after this instruction, the addressed data can not be read out correctly. For a correct data read out, either the address set instruction or cursor shift instruction (only with DD RAM) must be implemented just before this instruction or from the second time read out instruction execution if the read out instruction is executed 2 times consecutively.

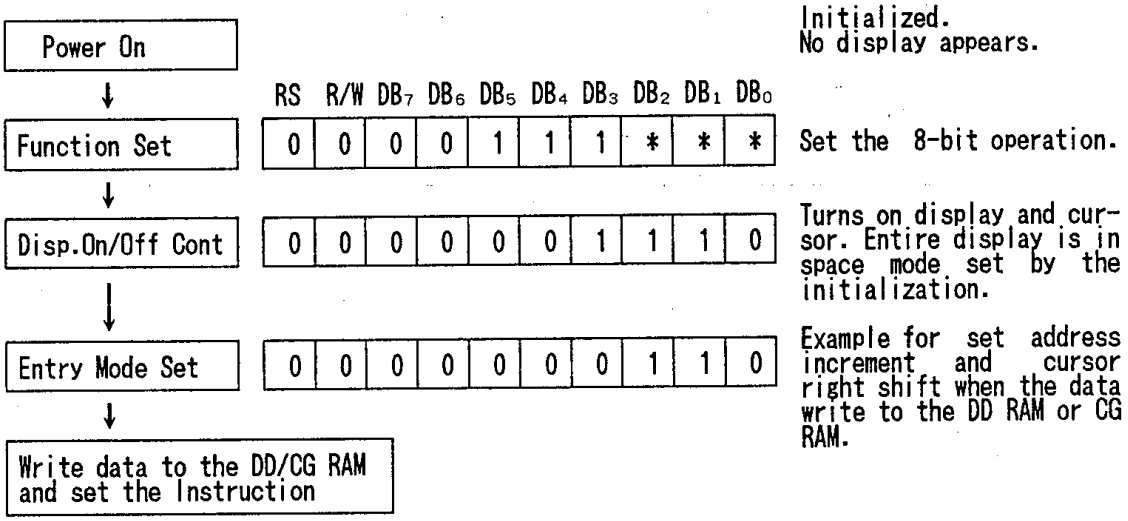
(3−2) Initialization using the internal reset circuits

(a) 8-bit operation (Using internal reset circuits).

The Function set, Display On/Off Control and Entry Set Instruction must be executed before the data input, as shown below.

The DD RAM of the NJU6461 can store up to 24 characters, as explained before, therefore the advertising moving display is available when combined with the display shift operation.

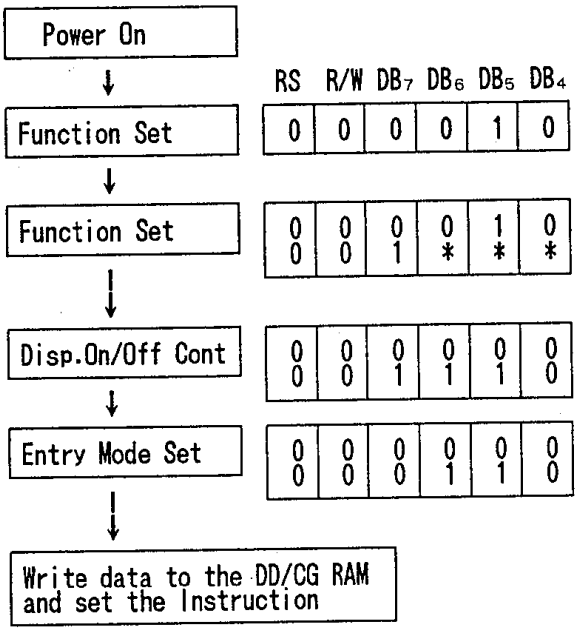
Since the display shift operation changes only display position and the DD RAM contents remain unchanged, display data which are entered first can be output when the return home operation is performed.



(b) 4-bit operation (Using internal reset circuits).

In the 4-bit operation, the function set must be performed by the user programming.

When the power is turned on, 8-bit operation is selected automatically, therefore the first input is performed under 8-bit operation. In this operation, full instruction can not input because of terminals DB_0 to DB_3 are no connection. Therefore, same instruction must be rewritten on the RS, R/W and DB_7 to DB_4, as shown below. Since one operation is completed by the two accesses in the 4-bit operation mode, rewrite is required to set the instruction code in full.



Initialized.
No display appears.

Set the 4-bit operation.
This step is executed in 8-bit mode set by the initialization.

Set the 4-bit operation.
The 4-bit operation starts from this step.

Turn on display and cursor.
Entire display is in space mode set by the initialization.

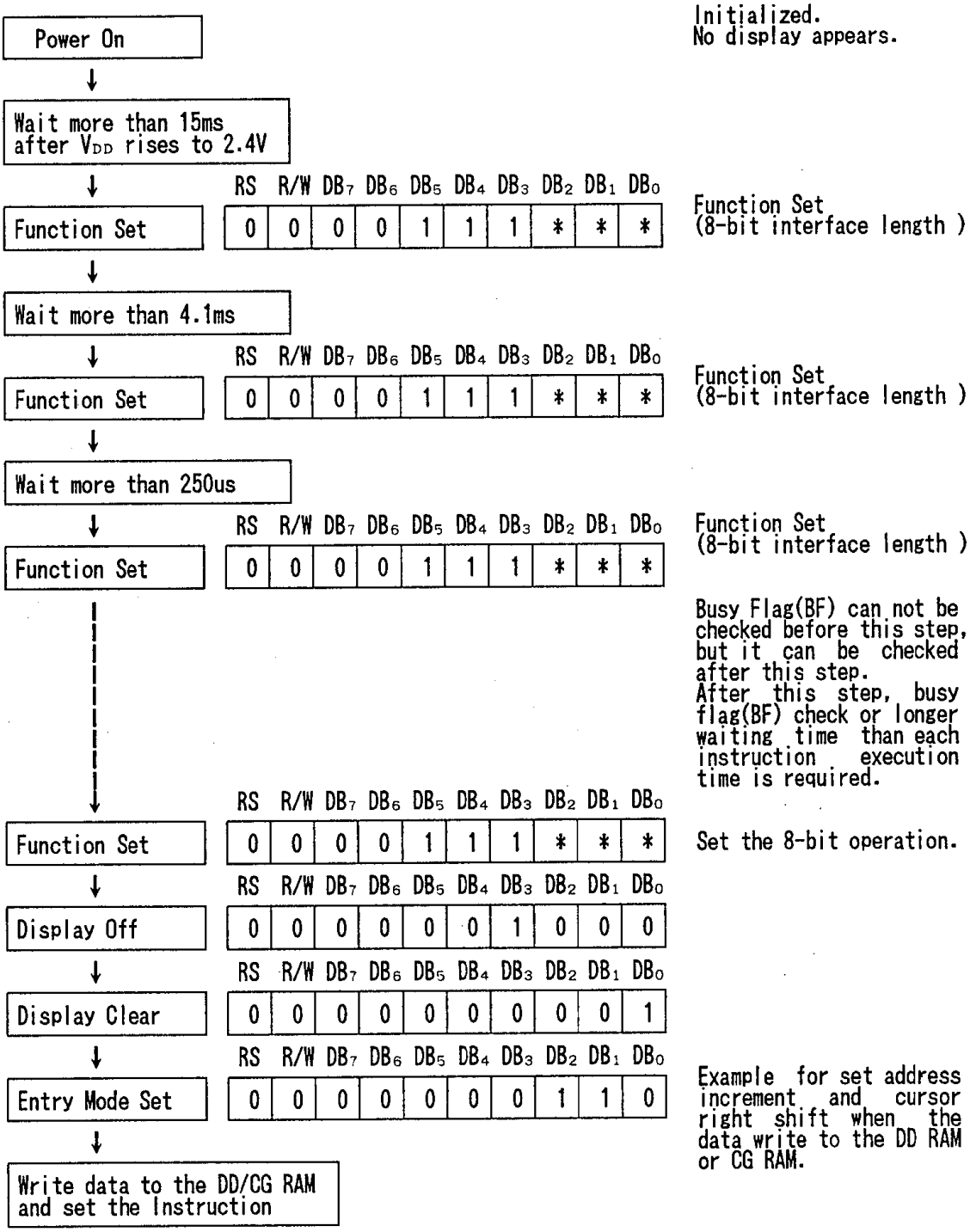
Example for set address increment and cursor right shift when the data write to the DD RAM or CG RAM.

5

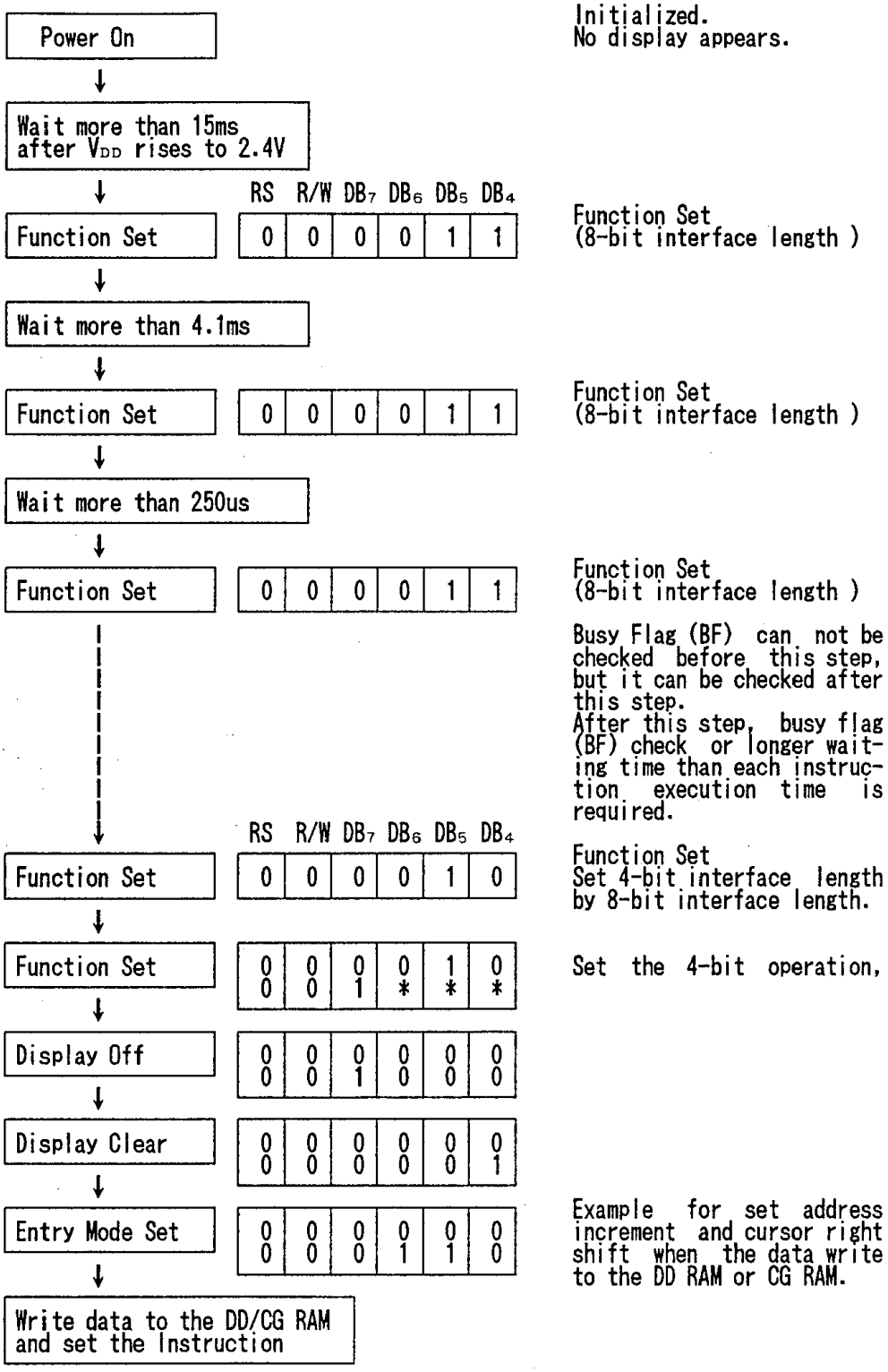
(3-3) Initialization by instruction

If the power supply conditions for the correct operation of the internal reset circuits are not met, the NJU6461 must be initialized by the instruction.

(a) Initialization by Instruction in 8-bit interface length.



(b) Initialization by Instruction in 4-bit interface length



(4) LCD DISPLAY

(4−1) Power Supply for LCD Driving

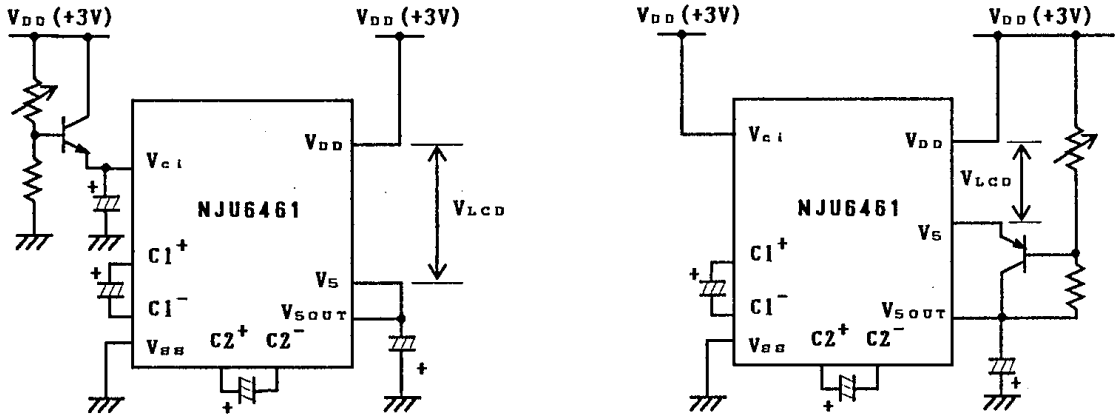
NJU6461 incorporate voltage tripler to generate LCD driving high voltage and bleeder resistance. The voltage tripler generate about triple voltage from the V_{ci} input voltage (V_{LCD}= 7.8V typ at Iout=100uA and V_{ci}=3V) and bleeder resistance generate each LCD driving voltage.

The bleeder resistance is set 1/5 bias suitable for 1/18 duty ratio and 1.0MΩ per resistance.

Furthermore, the bleeder resistance output the LCD Driving bias level through the voltage follower OP-AMP to get a enough display characteristics with low power consumption.

LCD Driving Voltage vs Duty Ratio

Power supply	Duty Ratio	1/18
	Bias	1/5
V_{SOUT}		V_{DD} to V_{LCD}



(a) 1/5 Bias(1/18 Duty)
(Voltage Tripler used example)

(b) 1/5 Bias(1/18 Duty)
(Voltage Tripler used example)

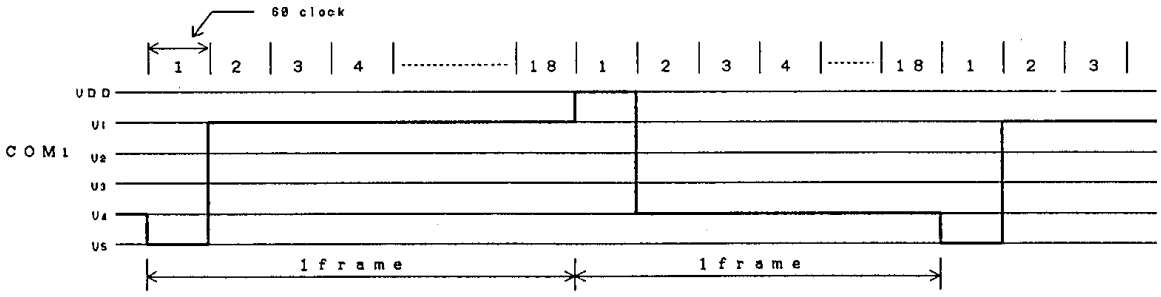
Note) The circuit value (resistors and transistor) should be designed, using the actual LCD panel.

(4−2) Relation between oscillation frequency and LCD frame frequency.

As the NJU6461 incorporate oscillation capacitor and resistance for CR oscillation, 80kHz oscillation is available without any external components.

The LCD frame frequency example mentioned below is based on 80kHz oscillation.
(1 clock = 12.5us)

1/18 duty



1 frame = 12.5(us) x 60 x 18 = 13.5(ms)
Frame frequency = 1/13.5(ms) = 74.1(Hz)

(5) Interface with MPU

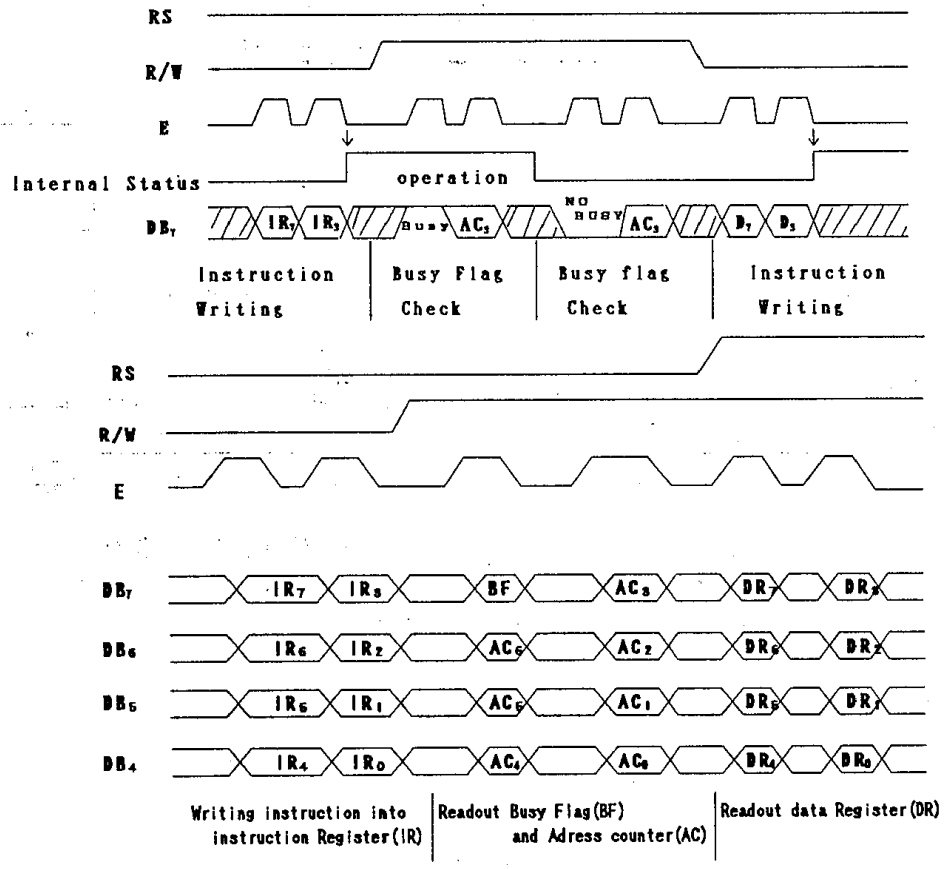
NJU6461 can be interfaced with both of 4/8-bit MPU and the two-time 4-bit or one-time 8-bit data transfer is available.

(5−1) 4-bit MPU interface

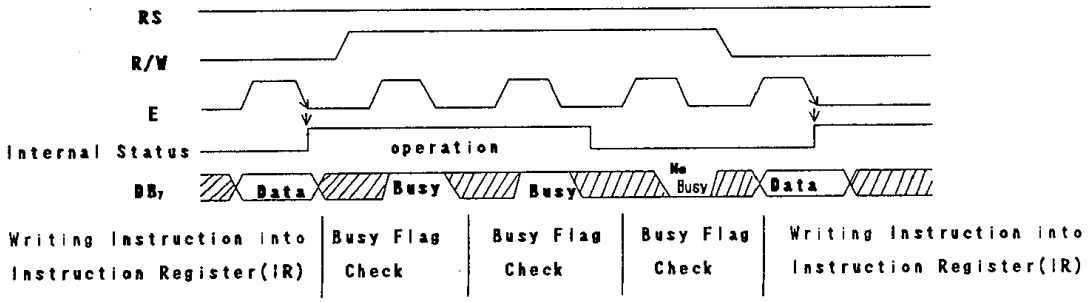
When the interface length is 4-bit, the data transfer is performed by 4 lines connected to DB_4 to DB_7 (DB_0 to DB_3 are not used). The data transfer with the MPU is completed by the two-time 4-bit data transfer.

The data transfer is executed in the sequence of upper 4-bit (the data DB_4 to DB_7 at 8-bit length) and lower 4-bit (the data DB_0 to DB_3 at 8-bit length).

The busy flag check must be executed after two-time 4bit data transfer (1 instruction execution). In this case the data of busy flag and address counter are also output twice.



(5−2) 8-bit MPU interface



(5−3) Serial interface

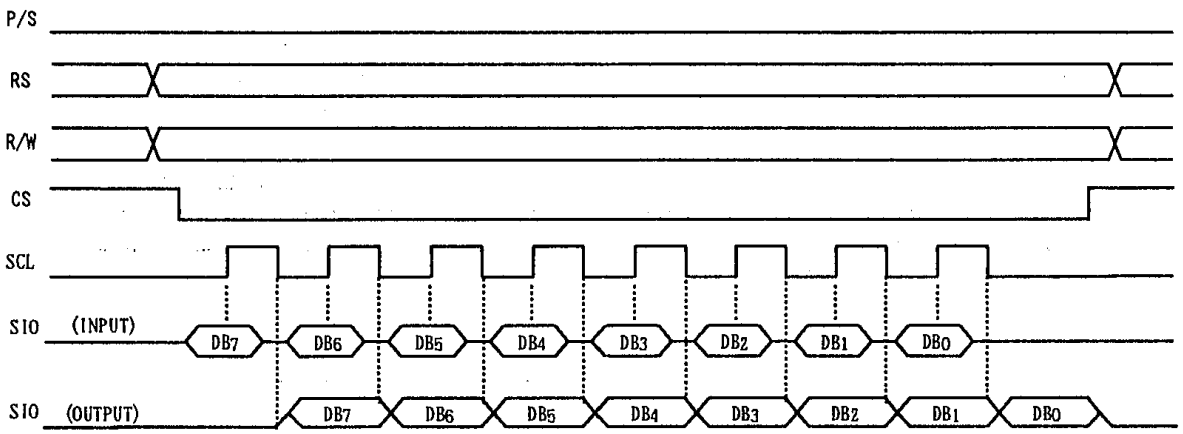
Serial interface circuit is activated when the P/S terminal is set to "L" level then the chip select terminal (CS) goes to "L" level. The data input/output is MSB first like as the order of DB_7, DB_6 ···· DB_0.

The input data is entered into the shift register synchronized at the rise edge of the serial clock SCL. The shift register converted to parallel data at the CS rise edge input. In case of entering over than 8-bit data, valid data is last 8-bit data.

The output data is exited from the shift register synchronized at the fall edge of the serial clock SCL.

The time chart for the serial interface is shown below.

Note : The level ("L" or "H") of RS and R/W terminals should be set before CS terminal goes to "L" level.



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (1)	V_{DD}	- 0.3 ~ + 7.0	V
Input Voltage	V_{IN}	- 0.3 ~ V_{DD}+0.3	V
Operating Temperature	Topr	- 30 ~ + 80	℃
Storage Temperature	Tstg	- 55 ~ + 125	℃

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recomended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 2) Decoupling capacitor should be connected between Vci and V_{SS} due to the stabilized operation for the Voltage Tripler (Doubler).

Note 3) All voltage values are specified as V_{SS} = 0V

Note 4) The relation : $V_{DD} \geqq V_{ci} > V_{SS}$, $V_{DD} > V_{SS} \geqq V_{5OUT}$, V_{SS}=0V must be maintained.
Turn on V_{DD} and V_{ci} at same time or turn on V_{DD} first then turn on V_{ci} must be required.
If the turn on sequence does not meet above conditions, latch up will occur.

■ ELECTRICAL CHARACTERISTICS

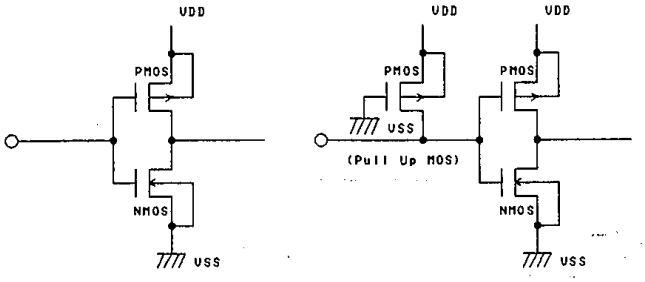
(V_{DD}=3V±20% , Ta=-20 ~ +75℃)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Operating Voltage		V_{DD}		2.4	3.0	3.6	V	
Input Voltage		V_{IH}		0.8V_{DD}		V_{DD}	V	5
		V_{IL}				0.2V_{DD}		
Output Voltage		V_{OH}	$-I_{OH}$=0.205mA	2.0			V	6
		V_{OL}	I_{OL}=1.6mA			0.5		
Driver On-resist.(COM)		R_{COM}	±I_d=50uA (All com term.)			20	kΩ	9
Driver On-resist.(SEG)		R_{SEG}	±I_d=50uA (All seg term.)			30		
Input Leakage Current		I_{LI}	V_{IN}=0 ~ V_{DD}	- 1		1	uA	7
Pull-up Resist Current		$-I_P$	V_{DD}=3V, RS,R/W,RESET,DB Terminals	10	25	50	uA	
Operating Current		I_{DD}	V_{DD}=3V, f_{OSC}=Internal freq		95	150	uA	8
Voltage Converter (Tripler)	Output Voltage	V_{up}	V_{ci}=3V, I_{OUT}=100uA, Ta=25℃	- 4.6	- 4.8		V	
	Input Voltage	V_{ci}		2.6		V_{DD}	V	
	Conversion Efficiency	V_{ef}	R_L=∞	95.0	99.9		%	
Bleeder resistance		R_B	V_{DD}-V_5=3V		5.0		MΩ	
Oscillation Frequency		f_{OSC}	V_{DD}=3V, Ta=25℃	56	80	104	kHz	
LCD Driving Voltage		V_{LCD}	V_{5OUT} Terminal, V_{DD}=3V	V_{DD}-3.0		V_{DD}-13.5	V	10
Output Current		I_5	V_{DD}=V_{ci}=3V			100	uA	

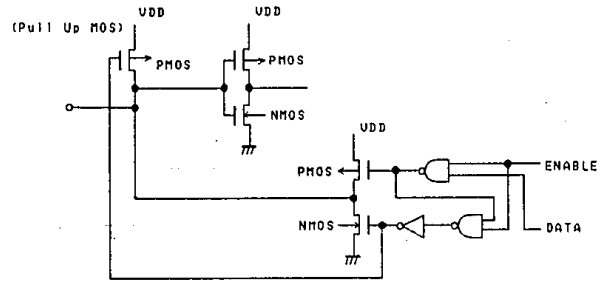
5

Note 5) Input/Output structure except LCD driver are shown below:

Input Terminal Structure



Input/Output Terminal Structure

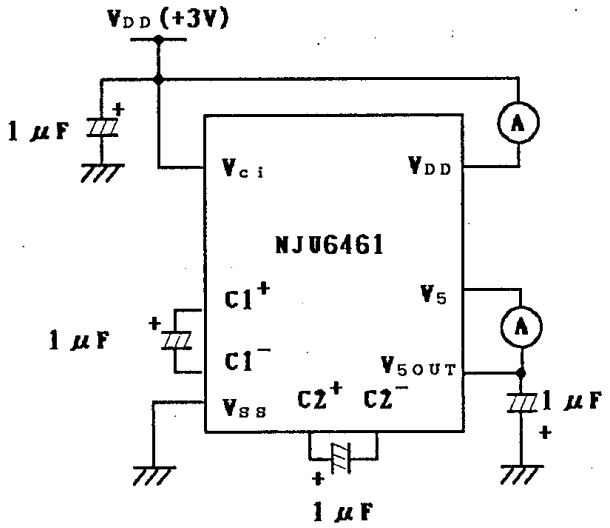


E Terminal RS,R/W Terminals

DB_0 to DB_7 Terminals

Note 6) Apply to the Output and Input/Output Terminal.
Note 7) Except pull-up resistance current and output driver current.
Note 8) Except Input/output current but including the current flow on bleeder resistance. If the input level is medium, current consumption will increase due to the penetration current. Therefore, the input level must be fixed to "H" or "L".

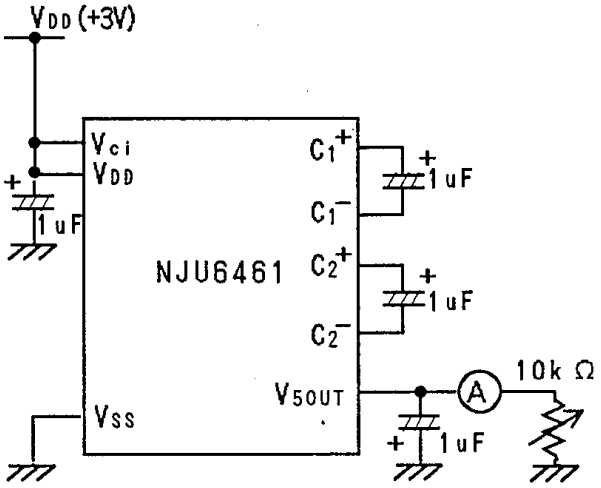
Operating Current Measurement Circuit



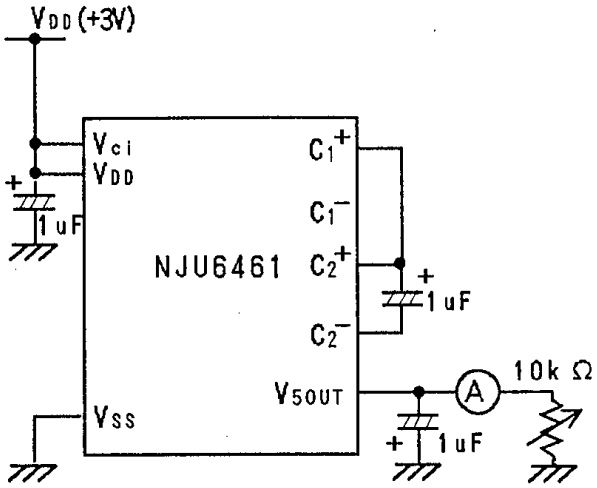
Note 9) R_{COM} and R_{SEG} are the resistance values between power supply terminals(V_{DD}, V_{5OUT} or V_1, V_2, V_3, V_4) and each common terminal(COM_1 to COM_{16} / COMMK1, COMMK2) and supply voltage (V_{DD}, V_{5OUT} or V_1, V_2, V_3, V_4) and each segment terminal (SEG_1 to SEG_{60}) respectively, and measured when the current I_d is flown on every common and segment terminals at a same time.

Note 10) Apply to the output voltage from each COM and SEG are less than ±0.15V against the LCD driving constant voltage (V_{DD}, V_{5OUT}) at no load condition.

Voltage Tripler Measurement Circuit



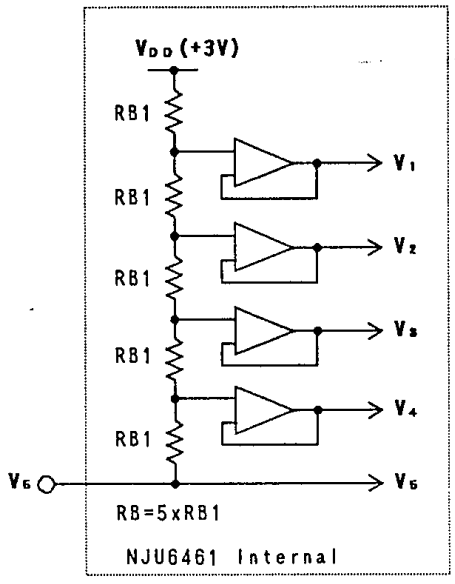
Voltage Doubler Measurement Circuit



Voltage Tripler/Doubler
Operation Clock Frequency = 10kHz

5

Bleeder Resistance and Buffer Amplifire



- **Bus timing characteristics (V_{DD} = 3.0V±20%, V_{SS} = 0V, Ta = -20 ~ +75℃)**

Write operation (Write from MPU to NJU6461)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Enable Cycle Time		t_{CYCE}	1		fig.1	us
Enable Pulse Width	"High" level	P_{WEH}	400			ns
Enable Rise Time, Fall Time		t_{Er}, t_{Ef}		20		
Set up Time	RS, R/W, E	t_{AS}	40			
Address Hold Time		t_{AH}	20			
Data Set up Time		t_{DSW}	70			
Data Hold Time		t_H	40			

Timing Characteristics (Write operation)

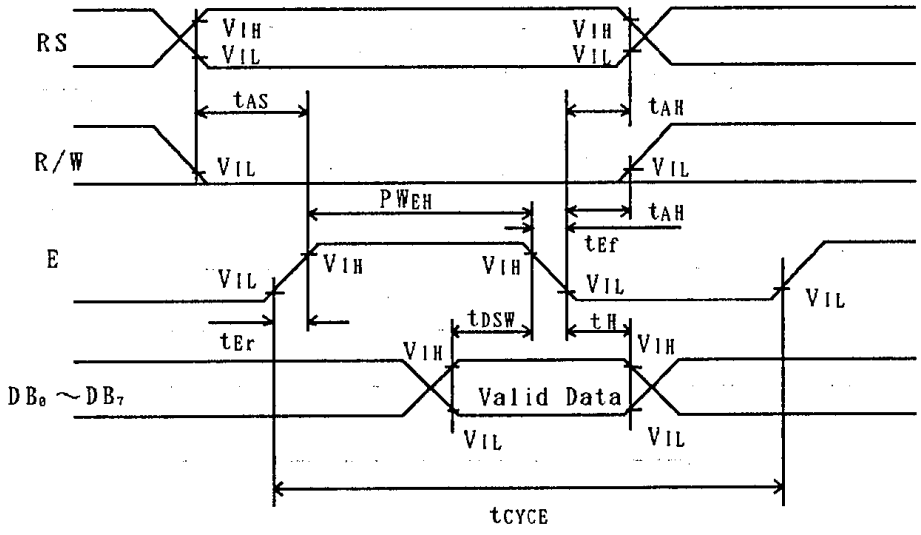


fig. 1

Read operation (Read from NJU6461 to MPU)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Enable Cycle Time		t_{CYCE}	1		fig.2	us
Enable Pulse Width	"High" level	P_{WEH}	700			ns
Enable Rise Time, Fall Time		t_{Er}, t_{Ef}		20		
Set up Time	RS, R/W, E	t_{AS}	40			
Address Hold Time		t_{AH}	20			
Data Delay Time		t_{DDW}		700		
Data Hold Time		t_{DDH}	40			

Load Condition of DB_0 to DB_7 : CL=100pF

Timing Characteristics (Read operation)

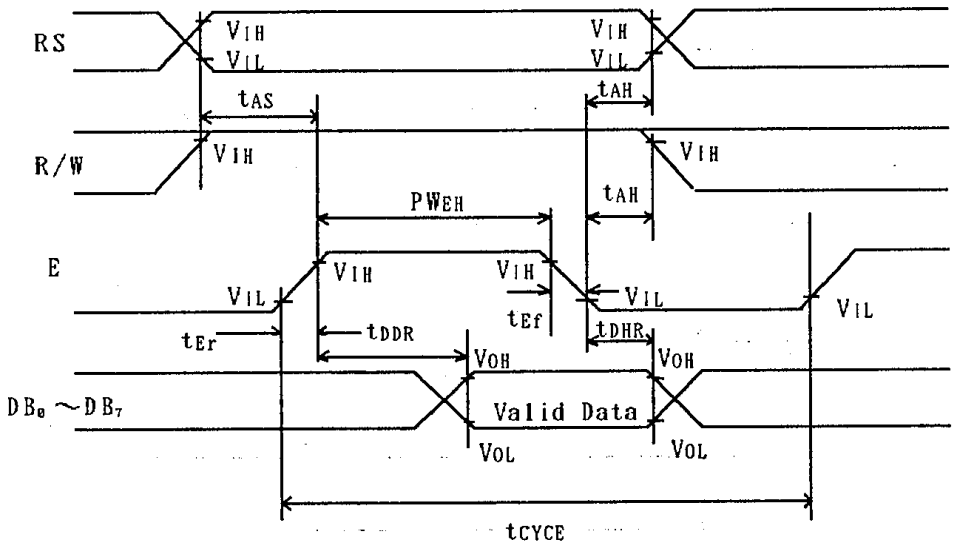


fig. 2

• Serial Interface Sequence

(V_{DD}=2.4~3.6V, V_{SS}=0V, Ta=-20~+75°C)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Serial Clock Cycle Time		t_{CYCE}	1		fig.3	μs
Serial Clock Width	"High" level	t_{SCH}	300			ns
	"LOW" level	t_{SCL}	700			ns
Serial Clock rise and fall Time		t_{SCR}, t_{SCF}		20		ns
Chip Select Pulse Width		PW_{CS}	500			ns
Chip Select Setup Time		t_{CSU}	200			ns
Chip Select Hold Time		t_{CH}	200			ns
Chip Select rise and fall Time		t_{CSR}, t_{CSF}		20		ns
Setup Time	RS, R/W - CS	t_{AS}	300			ns
Address Hold Time		t_{AH}	200			ns
Serial Input Data Setup Time		t_{SISU}	200			ns
Serial Input Data Hold Time		t_{SIH}	200			ns
Serial Output Data Delay Time		t_{SOD}		700		ns
Serial Output Data Hold Time		t_{SOH}	200			ns

Serial Interface

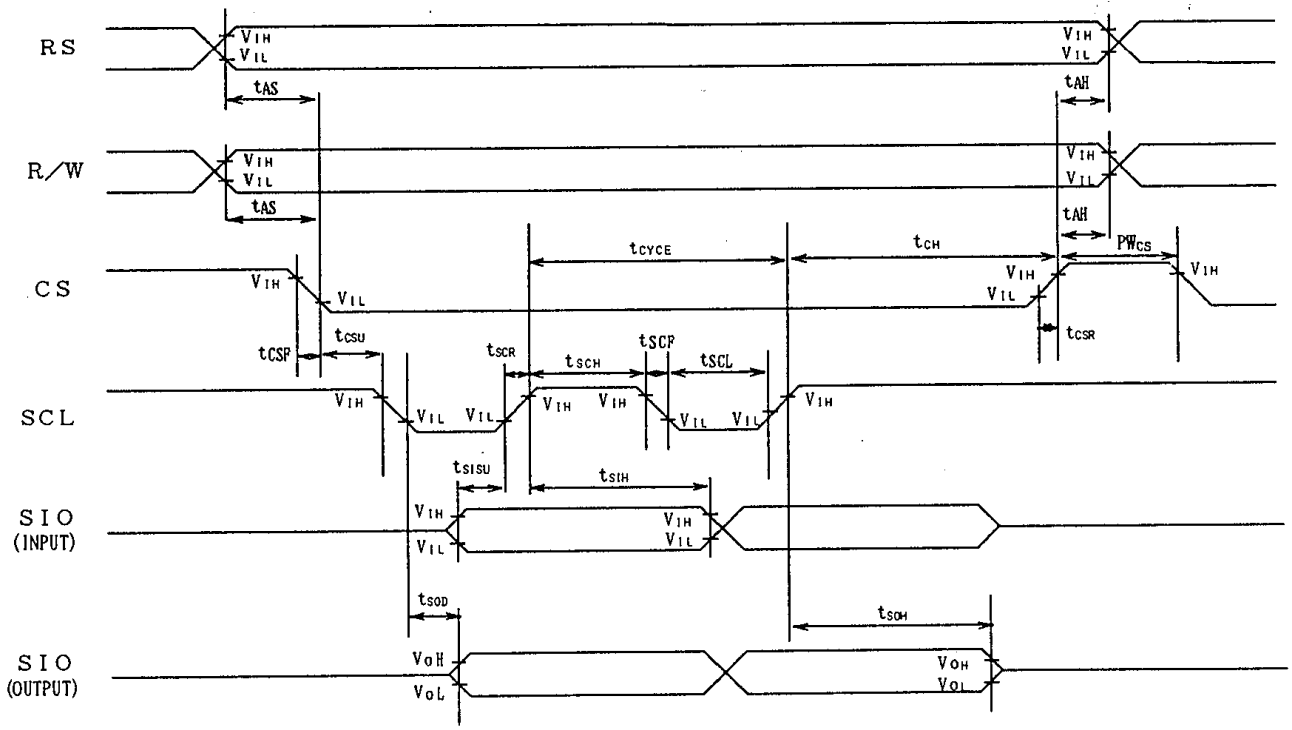
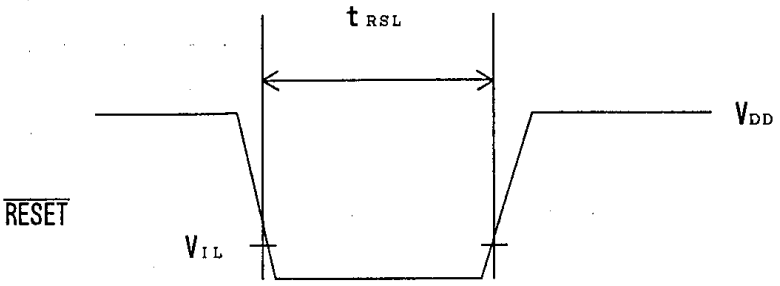


fig. 3

• The Input Condition when using the Hardware Reset Circuit

Input Timing

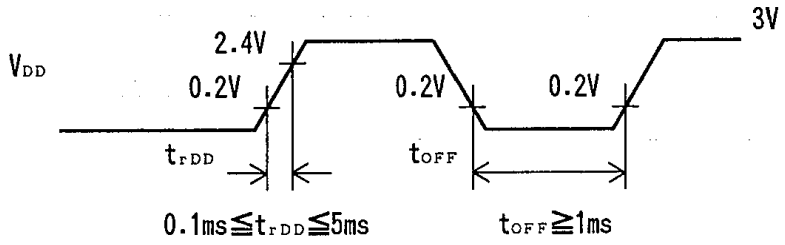


PARAMETER	SYMBOL	CONDITION	MIN	MAX	UNIT
Reset Input "L" Level Width	t_{RSL}	f_{OSC}=80kHz	1.2	-	ms

• Power Supply Condition when using the internal initialization circuit(Ta = -20 ~ +75°C)

PARAMETER	SYMBOL	CONDITION	MIN	MAX	UNIT
Power Supply Rise Time	t_{rDD}		0.1	5	ms
Power Supply OFF Time	t_{OFF}		1		

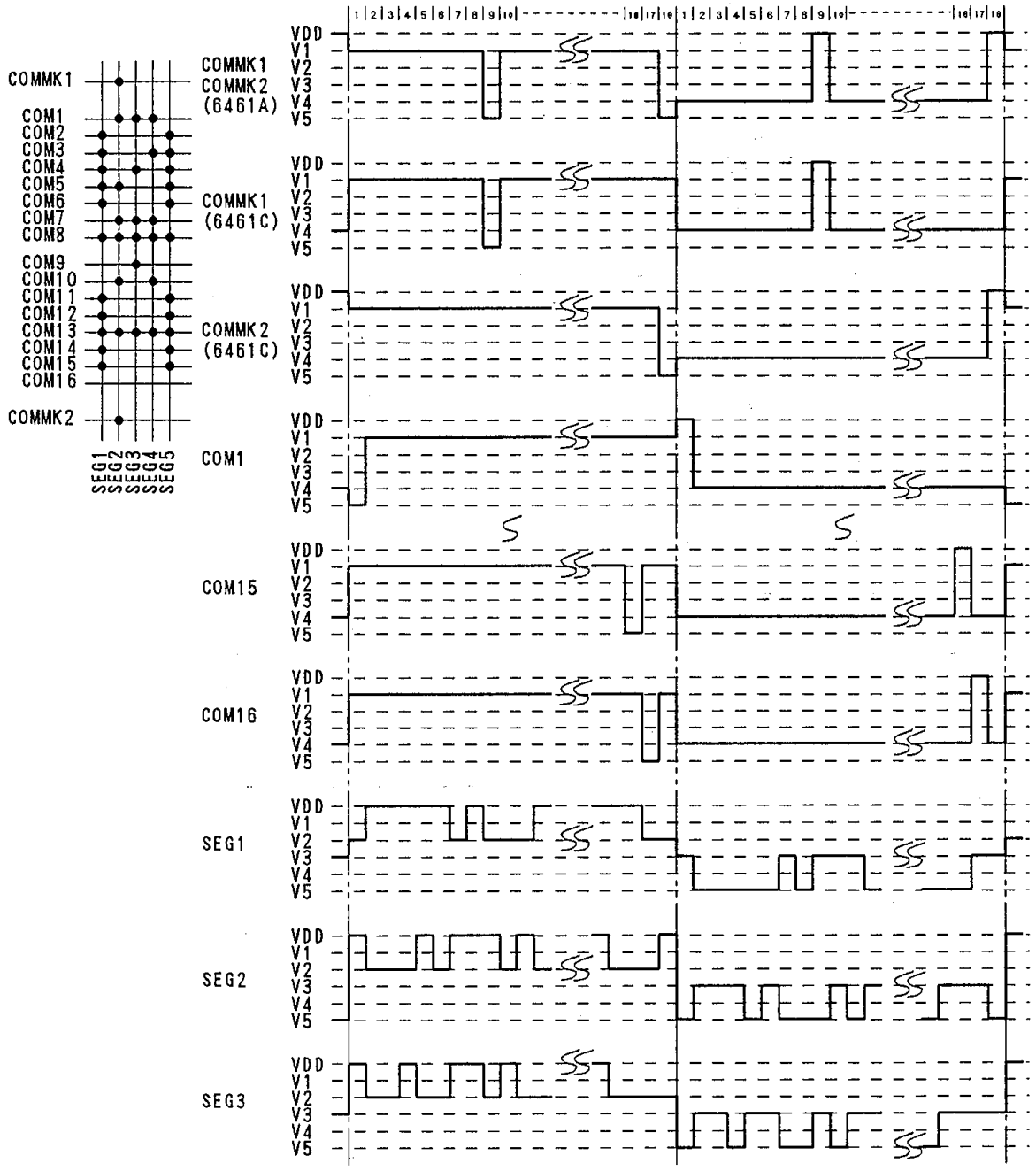
Since the internal initialization circuits will not operate normally unless the above conditions are met, in such a case initialize by instruction.
(Refer to initialization by the instruction)



t_{OFF} specifies the power off time in a short period off or cyclical on/off.

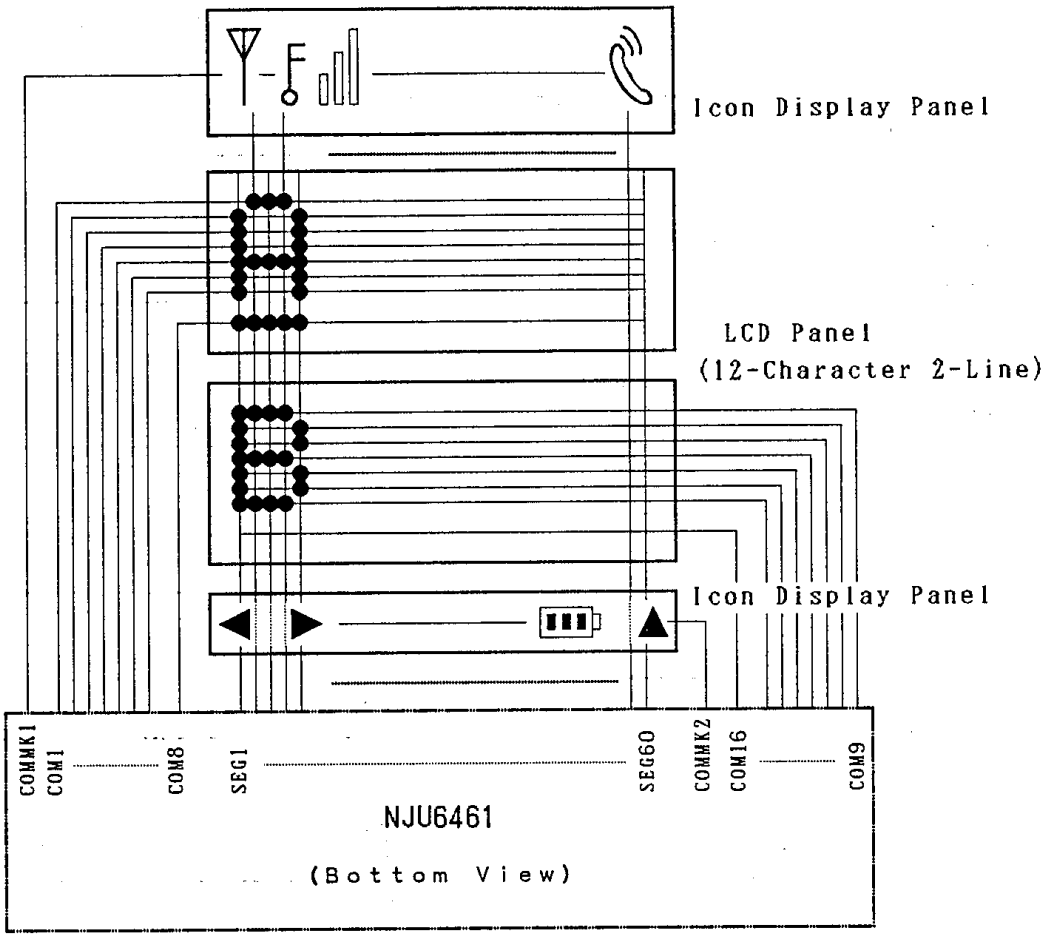
■ LCD DRIVING WAVE FORM

1/18 Duty Driving



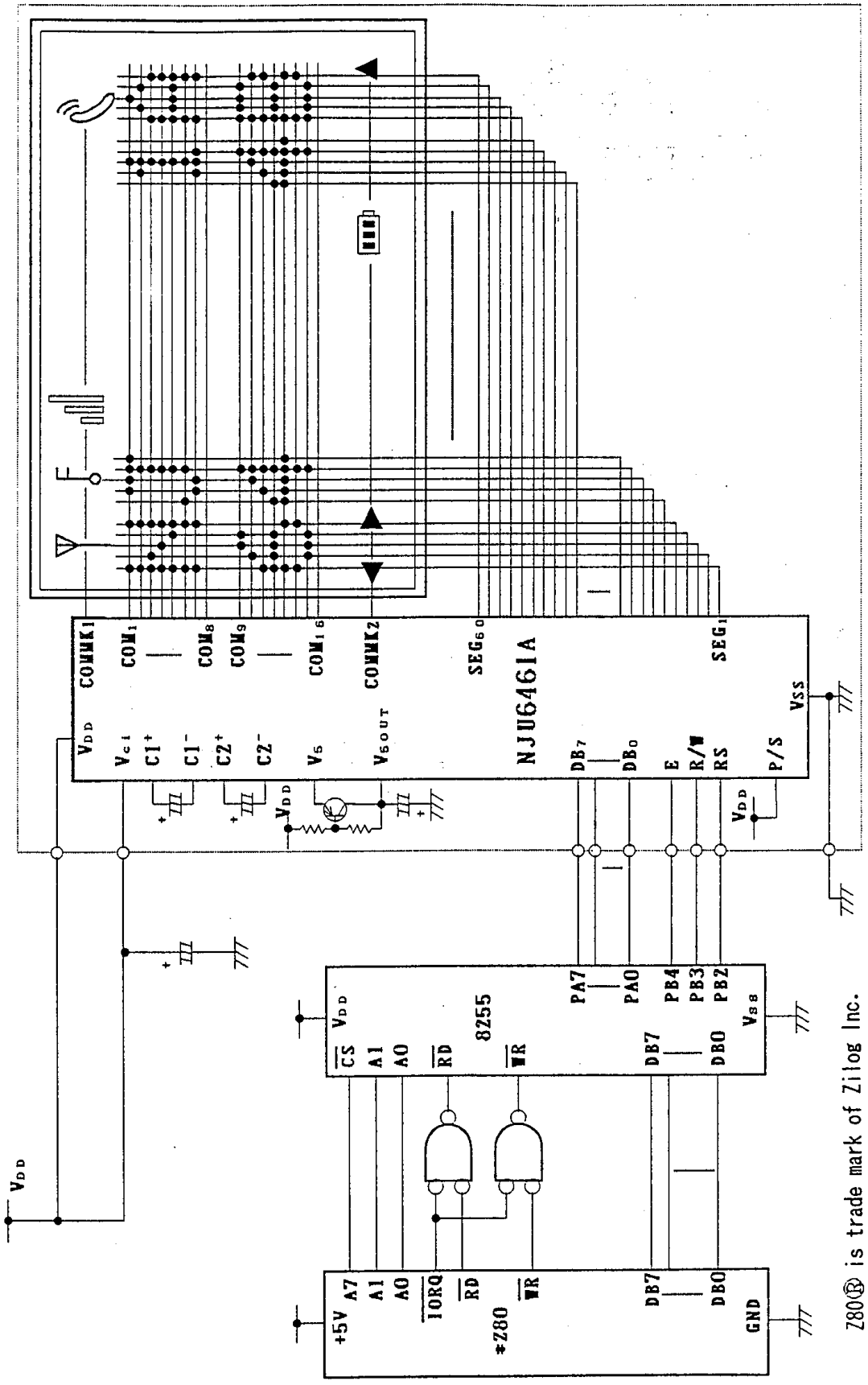
■ APPLICATION CIRCUITS (1)

- 12-character 2-line with Icon Display Example



Note : One segment line can apply only one Icon Display.
Please don't use same segnent line for both of upper and lower Icon display.

■ APPLICATION CIRCUITS (2)

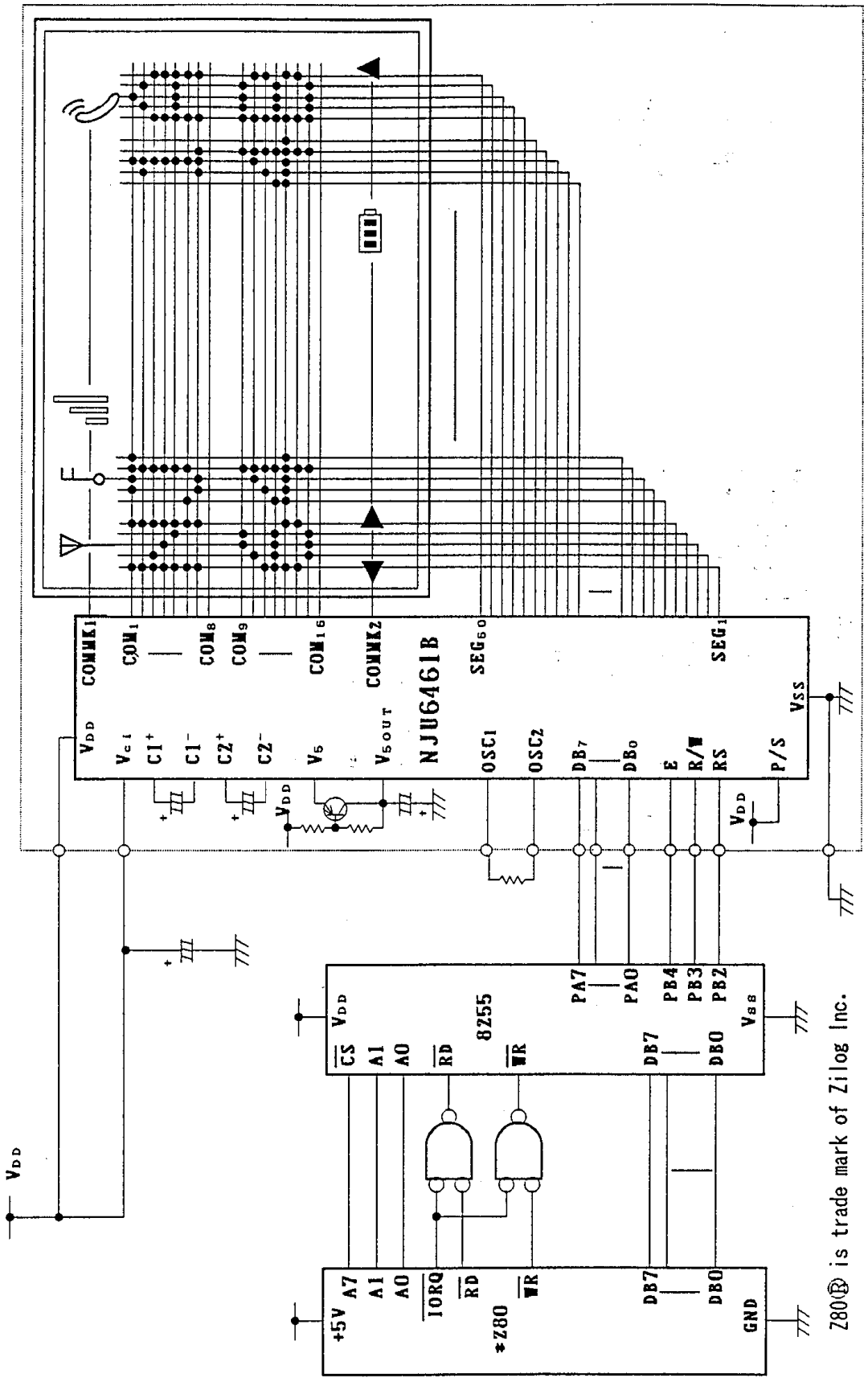


8 bit MPU interface example (Using the NJU6461A)

Z80® is trade mark of Zilog Inc.

5

■ APPLICATION CIRCUITS (3)

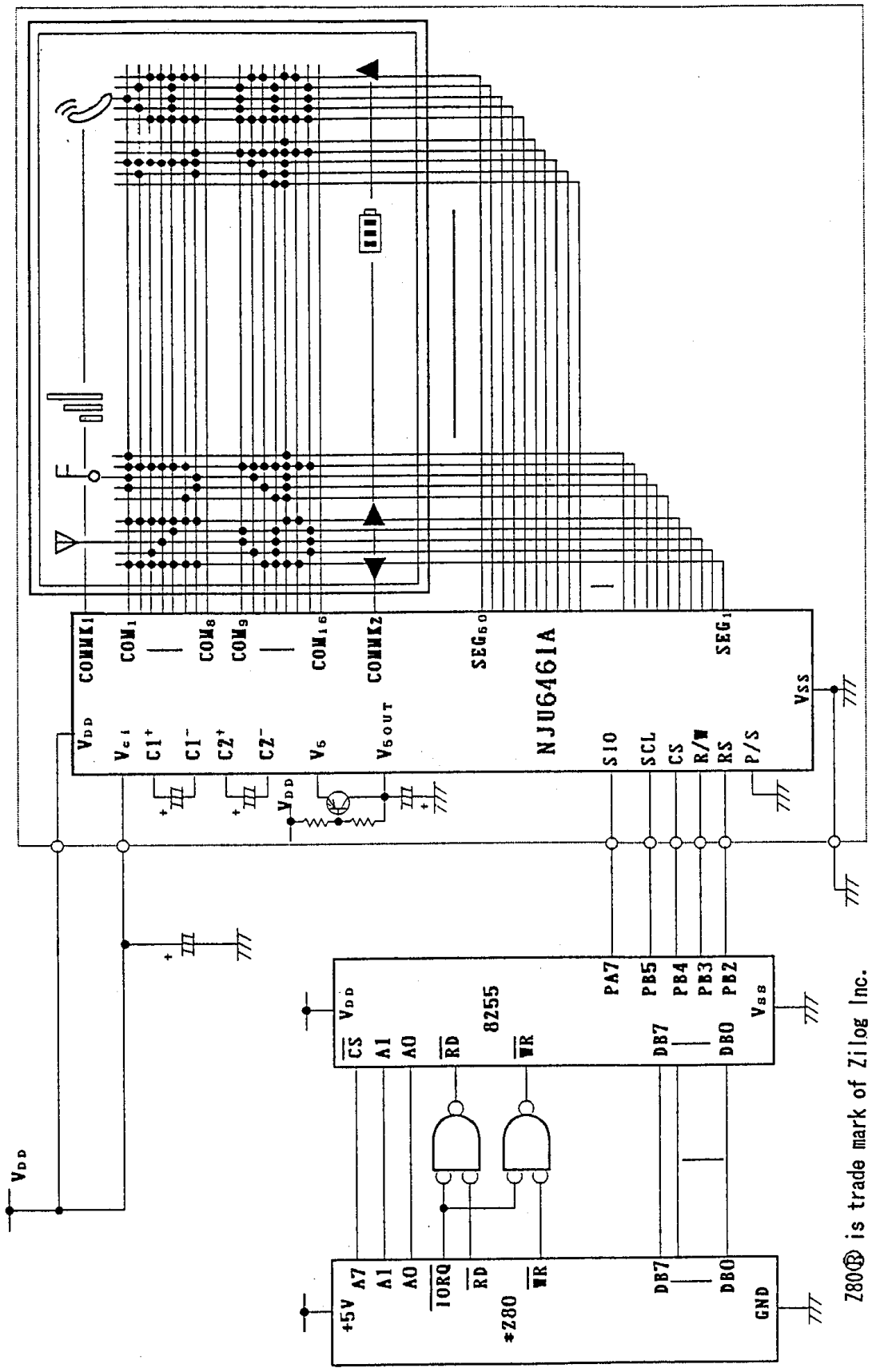


8 bit MPU interface example (Using the NJU6461B)

Z80® is trade mark of Zilog Inc.

5

■ APPLICATION CIRCUITS (4)



Serial interface example (Using the NJU6461A)

Z80® is trade mark of Zilog Inc.

5

MEMO