PRELIMINARY

12-Character 4-Line Dot Matrix Low Power

LCD Controller Driver with key Scan Function

■ GENERAL DESCRIPTION

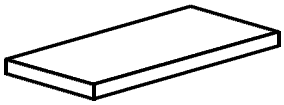
The NJU6475B is a Dot Matrix LCD Controller Driver for 12-character 4-line with Icon display in single chip. It contains voltage converter, voltage regulator, bleeder resistance, CR oscillator, instruction decoder, character generator ROM/RAM, high voltage operation controller/driver and key scan circuit.

The voltage converter generates (about 8V) from the supply voltage (3V) and regulated by the regulator. The bias level of LCD driving voltage is generated of high value bleeder resistance and the buffer amplifier matches the impedance. 16-step contrast control function is incorporated for its adjustment. Therefore, simple power supply circuit and easy contrast adjustment are available. The complete CR oscillator is incorporated without external components for oscillation circuit. The microprocessor interface circuit which operates by 1MHz, can be selected serial interface.

The character generator ROM consisting of 10,080bits stores 252 kinds of character Font.

Each 160bits CG RAM and Icon display RAM can story 4 kinds of special character to display on the dot matrix display area or 128 kinds of Icon on the display area.

■ PACKAGE OUTLINE

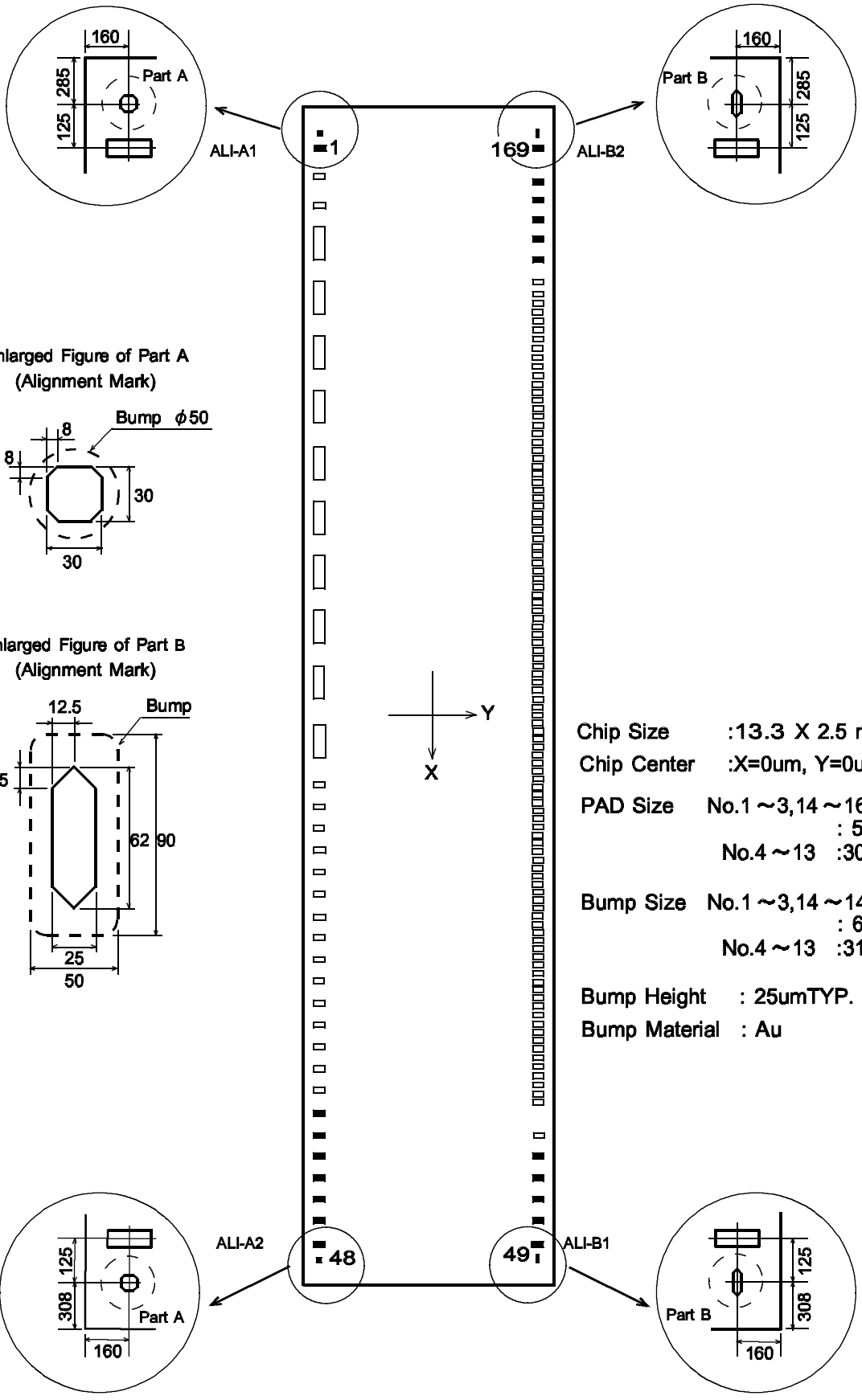


NJU6475B

■ FEATURES

- 12-Character 4-Line Dot Matrix LCD Controller Driver
- Maximum 128-Icon Display
- Serial CPU Interface
- Display Data RAM - 48 x 8 Bits :Maximum 12-Character 4-Line Display
- Character Generator ROM - 10,080 Bits:252 Characters (5 x 8 Dots)
- Character Generator RAM - 32 x 5 Bits :4 Patterns (5 x 8 Dots)
- Icon Display RAM - 32 x 5 Bits :Maximum 128-Icon
- High Voltage LCD Driver : 37-Common/63-Segment
- Duty & Bias Ratio : 1/36 duty 1/7Bias
- Useful Instruction Set : Clear Display, Return Home, Display On/Off Control Display Blink,Cursor Shift, Character Shift
- Common and Segment Driver location Order Select Function (Mode-A, Mode-B)
- Power On Reset Circuit On Chip
- Hardware Reset
- Voltage Regulator On Chip
- Electrical Variable Resistance On Chip
- 32-key scan function (8 x 4 Matrix)
- Oscillation circuit On Chip
- Voltage Converter (Doubler,Tripler) On Chip
- Bleeder Resistance On Chip
- Low Oprating Current
- Operating Voltage - 2.4V to 3.6V (Except For LCD Driving Voltage)
- Package Outline - Bumped-Chip / TCP
- C-MOS Technology

■ PAD LOCATION



Chip Size :13.3 X 2.5 mm
Chip Center :X=0um, Y=0um

PAD Size No.1～3,14～169
: 50um X 90um
No.4～13 :300um X 90um

Bump Size No.1～3,14～146
: 60um X100um
No.4～13 :310um X100um

Bump Height : 25umTYP.
Bump Material : Au

■ PAD COORDINATES

Chip Size 11.22×2.5mm (Chip Center X=0um,Y=0um)

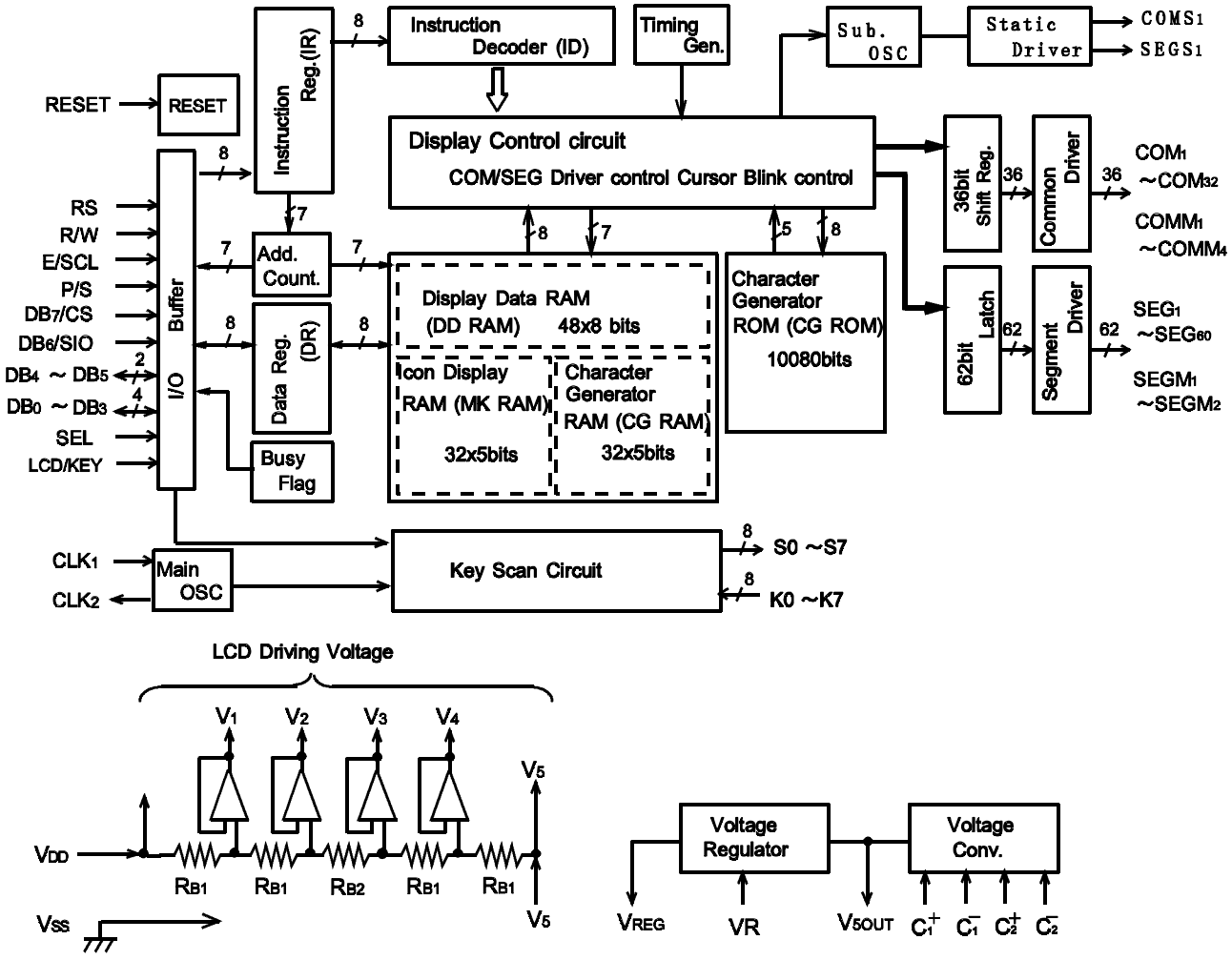
PAD No.	PAD Name		X=(um)	Y=(um)
	Mode A	Mode B		
1	ALI-A1	ALI-A1	-6240	-1090
2	OSC_1	OSC_1	-6020	-1090
3	OSC_2	OSC_2	-5775	-1090
4	V_5	V_5	-5479	-1090
5	V_{SS}	V_{SS}	-4979	-1090
6	V_{5OUT}	V_{5OUT}	-4479	-1090
7	$C2^-$	$C2^-$	-3979	-1090
8	$C2^+$	$C2^+$	-3479	-1090
9	$C1^-$	$C1^-$	-2979	-1090
10	$C1^+$	$C1^+$	-2479	-1090
11	V_{DD}	V_{DD}	-1979	-1090
12	VR	VR	-1479	-1090
13	V_{REG}	V_{REG}	- 979	-1090
14	TEST	TEST	- 531	-1090
15	SEL	SEL	- 302	-1090
16	RESET	RESET	- 74	-1090
17	P/S	P/S	155	-1090
18	RS	RS	383	-1090
19	R/W	R/W	612	-1090
20	E/SCL	E/SCL	840	-1090
21	LCD/KEY	LCD/KEY	1069	-1090
22	REQ	REQ	1298	-1090
23	DB_7/CS	DB_7/CS	1536	-1090
24	DB_6/SIO	DB_6/SIO	1773	-1090
25	DB_5	DB_5	2010	-1090
26	DB_4	DB_4	2247	-1090
27	DB_3	DB_3	2484	-1090
28	DB_2	DB_2	2721	-1090
29	DB_1	DB_1	2958	-1090
30	DB_0	DB_0	3195	-1090
31	K_0	K_0	3466	-1090
32	K_1	K_1	3632	-1090
33	K_2	K_2	3903	-1090
34	K_3	K_3	4068	-1090
35	S_0	S_0	4244	-1090
36	S_1	S_1	4352	-1090
37	S_2	S_2	4460	-1090
38	S_3	S_3	4568	-1090
39	S_4	S_4	4676	-1090
40	S_5	S_5	4784	-1090
41	S_6	S_6	4892	-1090
42	S_7	S_7	5000	-1090
43	NC	NC	5217	-1090
44	NC	NC	5417	-1090
45	NC	NC	5617	-1090
46	NC	NC	5817	-1090
47	NC	NC	6017	-1090
48	ALI-A2	ALI-A2	6217	-1090
49	ALI-B2	ALI-B2	6217	1090
50	NC	NC	6017	1090

PAD No.	PAD Name		X=(um)	Y=(um)
	Mode A	Mode B		
51	NC	NC	5817	1090
52	NC	NC	5617	1090
53	NC	NC	5417	1090
54	NC	NC	5217	1090
55	NC	NC	5017	1090
56	NC	NC	4817	1090
57	NC	NC	4617	1090
58	NC	NC	4417	1090
59	NC	NC	4217	1090
60	NC	NC	4017	1090
61	NC	NC	3817	1090
62	NC	NC	3617	1090
63	NC	NC	3417	1090
64	$SEGS_1$	$SEGS_1$	3160	1090
65	COM_9	COM_9	2780	1090
66	COM_{10}	COM_{10}	2700	1090
67	COM_{11}	COM_{11}	2620	1090
68	COM_{12}	COM_{12}	2540	1090
69	COM_{13}	COM_{13}	2460	1090
70	COM_{14}	COM_{14}	2380	1090
71	COM_{15}	COM_{15}	2300	1090
72	COM_{16}	COM_{16}	2220	1090
73	COM_{25}	COM_{25}	2140	1090
74	COM_{26}	COM_{26}	2060	1090
75	COM_{27}	COM_{27}	1980	1090
76	COM_{28}	COM_{28}	1900	1090
77	COM_{29}	COM_{29}	1820	1090
78	COM_{30}	COM_{30}	1740	1090
79	COM_{31}	COM_{31}	1660	1090
80	COM_{32}	COM_{32}	1580	1090
81	$SEGM_1$	$SEGM_2$	1500	1090
82	SEG_1	SEG_{60}	1420	1090
83	SEG_2	SEG_{59}	1340	1090
84	SEG_3	SEG_{58}	1260	1090
85	SEG_4	SEG_{57}	1180	1090
86	SEG_5	SEG_{56}	1100	1090
87	SEG_6	SEG_{55}	1020	1090
88	SEG_7	SEG_{54}	940	1090
89	SEG_8	SEG_{53}	860	1090
90	SEG_9	SEG_{52}	780	1090
91	SEG_{10}	SEG_{51}	700	1090
92	SEG_{11}	SEG_{50}	620	1090
93	SEG_{12}	SEG_{49}	540	1090
94	SEG_{13}	SEG_{48}	460	1090
95	SEG_{14}	SEG_{47}	380	1090
96	SEG_{15}	SEG_{46}	300	1090
97	SEG_{16}	SEG_{45}	220	1090
98	SEG_{17}	SEG_{44}	140	1090
99	SEG_{18}	SEG_{43}	60	1090
100	SEG_{19}	SEG_{42}	- 20	1090

PAD No.	PAD Name		X=(um)	Y=(um)
	Mode A	Mode B		
101	SEG_{20}	SEG_{41}	- 100	1090
102	SEG_{21}	SEG_{40}	- 180	1090
103	SEG_{22}	SEG_{39}	- 260	1090
104	SEG_{23}	SEG_{38}	- 340	1090
105	SEG_{24}	SEG_{37}	- 420	1090
106	SEG_{25}	SEG_{36}	- 500	1090
107	SEG_{26}	SEG_{35}	- 580	1090
108	SEG_{27}	SEG_{34}	- 660	1090
109	SEG_{28}	SEG_{33}	- 740	1090
110	SEG_{29}	SEG_{32}	- 820	1090
111	SEG_{30}	SEG_{31}	- 900	1090
112	SEG_{31}	SEG_{30}	- 980	1090
113	SEG_{32}	SEG_{29}	-1060	1090
114	SEG_{33}	SEG_{28}	-1140	1090
115	SEG_{34}	SEG_{27}	-1220	1090
116	SEG_{35}	SEG_{26}	-1300	1090
117	SEG_{36}	SEG_{25}	-1380	1090
118	SEG_{37}	SEG_{24}	-1460	1090
119	SEG_{38}	SEG_{23}	-1540	1090
120	SEG_{39}	SEG_{22}	-1620	1090
121	SEG_{40}	SEG_{21}	-1700	1090
122	SEG_{41}	SEG_{20}	-1780	1090
123	SEG_{42}	SEG_{19}	-1860	1090
124	SEG_{43}	SEG_{18}	-1940	1090
125	SEG_{44}	SEG_{17}	-2020	1090
126	SEG_{45}	SEG_{16}	-2100	1090
127	SEG_{46}	SEG_{15}	-2180	1090
128	SEG_{47}	SEG_{14}	-2260	1090
129	SEG_{48}	SEG_{13}	-2340	1090
130	SEG_{49}	SEG_{12}	-2420	1090
131	SEG_{50}	SEG_{11}	-2500	1090
132	SEG_{51}	SEG_{10}	-2580	1090
133	SEG_{52}	SEG_{9}	-2660	1090
134	SEG_{53}	SEG_{8}	-2740	1090

PAD No.	PAD Name		X=(um)	Y=(um)
	Mode A	Mode B		
135	SEG_{54}	SEG_{7}	-2820	1090
136	SEG_{55}	SEG_{6}	-2900	1090
137	SEG_{56}	SEG_{5}	-2980	1090
138	SEG_{57}	SEG_{4}	-3060	1090
139	SEG_{58}	SEG_{3}	-3140	1090
140	SEG_{59}	SEG_{2}	-3220	1090
141	SEG_{60}	SEG_{1}	-3300	1090
142	$SEGM_{2}$	$SEGM_{1}$	-3380	1090
143	COM_{24}	COM_{24}	-3460	1090
144	COM_{23}	COM_{23}	-3540	1090
145	COM_{22}	COM_{22}	-3620	1090
146	COM_{21}	COM_{21}	-3700	1090
147	COM_{20}	COM_{20}	-3780	1090
148	COM_{19}	COM_{19}	-3860	1090
149	COM_{18}	COM_{18}	-3940	1090
150	COM_{17}	COM_{17}	-4020	1090
151	COM_{8}	COM_{8}	-4100	1090
152	COM_{7}	COM_{7}	-4180	1090
153	COM_{6}	COM_{6}	-4260	1090
154	COM_{5}	COM_{5}	-4340	1090
155	COM_{4}	COM_{4}	-4420	1090
156	COM_{3}	COM_{3}	-4500	1090
157	COM_{2}	COM_{2}	-4580	1090
158	COM_{1}	COM_{1}	-4660	1090
159	$COMM_{4}$	$COMM_{4}$	-4740	1090
160	$COMM_{3}$	$COMM_{3}$	-4820	1090
161	$COMM_{2}$	$COMM_{2}$	-4900	1090
162	$COMM_{1}$	$COMM_{1}$	-4980	1090
163	$COMS_{1}$	$COMS_{1}$	-5085	1090
164	NC	NC	-5285	1090
165	NC	NC	-5485	1090
167	NC	NC	-5885	1090
168	NC	NC	-6085	1090
169	ALI-B2	ALI-B2	-6240	1090

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

PAD No.	Symbol	I/O	F u n c t i o n
11,5	V_{DD},V_{SS}	-	Power Source : V_{DD}=+3V GND : V_{SS}=0V
4	V_5	-	LCD driving voltage
2,3	OSC_1, OSC_2	I/O	System clock terminal Oscillation C and R are incorporated. (Normally Open) For external clock operation, the clock should be input on OSC_1.
17	P/S	I	Serial input select terminal (fixed to "L")
18	RS	I	Register selection signal input terminal "0" instruction register. (Writing) "1" Data register. (Writing, Reading)
19	R/W	I	Read(R) / Write(W) selection signal input terminal
20	E/SCL	I	Serial clock input terminal
23	DB_7/CS	I	Chip select signal
24	DB_6/SIO	I/O	Data input terminal (3-state data bus.)
25 - 30	DB_0 - DB_5	I	I/O port output terminal
22	REQ	O	This terminal normally output "L". When confirm a key action, REQ terminal output puls.
21	LCD/KEY	I	Fix to "H" Level
35 - 42	S_0 -S_7	O	Key scan signal data output terminal Open Drain Output
31 - 34	K_0 - K_3	I	Key scan data input terminal In case of non use, fix to "H".
158 - 151 65 - 72 150 - 143 73 - 80	COM_1 - COM_{32}	O	Common signal output terminal
162 - 159	$COMM_1$ - $COMM_4$	O	Icon common display signal output terminal
163	$COMS_1$	O	Static driving common signal output terminal When power down mode V_{DD} or V_{SS} levels are output.
82 - 141	SEG_1 - SEG_{60}	O	Segment signal output terminal
81,142	$SEGM_1$,$SEGM_2$	O	Icon segment driving signal output terminal

PAD No.	Symbol	I/O	F u n c t i o n
57	$SEGS_1$	O	Static driving segment signal output terminal When power down mode V_{DD} or V_{SS} level are output.
10,9 8,7	$C1^+$ $C1^-$ $C2^+$,$C2^-$	I/O	Step up voltage capacitor connecting terminal
6	V_{SOUT}	O	Step up voltage output terminal
13	V_{REG}	O	Voltage regulator output terminal Connect the resistor between this terminal and VR terminal.
12	VR	I	Reference voltage for voltage regulator input terminal Connect the resistor between this reference voltage and V_{DD} terminal.
16	$\overline{\text{RESET}}$	I	Reset terminal When the "L" level input over than 1.2ms to this terminal, the system is reset (at f_{osc}=180KHz).
15	SEL	I	Common and Segment driver location order select terminal. "0" Mode A location (See ■ PAD COORDINATES) "1" Mode B location (See ■ PAD COORDINATES)
14	TEST	I	Maker test terminal This terminal should be connected to V_{SS} (or open.)
43 - 47 50 - 63 164 - 168	NC	-	Non connection terminal These terminals are electrically open.
169 49 1 48	ALI-A1 ALI-A2 ALI-B1 ALI-B2	-	Alignment mark These terminals are electrically open.

■ FUNCTIONAL DESCRIPTION

(1) Description for each blocks

(1-1) Register

The NJU6475B incorporates three 8-bit registers, an instruction register (IR), and a Data Register (DR), Key Register (KR). The register (IR) stores an instruction code such as "clear display" and "cursor shift" or address data for Display Data RAM (DD RAM), Character Generator RAM (CG RAM) and Icon Display RAM (MK RAM). The MPU can write the instruction code and address data to the register (IR), but it cannot read out from register (IR). The Register (DR) is a temporary register, the data stored in the Register (DR) is written into DD RAM, MK RAM. A register from these two registers is selected by the register select signal (RS). Register (KR) is an only temporary register for key scan data. This Register (KR) can read out the contents when selected Key signal at "H" signal. And non relation ship with signal of register select (RS).

The Relation ship with RS, R/W register as shown below.

<Table-1> Register selection

RS	R/W	O p e r a t i o n
0	0	IR write & internal register operation mode (Clear Display etc...)
0	1	Read out (KR)
1	0	Write (DR) & internal register operation mode (DR→ DD RAM/CG RAM/MK RAM)
1	1	Read out (KR)

(1-2) Address Counter (AC)

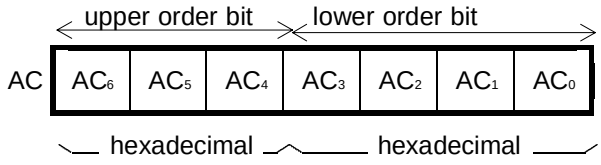
The address counter (AC) addresses the DD RAM, CG RAM or MK RAM. When the address setting instruction is written into register (IR), the address information is transferred from register (IR) to the address counter (AC). The selection of DD RAM, CG RAM or MK RAM is also determined by this instruction.

After writing (or reading) the display data to (or from) the DD RAM, CG RAM or MK RAM, the address counter (AC) increments (or decrements) automatically.

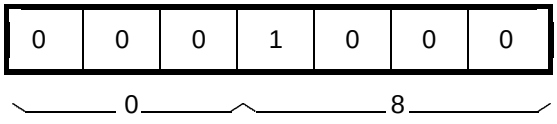
(1-3) Display Data RAM (DD RAM)

The display data RAM (DD RAM) consisting of 48 x 8 bits stores up to 48-character display data represented in 8-bit code.

The DD RAM address data set in the address counter (AC) is represented in Hexadecimal code.



(Example) DD RAM Address "08"



(1-3-1) The relation between DD RAM address and display position on the LCD

-12-Characters 4-Line Display

	1	2	3	4	5	6	7	8	9	10	11	12	← Display Position
1st Line	00	01	02	03	04	05	06	07	08	09	0A	0B	← DD RAM Address (Hexadecimal)
2nd Line	10	11	12	13	14	15	16	17	18	19	1A	1B	
3rd Line	20	21	22	23	24	25	26	27	28	29	2A	2B	
4th Line	30	31	32	33	34	35	36	37	38	39	3A	3B	

When the display shift is performed, the DD RAM address changes as follows:

[Left shift display]

(00)←	01	02	03	04	05	06	07	08	09	0A	0B	00
(10)←	11	12	13	14	15	16	17	18	19	1A	1B	10
(20)←	21	22	23	24	25	26	27	28	29	2A	2B	20
(30)←	31	32	33	34	35	36	37	38	39	3A	3B	30

[Right shift display]

0B	00	01	02	03	04	05	06	07	08	09	0A	→(0B)
1B	10	11	12	13	14	15	16	17	18	19	1A	→(1B)
2B	20	21	22	23	24	25	26	27	28	29	2A	→(2B)
3B	30	31	32	33	34	35	36	37	38	39	3A	→(3B)

(1-4) Character Generator ROM (CG ROM)

The Character Generator ROM (CG ROM) stores 5 x 8 dots character pattern represented in 8-bit character code. The capacity is up to 252 kinds of 5 x 8 dots character pattern.

The correspondence between character code and standard character pattern of NJU6475B is shown in table 2.

User defined character patterns (Custom Font) are also available by mask option. (in this case, the address $(20)_H$ are using for "Space Pattern".)

<Table-2> The Correspondence Between Character Code
and Standard Character Pattern (ROM Version -02)

Lower 4bit (Hexadecimal) \ Upper 4bit (Hexadecimal)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM (01)															
1	(02)															
2	(03)															
3	(04)															
4																
5																
6																
7																
8																
9																
A																
B																
C																
D																
E																
F																

(1-5) Character Generator RAM (CG RAM)

The Character Generator RAM stores any kinds of character pattern in 5 x 8 dots written by the user program to display user's original character pattern. The CG RAM can store 4 kinds of character in 5 x 8 dots mode.

To display user's original character pattern stored in the CG RAM, the address data $(00)_H$-$(03)_H$ should be written to the DD RAM as shown in Table-3.

<Table-3> Correspondence of CG RAM address, DD RAM character code and CG RAM character pattern (5 x 8 dots)

Character Code (DD RAM Data)	CG RAM Address		Character Pattern (CG RAM Data)		
7 6 5 4 3 2 1 0	7 6 5 4 3	2 1 0	4 3 2 1 0		
Upper Bits / Lower Bits	Upper	Lower	Upper	Lower	
0 0 0 0 0 0 0 0	0 1 0 0 0	0 0 0	1 1 1 1 0		Character Pattern Example (1)
		0 0 1	1 0 0 0 1		
		0 1 0	1 0 0 0 1		
		0 1 1	1 1 1 1 0		
		1 0 0	1 0 1 0 0		
		1 0 1	1 0 0 1 0		
		1 1 0	1 0 0 0 1		
		1 1 1	0 0 0 0 0		← Cursor Position
0 0 0 0 0 0 0 1	0 1 0 0 1	0 0 0	1 0 0 0 1		Character Pattern Example (2)
		0 0 1	0 1 0 1 0		
		0 1 0	1 1 1 1 1		
		0 1 1	0 0 1 0 0		
		1 0 0	1 1 1 1 1		
		1 0 1	0 0 1 0 0		
		1 1 0	0 0 1 0 0		
		1 1 1	0 0 0 0 0		← Cursor Position
		0 0 0			
		0 0 1			
⋮	⋮	⋮	⋮	⋮	
0 0 0 0 0 0 1 1	0 1 0 1 1				
		1 0 0			
		1 0 1			
		1 1 0			
		1 1 1			

Notes : 1. Character code bit 0,1 correspond to the CG RAM address bit 3,4 (2bits ; 4patterns).

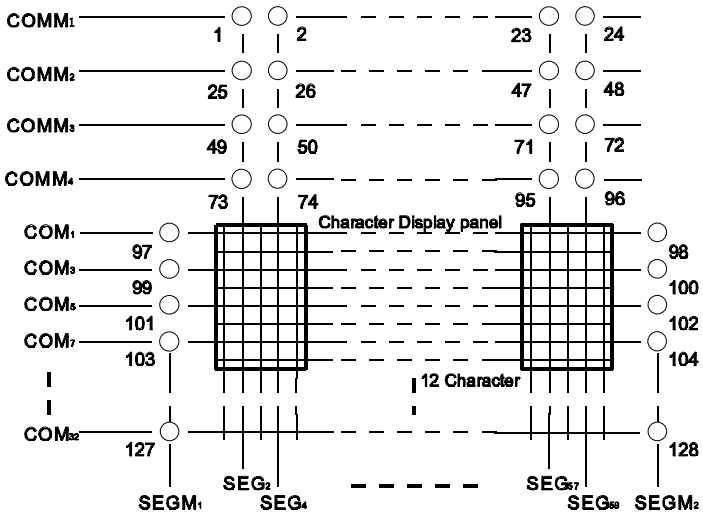
2. CG RAM address 0 to 2 designate character pattern line position. The 8th line should be "0". If there is "1" in the 8th line, but bit "1" is always displayed on the cursor position regardless of cursor existence.
3. Row position character pattern correspond to CG RAM data bits 0 to 4 are shown above.
4. CG RAM character patterns are selected when character code bits 2 to 7 are all "0" and these are addressed by character code bits "0" and "1".
5. "1" for CG RAM data corresponds to display on and "0" to display off.

(1-6) Icon display RAM (MK RAM)

The NJU6475B can display maximum 128 Icons.

The Icon display can be controlled by writing the data into MK RAM corresponding to the Icons.

The relation between MK RAM address and Icon display position is shown in Table-4.



<Table-4> Correspondence among Icon Position, MK RAM Address and Data

MK RAM Address (60_H - $7F_H$)		Bits for Icon Position MK RAM Address and Data								
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0110 0000	60_H	*	*	*	1	2	3	4	97	$COMM_1$ Line and Both besides of 1st Line (COM_1,COM_3,COM_5,COM_7)
0110 0001	61_H	*	*	*	5	6	7	8	98	
⋮	⋮									
0110 0101	65_H	*	*	*	21	22	23	24	102	
0110 0110	66_H	*	*	*	*	*	*	*	103	
0110 0111	67_H	*	*	*	*	*	*	*	104	
0110 1000	68_H	*	*	*	25	26	27	28	105	$COMM_2$ Line and Both besides of 2nd Line (COM_9,COM_{11},COM_{13},COM_{15})
0110 1001	69_H	*	*	*	29	30	31	32	106	
⋮	⋮									
0110 1101	$6D_H$	*	*	*	45	46	47	48	110	
0110 1110	$6E_H$	*	*	*	*	*	*	*	111	
0110 1111	$6F_H$	*	*	*	*	*	*	*	112	
0111 0000	70_H	*	*	*	49	50	51	52	113	$COMM_3$ Line and Both besides of 3rd Line (COM_{17},COM_{19},COM_{21},COM_{23})
0111 0001	71_H	*	*	*	53	54	55	56	114	
⋮	⋮									
0111 0101	75_H	*	*	*	69	70	71	72	118	
0111 0110	76_H	*	*	*	*	*	*	*	119	
0111 0111	77_H	*	*	*	*	*	*	*	120	
0111 1000	78_H	*	*	*	73	74	75	76	121	$COMM_4$ Line and Both besides of 4th Line (COM_{25},COM_{27},COM_{29},COM_{31})
0111 1001	79_H	*	*	*	77	78	79	80	122	
⋮	⋮									
0111 1101	$7D_H$	*	*	*	93	94	95	96	126	
0111 1110	$7E_H$	*	*	*	*	*	*	*	127	
0111 1111	$7F_H$	*	*	*	*	*	*	*	128	

Notes : 1. When the Icon display function using, the system should be initialized by the software initialization Because the MK RAM is not initialized by the power on reset and hardware.

2. The cross-points between segments ($SEGM_1$ and $SEGM_2$) and commons ($COMM_1$ to $COMM_4$ and COM_2 to COM_{32}) are always set "OFF" level.

3. In the table 4, * mark are invalid, therefore both of "0" or "1" can be written but these are no meaning.

(1-7) Timing generator

The timing generator generates a timing signals for the DD RAM, CG RAM and MK RAM and other internal circuits. RAM and timing for the display and internal operation timing for MPU access are separately generated, so that may not interfere with each other.

Therefore, when the data write to the DD RAM for example, there will be undesirable influence, such as flickering, in areas other than display area.

(1-8) LCD Driver

LCD Driver consists of 37-common driver and 63-segment driver. The character pattern data are latched to the addressed segment-register respectively.

This latched data controls display driver to output LCD driving waveform.

(1-9) Cursor Blinking control circuit

This circuit controls cursor On / Off and cursor position character blinking. The cursor or blinking appear in the digit locating at the DD RAM address set in the address counter (AC). When the address counter is $(08)_H$, a cursor position is shown as bellow.

	AC_6	AC_5	AC_4	AC_3	AC_2	AC_1	AC_0
AC	0	0	0	1	0	0	0

4-Line Display

	1	2	3	4	5	6	7	8	9	10	11	12	←Display position
1st Line	00	01	02	03	04	05	06	07	08	09	0A	0B	← DD RAM Address (Hexadecimal)
2nd Line	10	11	12	13	14	15	16	17	18	19	1A	1B	
3rd Line	20	21	22	23	24	25	26	27	28	29	2A	2B	
4th Line	30	31	32	33	34	35	36	37	38	39	3A	3B	

Cursor position

Note : The cursor or blinking also appear when the address counter (AC) selects the CG RAM or the MK RAM. But the displayed cursor and blinking are meaningless.
If the AC stores the CG or MK RAM address data, the cursor and blinking are displayed in the meaningless position.

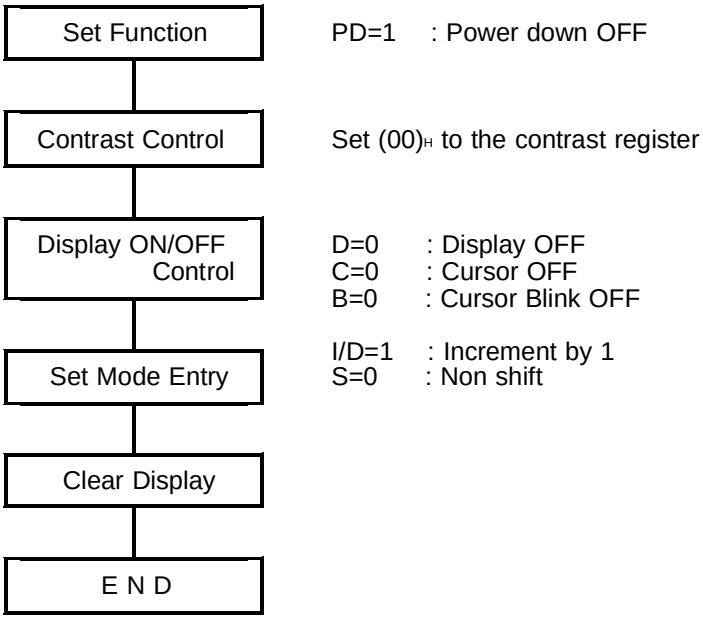
(2) Power on Initialization by internal circuits

(2-1) Internal Reset circuits Initialization

The NJU6475B is automatically initialized by internal power on initialization circuits when the power is turned on. In the internal power on initialization, following instructions are executed.

During the Internal power on initialization, the busy flag (BF) is "1" and this status is kept during 6ms (f_{OSC}=180KHz) after V_{DD} rose to 2.4V.

Initialization sequence



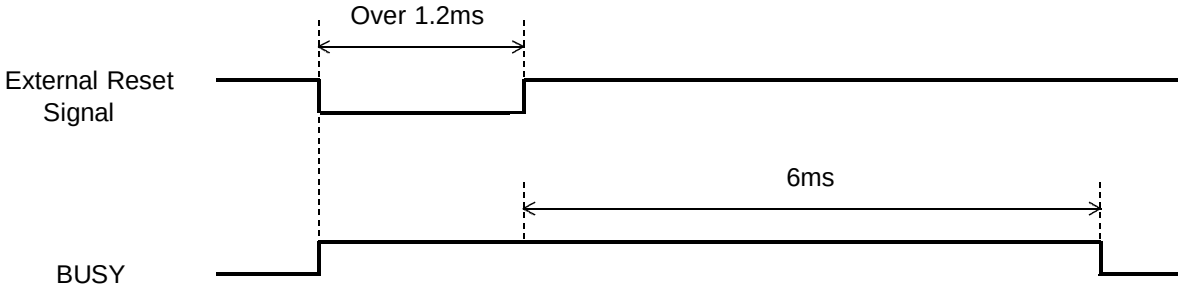
Note : If the condition of power supply rise time described in the Electrical Characteristics is not satisfied, the internal Power On Initialization will not performed.
In this case, the software initialization by MPU is required.

(2-2) Hardware Initialization

The NJU6475B prepares RESET terminal to initialize the all system.

When the "L" level is input over 1.2ms to the RESET terminal, reset sequence is executed. In this time, the busy signal is output during 6ms (f_{OSC}=180KHz) after RESET terminal went to "H".

-Timing Chart



(3) Instruction

The NJU6475B incorporates two registers, an Instruction Register (IR) and a Data Register (DR). These two registers store control information temporarily to allow interface between NJU6475B and MPU or peripheral IC operating different cycles. The operation of NJU6475B is determined by this control signal from MPU.

The control information includes resister selection signals (RS), Read / Write signals (R/W) and data signal (SIO).

<Table-5> shows each instruction and its operating time

Instruction	Code										Description	Execute Time (f_{CP} or f_{OSC} (MAX) =180kHz)
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
Maker Test	0	0	0	0	0	0	0	0	0	0	All "0" code is using for maker testing.	-
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears Display and sets RAM address $(00)_H$ in AC.	5.42ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets RAM address $(00)_H$ in AC and returns shifted display to original position. RAM contents are not changed	83.4us
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	sets cursor move direction and display shift operation which are performed at data read/write.	0us
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set Display Control On /Off (D), cursor On /Off (C) and character blinking (B) at cursor position.	0us
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	moves cursor and shifts display without changing RAM(DR) contents.	Cursor : 83.4us Display : 0us
Function Set	0	0	0	0	1	*	*	*	*	PD	Sets Interface data length (DL) and power down mode (PD).	0us
Electronic Volume Register Set	0	0	0	1	*	*	Electronic volume				Sets Vreg data to EVR control register.	0us
RAM Address Set	0	0	1	Address							Sets RAM Address. After this instruction, the data is transferred to/from RAM.	83.4us
Key Data Read	0	1	Read Data (KEY DATA)								When LCD/Key= "1", reads key data out.	0us
Data Write to CG or DD or MK RAM	1	0	Write Data (DD RAM)								Writes data into DD or CG or MK RAM.	83.4us
			*	*	*	(CG RAM)						
						(MK RAM)						
* : Don't care	I/D=1:Increment, I/D=0:Decrement, S=1:Include Display Shift, S/C=1:Shift Display, S/C=0:Cursor shift, R/L=1:Shift to Right, R/L=1:Shift left, PD=0:Power Down Mode PD=1:Cancel Power Down Mode										DD RAM : Display data RAM CG RAM : Character generator RAM MK RAM : Icon display RAM AC : Address counter use for DD, CG and MK RAM	When FRQ is changed, the execute time is also changed.

Note : If the oscillation frequency is changed, the execution time is also changed.

(3-1) Description of each instructions

(a) Maker Test

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	0	0

(b) Clear Display

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	0	1

Clear Display Instruction is executed when the code "1" is written into DB_0.

When this instruction is executed, the space code $(20)_H$ is written into every DD RAM address, then the DD RAM $(00)_H$ is set into address counter and I/D of entry mode is set as increment mode. If the cursor or blink are displayed, they are returned to the left end of the 1st line on the LCD panel.

In addition, S of entry mode is not changes and contents of MK RAM and CG RAM are also not changed.

Note : The character code $(20)_H$ must be blank code in the user defined character pattern (Custom font).

(c) Return Home

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	0	0	0	0	0	0	0	0	1	*	*= Don't Care

Return Home instruction is executed when the code "1" is written into DB_1.

When this instruction is executed, the DD RAM address $(00)_H$ is set into the address counter. Display is returned to its original position if shifted, the cursor or blink are returned to the left end of the 1st line on the LCD if the cursor or blink are operating. The DD RAM contents do not change.

(d) Entry Mode Set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

Entry Mode Set instruction which sets the cursor moving direction and display shift On/Off, is executed when the code "1" is written into DB_2 and codes of (I/D) and (S) are written into DB_1 (I/D) and DB_0 (S). (I/D) sets the address increment or decrement, and the (S) sets the entire display shift at the DD RAM writing.

I/D	F u n c t i o n
1	Address increment : The address of the DD RAM or CG RAM increment (+1) when the read/write operation, and the cursor or blink moves to the right.
0	Address decrement : The address of the DD RAM or CG RAM decrement (-1) when the read/write operation, and the cursor or blink moves to the left.

S	F u n c t i o n
1	Entire display shift. The shift direction is determined by I/D. : shift to left at I/D=1 and shift to the right at the I/D=0. The shift is operated only for the character, so that it looks as if the cursor stands still and display moves. The display does not shift when reading from DD RAM and writing/reading into/from CG RAM.
0	The display does not shift.

(e) Display ON/OFF Control

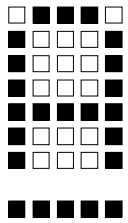
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	1	D	C	B

Display ON/OFF control instruction which controls the whole display ON/OFF, the cursor ON/OFF and the cursor position character blink, is executed when the code "1" is written into DB_3 and codes of (D), (C) and (B) are written into DB_2(D), DB_1(C) and DB_0(B), as shown below.

D	Function
1	Display On
0	Display Off. In this mode, the display data remains in the DD RAM so that it is retrieved immediately on the display when the D changes to 1.

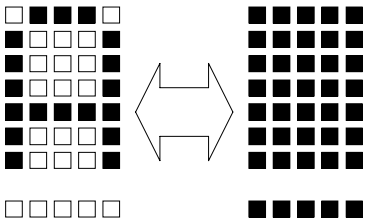
C	Function
1	Cursor On. The cursor is displayed by 5 dots on the 8th line.
0	Cursor Off. Even if the display data write, the I/D etc does not change.

B	Function
1	The cursor position character is blinking. Blinking rate is 480ms at f_{OSC}=180KHz. The cursor and the blink can be displayed simultaneously.
0	The character does not blink.



Character Font 5×7 Dots

(1) Cursor Display Example



Alternating Display

(2) Brink Display Example

(f) Cursor Display Shift

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	1	S/C	R/L	*	*

*= Don't Care

The cursor /display shift instruction shifts the cursor display to the right or left without writing or reading display data. This function is used to correct or search the display. The cursor moves to the 2nd line after the 12nd digit of the 1st line. Notice that 1st to 3rd line displays shift at the same time. When the displayed data are shifted repeatedly, each display moves in only same line. The 2nd and 3rd line display do not shift into the 1st and 2nd line.

The contents of address counter (AC) does not change by operation of only the display shift.

This instruction is executed when the code "1" is written into DB_4 and the codes of (S/C) and (R/L) are written into DB_3(S/C) and DB_2(R/L), as shown below.

S/C	R/L	Function
0	0	Shift the cursor position to the left ((AC) is decremented by 1).
0	1	Shift the cursor position to the right ((AC) is incremented by 1).
1	0	Shifts the entire display to the left and the cursor follows it.
1	1	shifts the entire display to the right and the cursor follows it.

(g) Function Set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	0	0	0	0	1	*	*	*	*	PD	*= Don't Care

Function set instruction which sets the interface data length and power down is executed, when the code "1" is written into DB_5 and (PD) is written into DB_0, as shown below.

When the power down mode is set, the display turns off automatically. Afterward, when the power down mode is reset, the display is off continuously.
The display appears by the display on instruction.

PD	Function
1	Power down mode off (Normal operation)
0	Power down mode on (the display goes to off automatically.)

(h) Set Electronic Volume Register

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	0	0	0	1	*	*	C_3	C_2	C_1	C_0	*= Don't Care
					← Higher order bit		→	← Lower order bit			→

Contrast Control instruction which adjusts the contrast of LCD, is executed when the code "1" is written into DB_6 and the codes of C_0 to C_3 are written into DB_0 to DB_3 as shown below.
The contrast of LCD can be adjusted one of 16 voltage stage by setting 4 bit register.
Set the binary code "0000" when contrast control unused.

C_3	C_2	C_1	C_0	V_{LCD}
0	0	0	0	low
	:			
	:			
1	1	1	1	high

$V_{LCD} = V_{DD} - V_5$

(i) Set RAM Address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	1	A	A	A	A	A	A	A

← Higher order bit → ← Lower order bit →

The RAM address set instruction is executed when the code "1" is written into DB_7 and the address is written into DB_6 to DB_0 as shown above.

The address data (DB_6 to DB_0) is written into the address counter (AC) by this instruction.

After this instruction execution, the data writing/reading is performed into/from the addressed RAM.

The RAM includes DD RAM, CG RAM and MK RAM and these RAMs are shared by addressed as shown below.

			RAM Address
DD RAM	1st Line	:	$(00)_H$ to $(0B)_H$
DD RAM	2nd Line	:	$(10)_H$ to $(1B)_H$
DD RAM	3rd Line	:	$(20)_H$ to $(2B)_H$
DD RAM	4th Line	:	$(30)_H$ to $(3B)_H$
CG RAM	4 Characters	:	$(40)_H$ to $(5F)_H$
MK RAM	128 Icons	:	$(60)_H$ to $(7F)_H$

(j) Write Data to CG, DD or MK RAM

-Write Data to DD RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	D	D	D	D	D	D	D	D

← Higher order bit → ← Lower order bit →

-Write Data to CG or MK RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	1	0	*	*	*	D	D	D	D	D	*= Don't Care

← Higher order bit → ← Lower order bit →

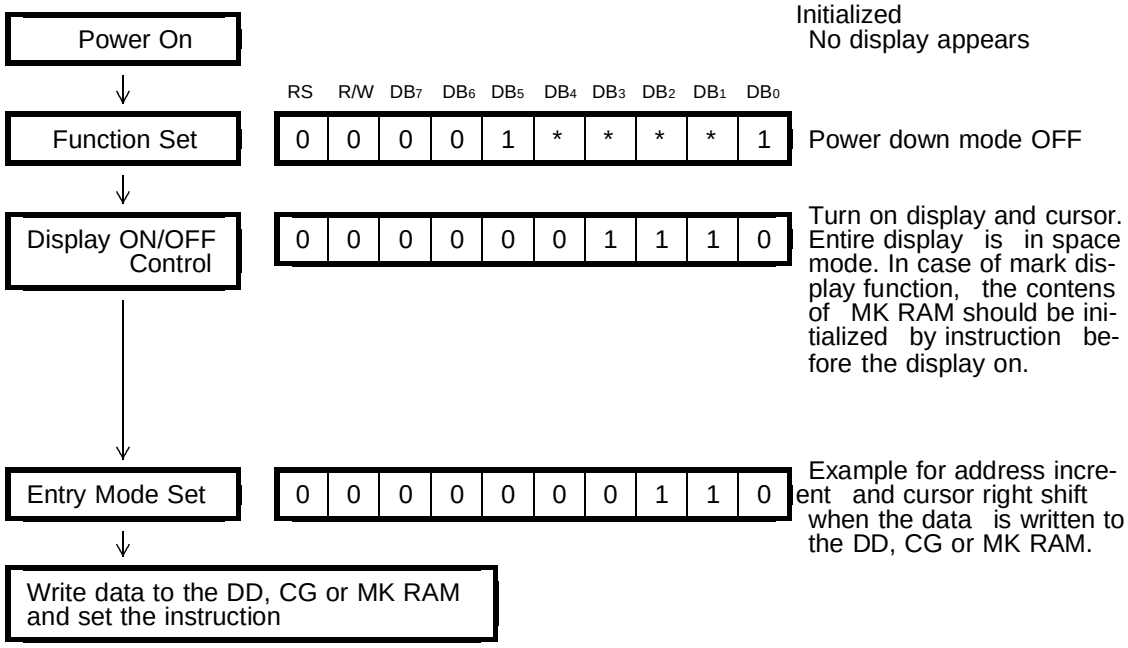
Write Data to RAM instruction is executed when the code "1" is written into (RS) and code "0" is written into (R/W).

By the execution of this instruction, the data is written into RAM. The selection of RAM is determined by the previous instruction.

After this instruction execution, the address increment (+1) or decrement (-1) is performed automatically according to the entry mode set.

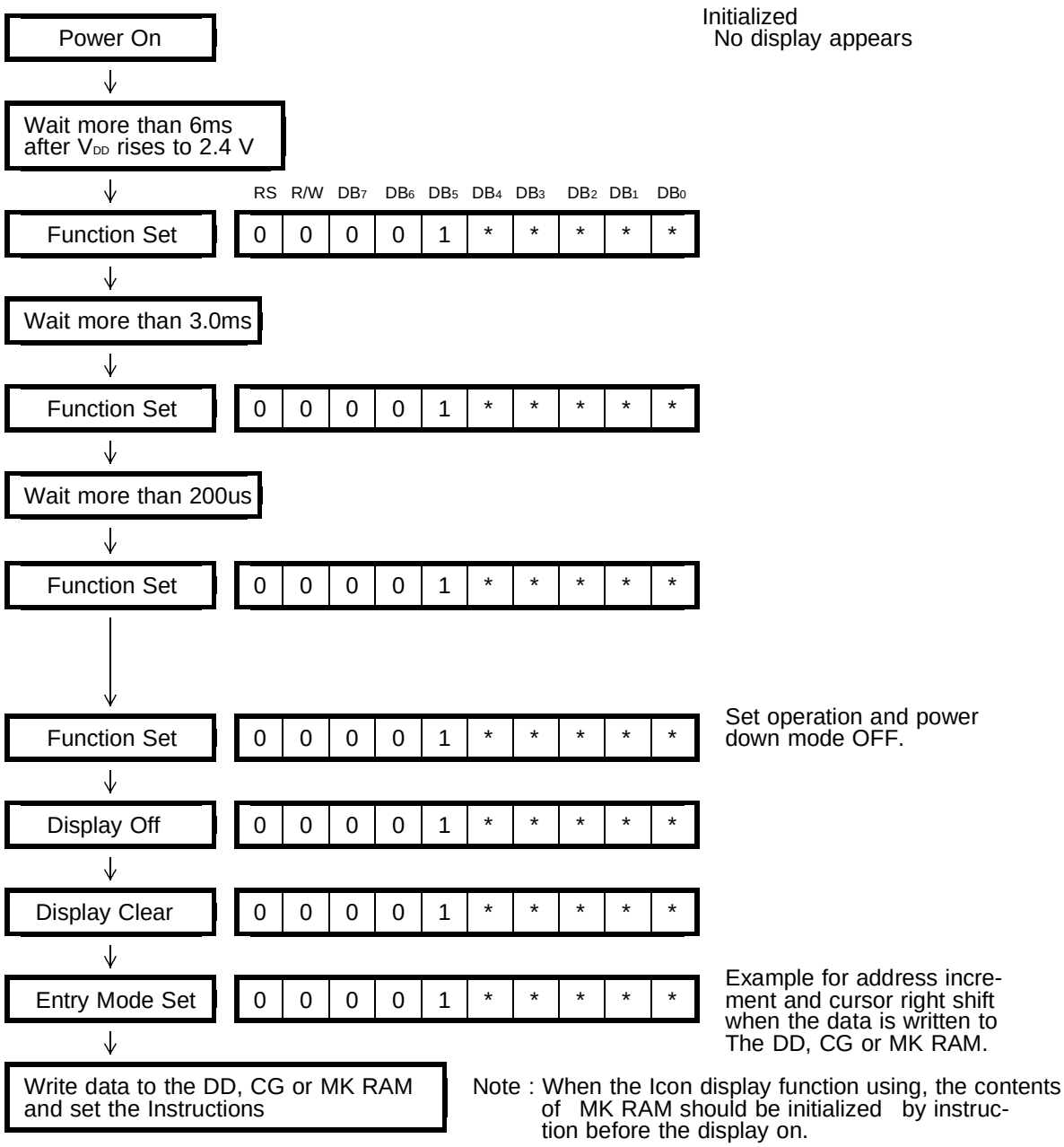
(3-2) Initialization using the internal reset circuit

When internal reset operates for initialization, the function set, Display ON/OFF Control and Entry Set instruction must be executed before the data input as shown below.



(3-3) Initialization by instruction

If the power supply conditions for the correct operation of the internal reset circuits are not met, the NJU6475B must be initialized by instruction.



Note : When the Icon display function using, the contents of MK RAM should be initialized by instruction before the display on.

(4) Power down Function

NJU6475B incorporates the power down mode to reduce the operating current.
The power down mode is set/reset by the function set instruction.
In the power down mode, all the character display and Icon display turn off and only static display operation is available.
The status of internal circuits at the power down mode is shown below.

-Main oscillator stops and sub oscillator for the static display starts the operation.
-Voltage converter, Key Scan, Voltage Regulator, Voltage follower (OP-AMP) are stopped.
-The contents of DD, CG, MK RAM are kept.

(5) LCD Display

(5-1) Power Supply for LCD Driving

NJU6475B incorporates voltage converter to generate the LCD driving voltage which is adjusted by the voltage regulater and the EVR.

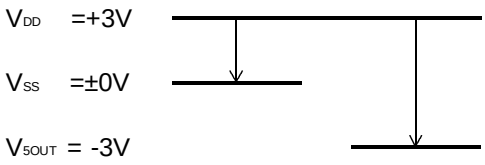
(a) Voltage Converter

-Voltage Tripler

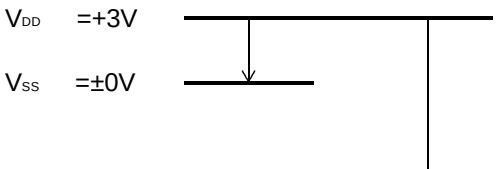
By connecting capacitor between $C1^+$ and $C1^-$, $C2^+$ and $C2^-$, V_{SS} and V_{5OUT} respectively, two times negative voltage of V_{DD}--V_{SS} output from V_{5OUT}.

-Voltage Doubler

By connecting capacitor between $C2^+$ and $C2^-$, V_{SS} and V_{5OUT} respectively, and connecting the $C1^+$ terminal to $C2^+$ terminal, and $C1^-$ terminal being open, negative voltage of V_{DD}--V_{SS} output from V_{5OUT}.



Voltage Doubler



Voltage Tripler

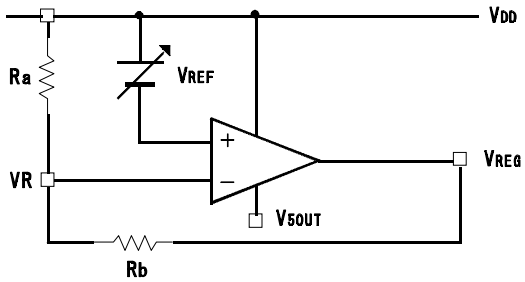
(b) Voltage Regulator

Voltage Regulator incorporates a OP-AMP which is supplied V_{DD} and V_{5OUT}, and a reference voltage source (V_{REF}).

By setting the VR level by connecting Ra and Rb, the regulator which amplifies V_{REF}, outputs the LCD driving voltage to the V_{REG} terminal.

Therefore the LCD driving voltage can be output between V_{DD} and V_{REG} by setting.

$V_{REG} = (1+ Rb / Ra) V_{REF}$ in condition, $V_{DD} = 0V$, $|V_{REG}| < |V_{5OUT}|$



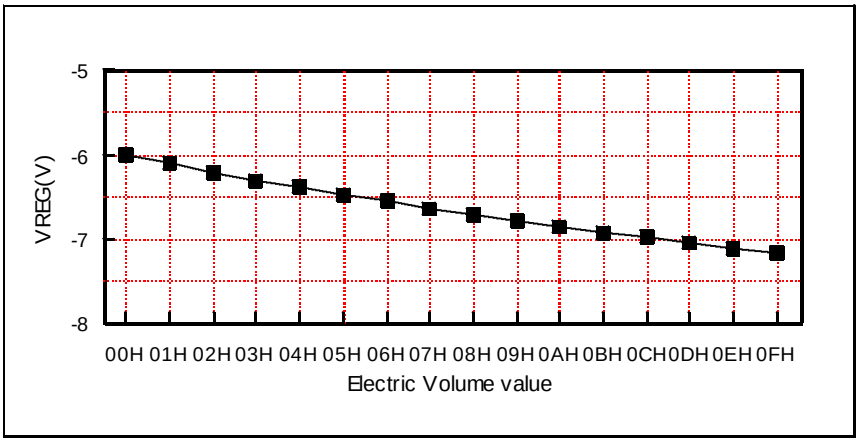
The EVR functions V_{REF} value adjustment from 1st step to 16th by a step when the 4 bit data write into the EVR register by the instruction.

Set the EVR register to $(00)_H$ when the EVR function is unused. Use variable resistances to external to the external resistances Ra, Rb and thermistor if need due to the voltage reference V_{REF} is changed by the lot and operating temperature.

Take care the noise input on the VR terminal because of it is designed with high impedance. Short wiring should be required to avoid the noise input, if necessary.

[The Voltage Reference V_{REF} Characteristics]

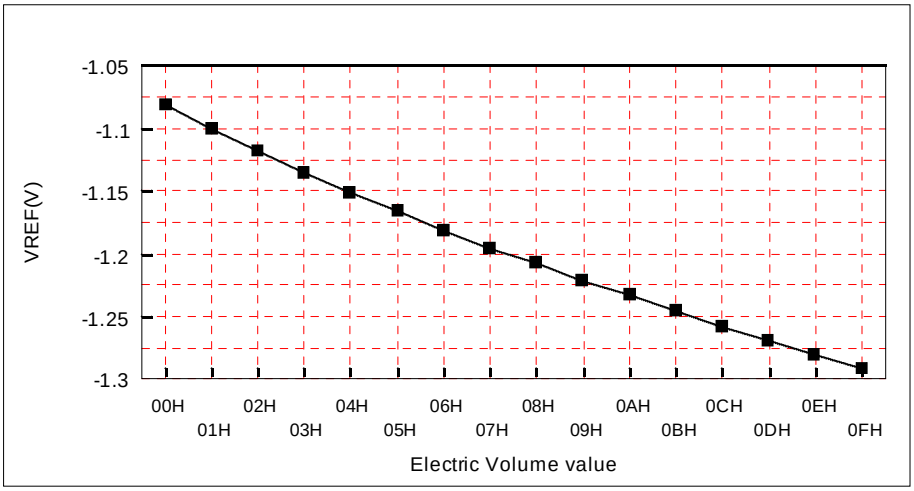
Supply Voltage : V_{DD} = 0V, V_{SS} = -3V Temperature : 25 °C



[The LCD Operating Voltage V_{REG} Characteristics]

Supply Voltage : V_{DD} = 0V, V_{SS} = -3V, Voltage Tripler Output : V_{5OUT} = -9V
External Resistances : Ra = 180KΩ, Rb = 820KΩ Temperature : 25 °C

Used Formulation : $V_{REG}(XX)_H = (1 + 820k\Omega/180k\Omega)\ V_{REF}(XX)_H$



(c) Bleeder Resistance

Each LCD driving voltage (V_1, V_2, V_3, V_4, V_5) is generated by the high impedance bleeder resistance buffered by voltage follower OP-AMP to get a enough display characteristics with low operating current. The bleeder resistance is set 1/7 bias suitable for 1/36 duty by 5MΩ resistance in total.

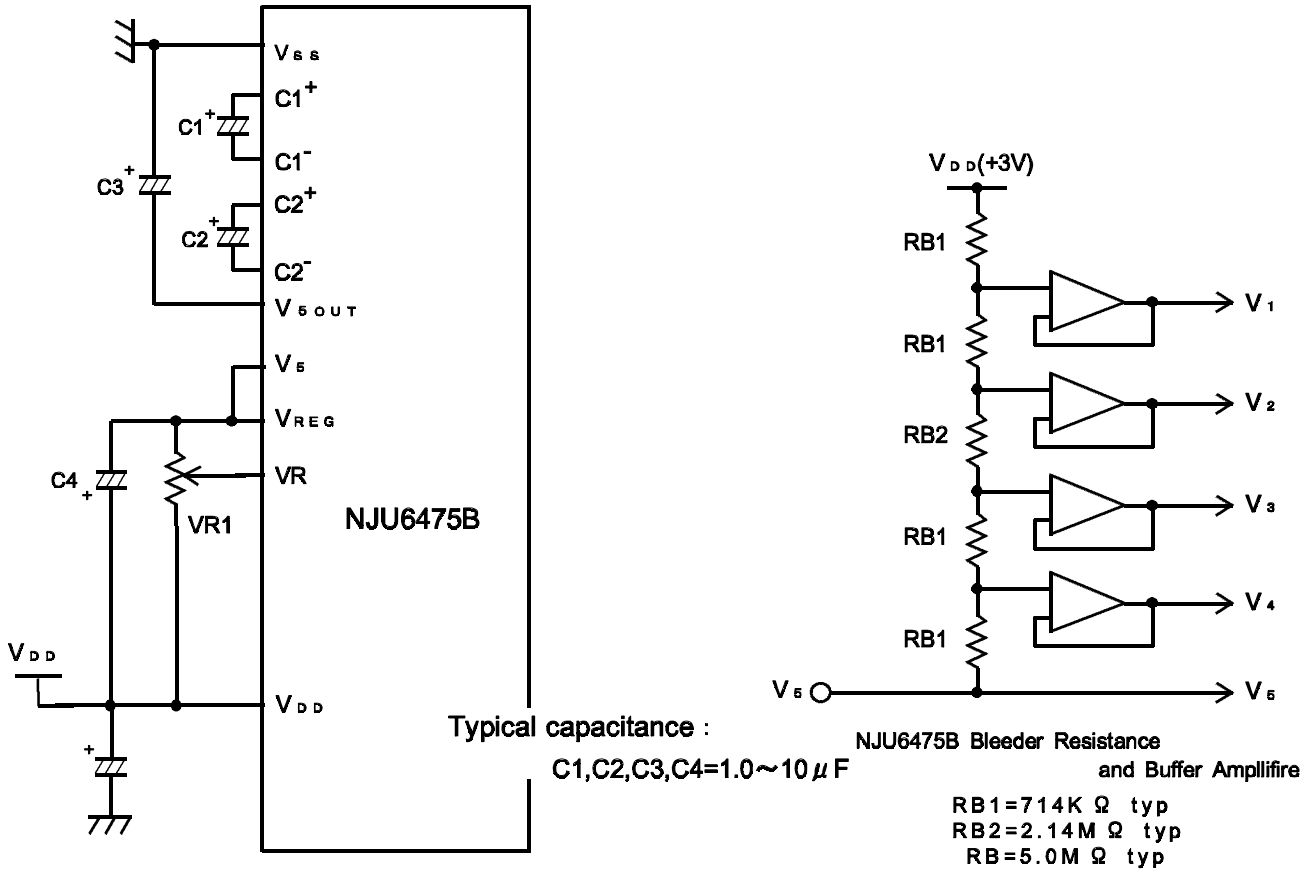
The capacitor connected between V_5 and V_{DD} is needed for stabilizing V_5. The determination of the each capacitance of C_1, C_2 and C_3 generating for LCD operating voltage is required to operate with the LCD panel actually.

The capacitance for the typical application is shown below:

LCD Driving Voltage vs Duty

Power	Duty Ratio	1/36
Supply	Bias	1/7
V_{LCD}		V_{DD} - V_5

V_{LCD} is the maximum amplitude for LCD driving voltage.



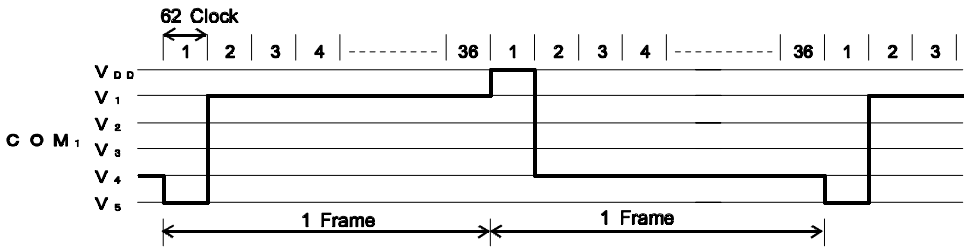
Typical application for LCD operating voltage generation

Note : Take care the noise into the VR terminal as designed with high impedance.
Short wiring or sealed wiring are required to avoid the noise, if necessary.

(5-2) Relation between oscillation frequency and LCD frame frequency

As the NJU6475B incorporates oscillation capacitor and resistor for CR oscillation, 180KHz oscillation is available without any external components. (1 Clock = 5.56us)

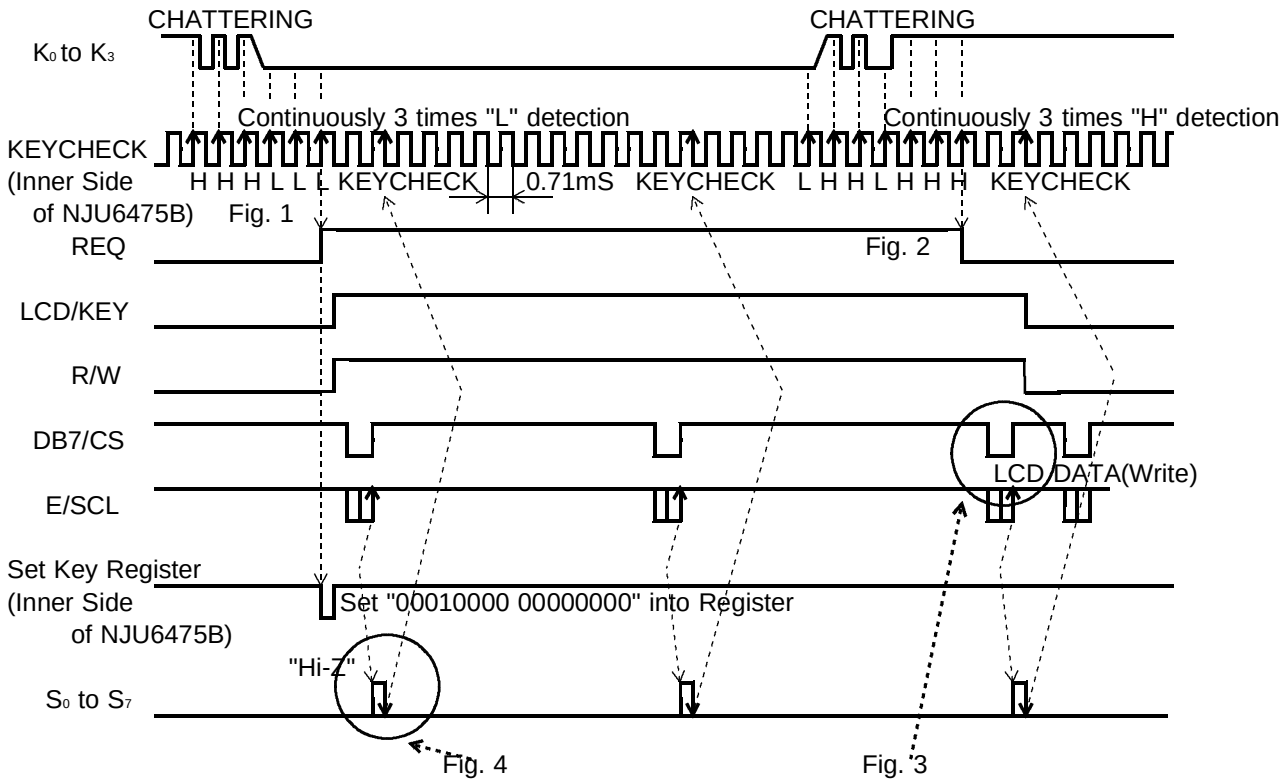
1/36 Duty



1 frame = 5.56 (us) x 62 x 36 = 12.4 (ms)
Frame frequency = 1 / 12.4 (ms) = 80.6 (Hz)

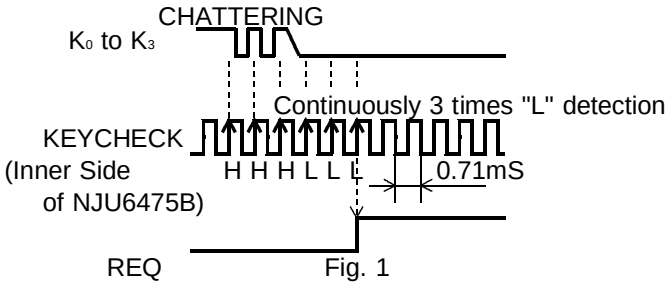
(6) Key Scan Circuit

(6-1) Key scan timing chart

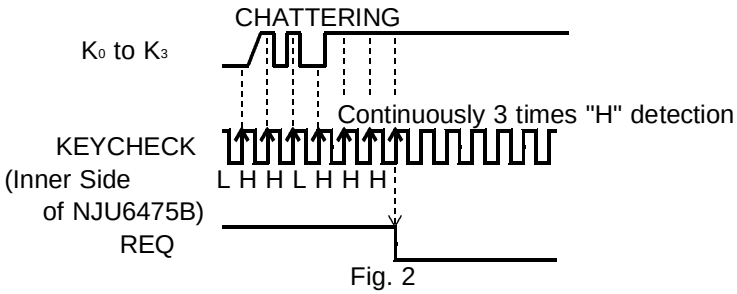


(6-2) Key Scan

1. KEYCHECK signal always operates to check the status of keys excepting for power down mode.
2. When Key signal (K_0 to K_3) 3 times detected continuously at rise up edge of KEYCHECK (inner side NJU6475), key Scan circuit performs output request signal (REQ terminal) rise to "H" and simultaneously key input information transmit to CPU. Its useful for anti-chattering. At the same time of REQ signal output, the key register status is "00010000 00000000" (Non Key Input) automatically. Key input terminal (K_0 to K_3) are "H" in normal, then turn to "L" when Key input.



In case of request signal "H", When detects 3 times continuously key released status, request signal will be "L".



3. When the request signal is detected, CPU should be LCD / KEY to "H" and read out key data by instruction. 16-bit key data synchronizing to "SCL" (SCL terminal) is read out to CPU.
   (1st time output key data was fixed as "00010000 00000000")
   keyscan operation start from the next rising edge of SCL after the end of key data read out opration.

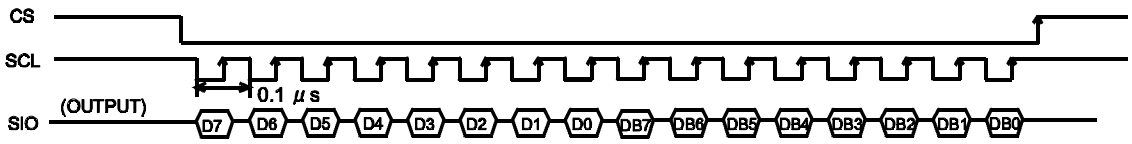


Fig. 3

4. The key data are gotten from 4 terminals (K_0 to K_3) at each timing of key scan signals (S_0 to S_7).
   The detected data are up dating anytime and stores to key register.

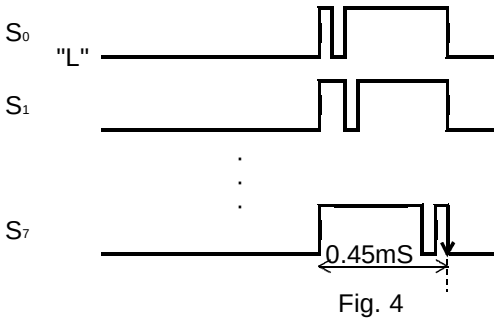
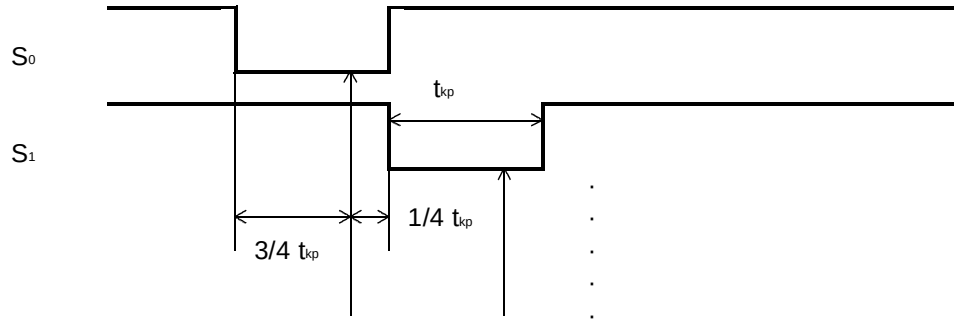


Fig. 4 End of Key Scan

- Key scan timing : 0.45ms (fosc = 180KHz,MAX =0.64ms)
- Pulth width : 45us (fosc = 180KHz, MAX =64us)

(6-3) Key scanning timing

Key status is gotten at 3/4 port timing of t_{kp} during "L" period of S_0 to S_7.



Detecting timing

(6-4) The format of detection

1st Byte

MSB							LSB
0	0	0	1	K_{L3}	K_{L2}	K_{L1}	K_{L0}

Fix

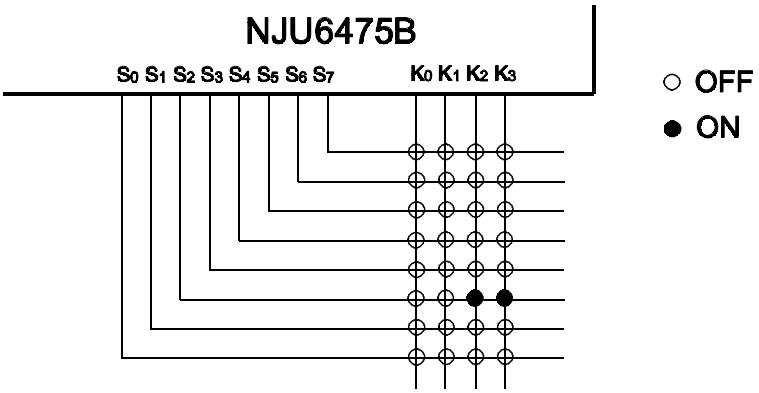
K_{L3} to K_{L0} : Corresponds to K_3 to K_0

2nd Byte

MSB							LSB
K_{H7}	K_{H6}	K_{H5}	K_{H4}	K_{H3}	K_{H2}	K_{H1}	K_{H0}

K_{H7} to K_{H0} : Corresponds to S_7 to S_0

(For Example)



1st Byte

MSB							LSB
0	0	0	1	1	1	0	0

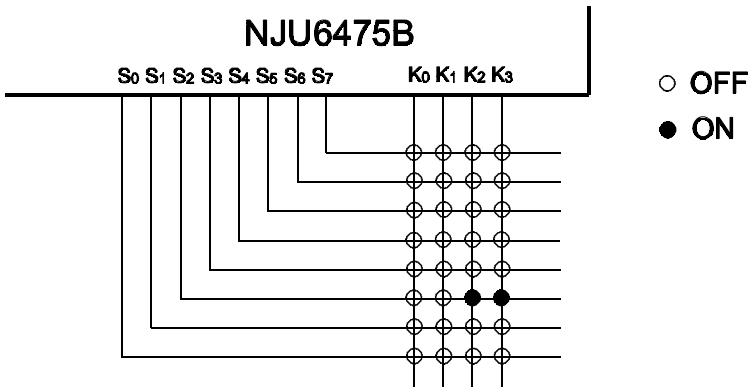
2nd Byte

MSB							LSB
0	0	0	0	0	1	0	0

(6-5) Key roll over input

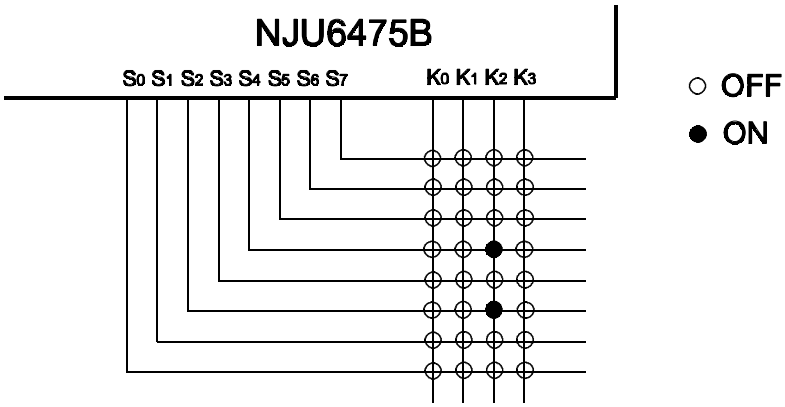
NJU6475B can be accepted the key roll over input.
In case of key roll over input, the output results are shown below;

-Connecting same S_x signal line at multiple key push.



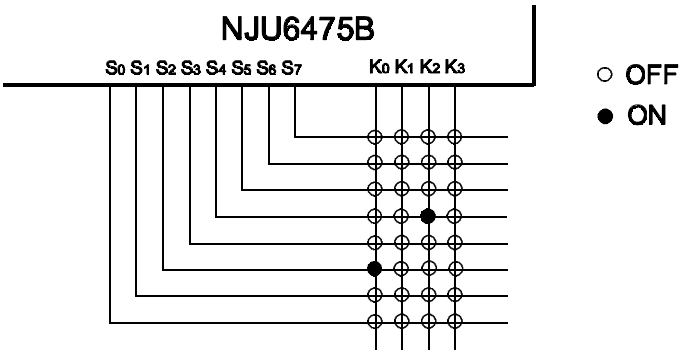
When key-in shown above case, the data contents are "00011100" "00000100".

-The case of connecting different S_x signal line at multiple key push (1)



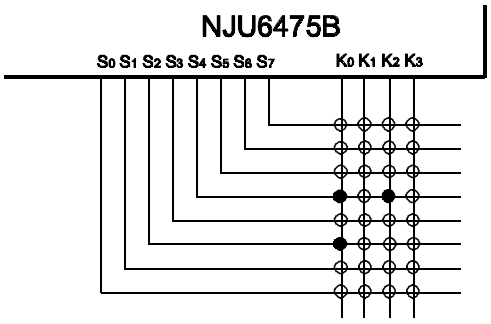
When key-in shown above case, the data contents are "00010100" "00010100".

-The case of connecting different S_x signal line at multiple key push (2)

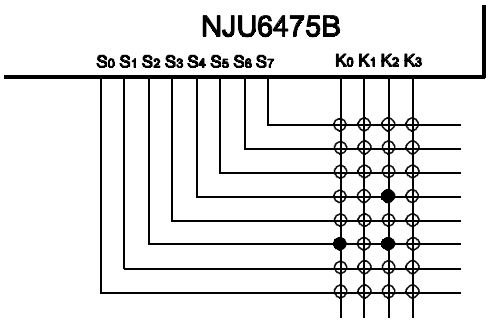


When key-in like as shown above, the data contents are "00010101" "00010100".
In this case, the result will be same, at each key-in shown below.

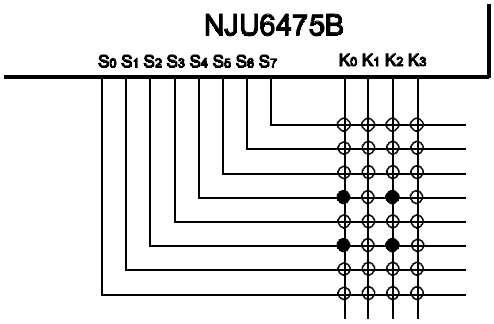
[Case 1]



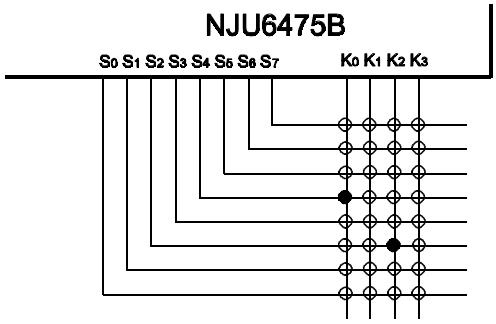
[Case 2]



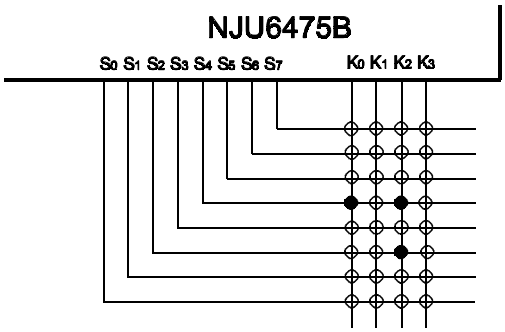
[Case 3]



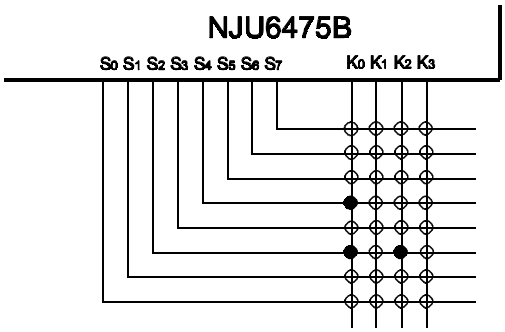
[Case 4]



[Case 5]

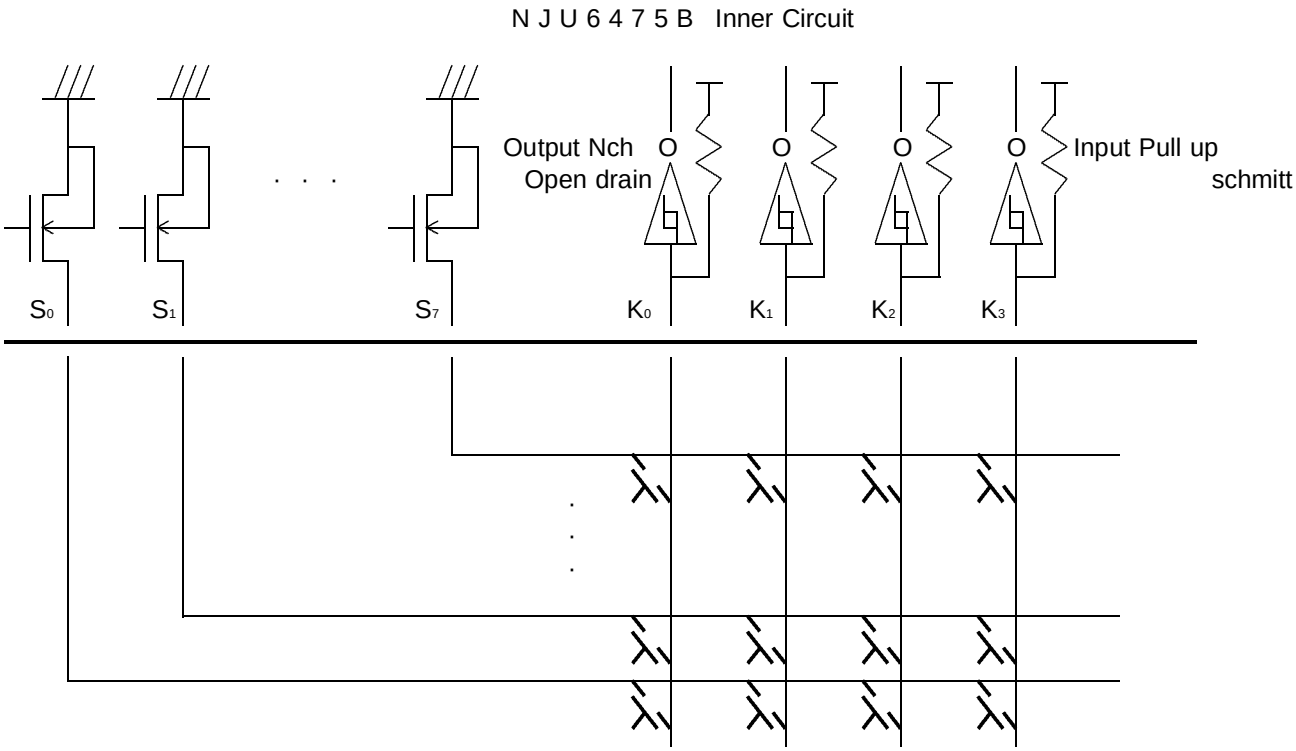


[Case 6]



(6-6) The inner composition of Key Scan circuit

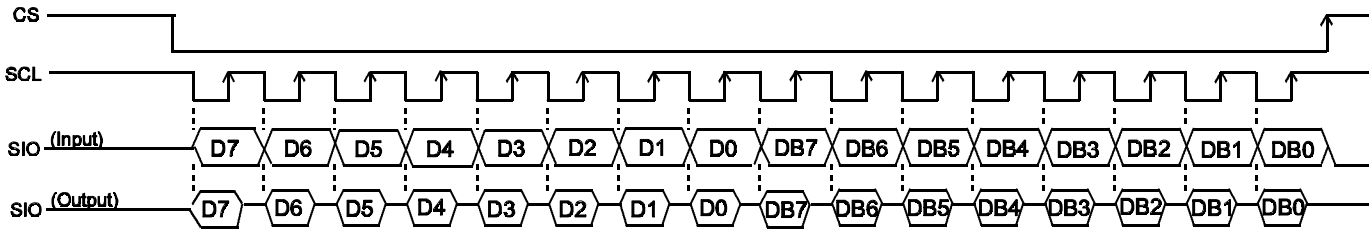
The inner composition of key scan circuit shown below :



-In case of non input the key each terminal status shown below:
S_0 to S_7 : The status of Nch FET output side is ON, output result is "L".
K_0 to K_3 : The status is "H" by pull-up resistance.
-When any key key-in, K_x of key-in side turn to "L" and it can confirms.
-Input terminal (K_0 to K_3) are composed by schmitt inverter input method.

(7) Interface with MPU

Interface circuit of NJU6475B can be connected to serial by turn to "L" P/S terminal on shown below serial data timing. And DB_0 to DB_5 can be use to output port.



Notes : RS, R/W, LCD/KEY requires setting before CS fall down.
RS is unrelated to read out of key data and writing of port data.

Serial interface circuit is in operation at CS is "L".
When SCL rises, input data was lead, and rises CS case loading input data.
When the input data was less than 16 bits, input data will be invalid at rises CS. And so on equal or over than 16 bits case, rear side total 16 bits are effectiveness. The input data should be total 16 bits.
The data of read/write are composed MSB first.

-Data format

The data formatted by 2 byte form at read/write.
When writing data consists LCD data and port data.
The using data in write mode means one of key data.
In write mode of data format, 1st byte means recognition data of LCD data and Port data.
In "0110 0000" (fixed) selects LCD data, in "0110 0001" (fixed) selects Port data.
The data of 2nd byte consists each data contents.
When the 1st byte of MSB 4 bit data are not "0110", in this case the input data will be invalid.

				*	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	*
	LCD/ KEY	RS	R/W		1st Byte								2nd Byte								
LCD Data	0	0	0		Higher Selected Bit (0110)				Lower Selected Bit (0000)				LCD Data (Instruction)								Instruction Execution Time
LCD Data	0	1	0		Higher Selected Bit (0110)				Lower Selected Bit (0000)				LCD Data (RAM Data)								Instruction Execution Time
PORT Data	0	*	0		Higher Selected Bit (0110)				Lower Selected Bit (0001)				Output Port (Set "L"=0,"H"=1)								Instruction Execution Time
													*	*	DB5	DB4	DB3	DB2	DB1	DB0	
KEY Data	1	*	1		Selected Bit (0001)				Key Data 1				Key Data 2								
									KL3	KL2	KL1	KL0	KH7	KH6	KH5	KH4	KH3	KH2	KH1	KH0	

* : Invalid Data

Notes : The instruction requires execution time after transmit 16 bit data. After transmit data can not transmit continuously

■ MAXIMUM ABSOLUTE RATINGS

P A R A M E T E R	SYMBOL	R A T I N G S	UNIT	N O T E
Supply Voltage (1)	V_{DD}	- 0.3 ~ + 7.0	V	
Input Voltage	V_t	- 0.3 ~ V_{DD} + 0.3	V	
Operating Temperature	Topr	- 30 ~ + 80	°C	
Storage Temperature	Tstg	- 55 ~ + 125	°C	

Note-1 : If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note-2 : Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the voltage converter.

Note-3 : All voltage value are specified as V_{SS} = 0V.
The relation : $V_{DD} > V_{SS}$, $V_{DD} > V_{SS} \geq V_{5out}$, V_{SS} = 0V must be maintained.

■ ELECTRICAL CHARACTERISTICS (V_{DD} = 2.4 ~ 3.6V, Ta = -20 ~ +75 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input Voltage 1	V_{IH1}	(OSC1, Except terminals K_0 ~ K_3)	$0.8V_{DD}$	-	V_{DD}	V	4
	V_{IL1}	(OSC1, Except terminals K_0 ~ K_3)	V_{SS}	-	$0.2V_{DD}$	V	4
Input Voltage 2	V_{IH2}	(Application to terminals K_0 ~ K_3)	$0.8V_{DD}$	-	V_{DD}	V	4
	V_{IL2}	(Application to terminals K_0 ~ K_3)	V_{SS}	-	$0.2V_{DD}$	V	4
Input Voltage 3	V_{IH3}	(Applicate to terminal OSC1)	V_{DD}-0.5	-	V_{DD}	V	4
	V_{IL3}	(Applicate to terminal OSC1)	V_{SS}	-	0.5	V	4
Output Voltage 1	V_{OH1}	$-I_{OH}$ = 0.205mA, V_{DD} = 3.0V	2.0	-	-	V	5
	V_{OL1}	I_{OL} = 1.6mA, V_{DD} = 3.0V	-	-	0.5	V	5
Output Voltage (S_0 ~ S_7)	V_{OL2}	I_{OL} = 300uA	-	-	0.6	V	
Driver ON-resist (COM)	R_{COM1}	±I_d = 1uA (All COM Terminal) V_O = V_{DD}, V_5	-	-	20	kΩ	8
Driver ON-resist (SEG)	R_{SEG1}	±I_d = 1uA (All SEG Terminal) V_O = V_{DD}, V_5	-	-	30	kΩ	8
Driver Output-resist (COM)	R_{COM2}	±I_d = 1uA (All COM Terminal) V_O = V_1, V_4	-	-	40	kΩ	8
Driver Output-resist (SEG)	R_{SEG2}	±I_d = 1uA (All SEG Terminal) V_O = V_2, V_3	-	-	50	kΩ	8
Driver current	IV_1	V_1 Sink Current	-	-	-12.3	uA	
	IV_4	V_4 Source Current	16.8	-	-	uA	
Input Leak Current	ILI	V_{in} = 0 ~ V_{DD}	-1	-	1	uA	6
Pull-up MOS Current	-Ip	V_{DD} = 3V (ALL DB, K_0 ~ K_3 terminal)	10	25	50	uA	
Operating Current	I_{DD1}	f_{OSC} = Internal OSC on Display V_{DD} = 3V, On display, V_5 = -5V		320	380	uA	7
	I_{DD2}	f_{OSC} = Internal OSC on Display V_{DD} = 3V,On access, t_{CYCE} = 5uS		-	640	uA	7
voltage converter Part — Output Voltage	V_{5OUT}	V_{DD} = 3V, Ta = 25°C, I_{OUT} 3 Times = 100uA	-4.6	-4.8		V	
voltage converter Part — Voltage Efficiency	V_{ef}	R_L = ∞ 3 Times	90.0	95.0		%	
LCD Drive Voltage	V_1	Ta = 25°C	2.44	2.57	2.70	V	
	V_2	V_{DD} = 3V	2.01	2.14	2.27		
	V_3	V_5 = 0V	0.73	0.86	0.99		
	V_4	Measured at COM/SEG terminal	0.30	0.43	0.56		
Bleeder Resistance R_B(V_{DD} - V_5)/IB I_B:Bleeder Resistance Cur. R_B : 5 Bleeder Resist	R_B	V_{DD} - V_5 = 3V		5.0		MΩ	
reg. — Output Voltage	V_{REG}	R_L = ∞, R_{RV}=1MΩ, V_{5OUT} = -10.8V	V_{DD}-10.8	-	V_{DD}-1.8	V	
reg. — Operating voltage	V_{5OUT}	V_{DD} Reference	V_{DD}-11	-	V_{DD}-3.6		
reg. — Reference Voltage	V_{REF}	V_{DD} Reference, Ta=25°C	V_{DD}-0.75	V_{DD}-1.05	V_{DD}-1.35		
Clock Oscillation Freq.	f_{OSC}	V_{DD} = 3V, Ta=25°C	125	180	235	kHz	
LCD Driving Voltage	V_{LCD}	V_{5OUT} Terminal, V_{DD} = 3V	V_{DD}-3	-	V_{DD}-13.5	V	9

Note-4 : Input/Output structure except LCD display are as shown below.

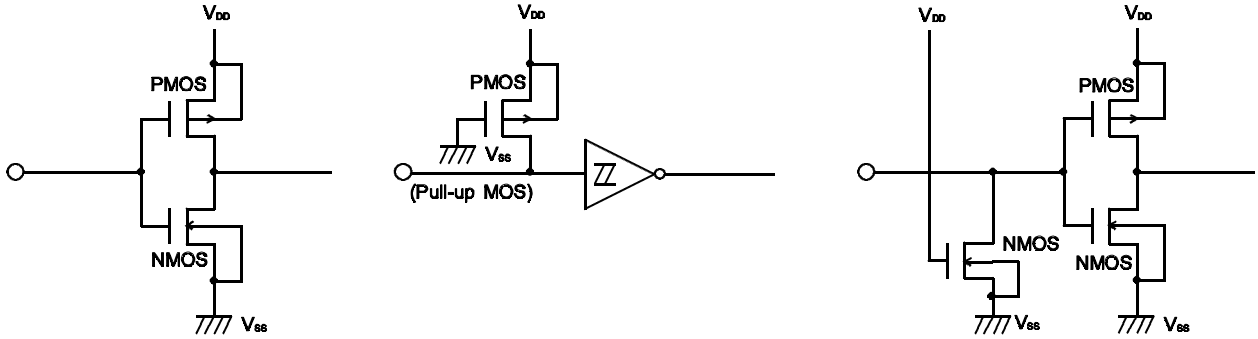
-Input terminal structure

(without pull-up MOS) (Pull-up with MOS, schmitt) (Pull down MOS)

Applicated terminals : E/SCL, RS, R/W, P/S, SEL, RESET, LCD/KEY

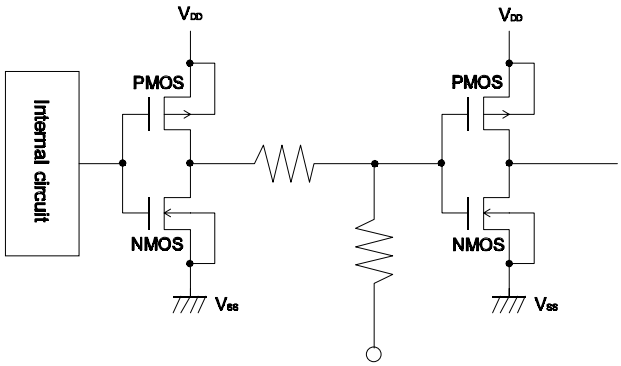
$K_0 \sim K_3$

TEST



-Input terminals structure

Applicated terminal : OSC1

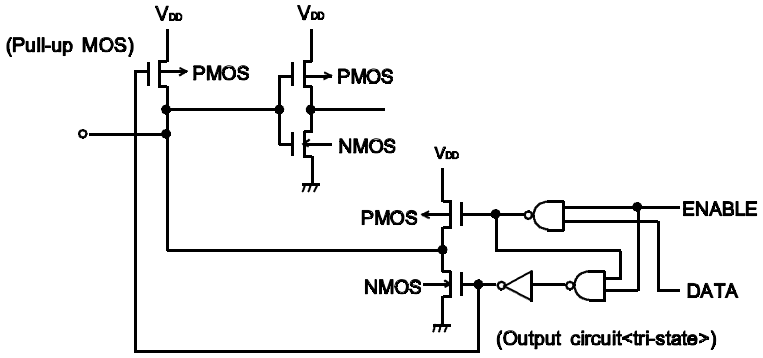


-Common terminals

Input/Output structure.

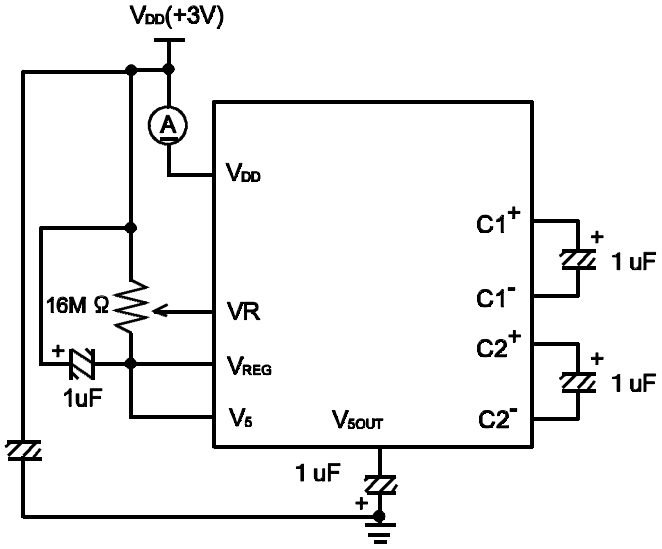
Applicated terminal

: DB_7 to DB_0



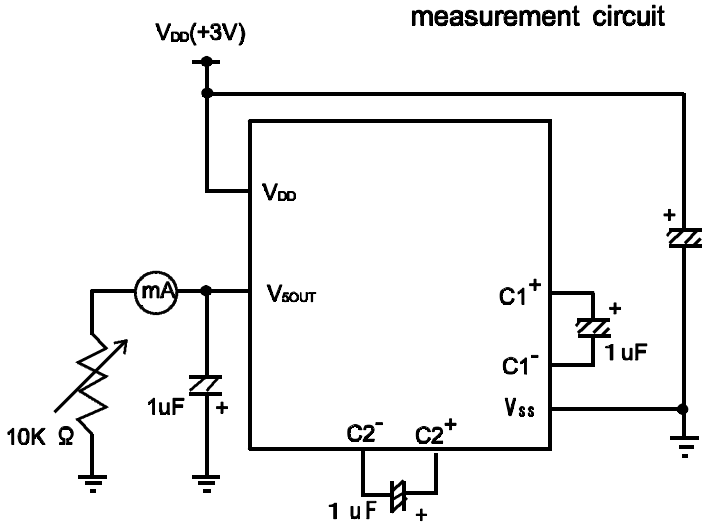
Note-5 : Apply to the output and Input/Output Terminals.
Note-6 : Except current of pull-up MOS and output drive MOS.
Note-7 : Except Input/Output part current but including the current on bleeder resistance.
If the input level is medium, current consumption will increase due to penetration current. therefore, the input level must be fixed to "H" or "L".

-Operating Current Measurement Circuit



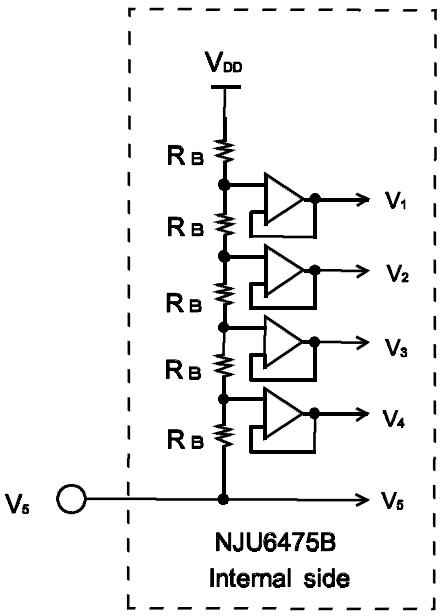
Note-8 : Rcom and Rseg are the resistance values between power supply terminals (V_{DD}, V_{5OUT}) and each common terminal (Com_1 to Com_{32} / $COMM_1$ to $COMM_4$) and Supply voltage (V_{DD}, V_{5OUT}) and each segment terminal (SEG_1 to SEG_{60} / $SEGM_1$ to $SEGM_2$) respectively, and measured when the current Id is flown on every common and segment terminals at same time.
Note-9 : Apply to the voltage from each COM and SEG are less than ±0.15V against the LCD driving contrast voltage (V_{DD}, V_{5OUT}) at no load condition.

Voltage converter characteristics measurement circuit



Voltage convering clock frequency =1 1 K H z(T Y P)

Internal bleeder resistance



■ BUS TIMING CHARACTERISTICS

-Serial Interface sequence

(V_{DD} = 2.4 ~ 3.6V, V_{SS} = 0V, Ta = -20 ~ +75°C)

PARAMETER		SYMBOL	MIN.	MAX.	CONDITION	UNIT
Serial clock cycle time		t_{CYCE}	1	-	Fig. 1	uS
Serial clock width	"High" level	t_{SCH}	300	-	Fig. 1	nS
	"Low" level	t_{SCL}	700	-	Fig. 1	nS
Serial clock rise and fall down time		t_{SCr}, t_{SCf}	-	20	Fig. 1	nS
Chip select pulse width		PW_{CS}	500	-	Fig. 1	nS
Chip select set up time		t_{CSU}	200	-	Fig. 1	nS
Chip select hold time		t_{CH}	300	-	Fig. 1	nS
Chip select rise and fall time		t_{CSr}, t_{CSf}	-	20	Fig. 1	nS
Set up time	RS, R/W, LCD/KEY-CS	t_{AS}	200	-	Fig. 1	nS
Address hold time		t_{AH}	200	-	Fig. 1	nS
Serial input data set up time		t_{SISU}	200	-	Fig. 1	nS
Serial input data hold time		t_{SIH}	200	-	Fig. 1	nS
Serial output data delay time		t_{SOD}	-	700	Fig. 1	nS
Serial output data hold time		t_{SOH}	200	-	Fig. 1	nS

Serial Interface

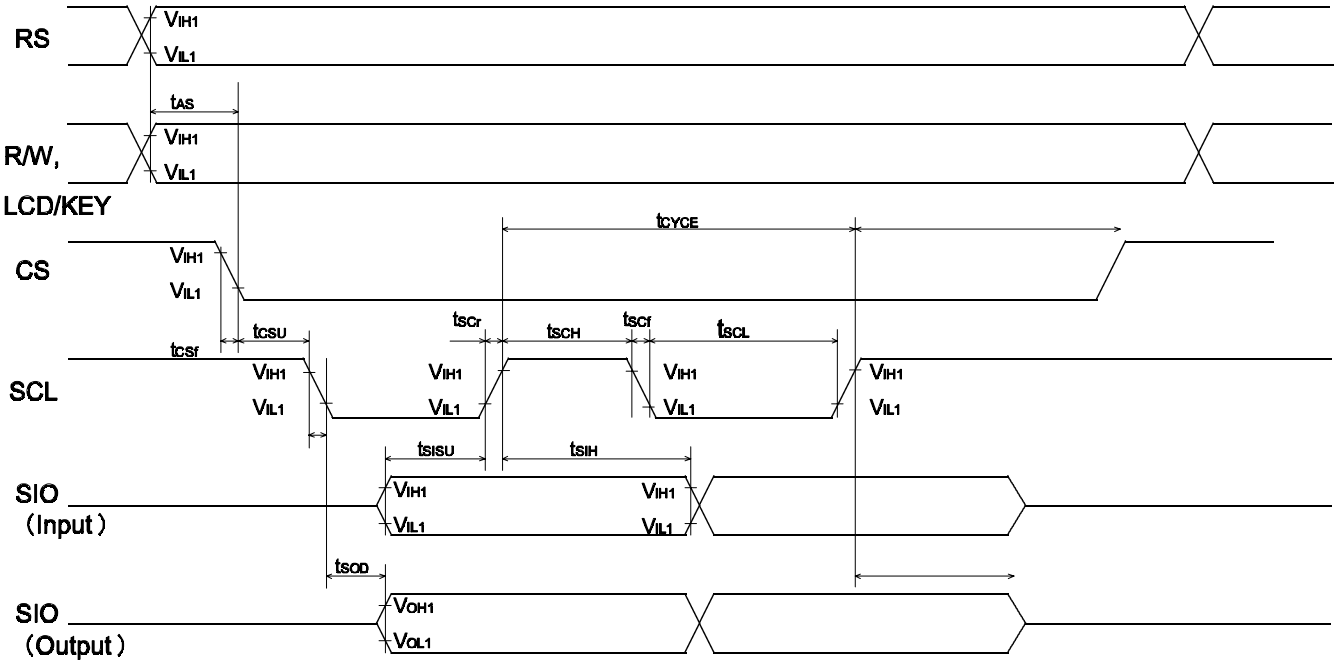


Fig. 3 Serial Interface Sequence Characteristics

-I/O Part sequence

P A R A M E T E R	S Y M B O L	MIN.	MAX.	CONDITON	UNIT
Port set time	t_{PS}	-	500	Fig. 2	uS

-The load of DB_0 to DB_7 is CL = 100 pF

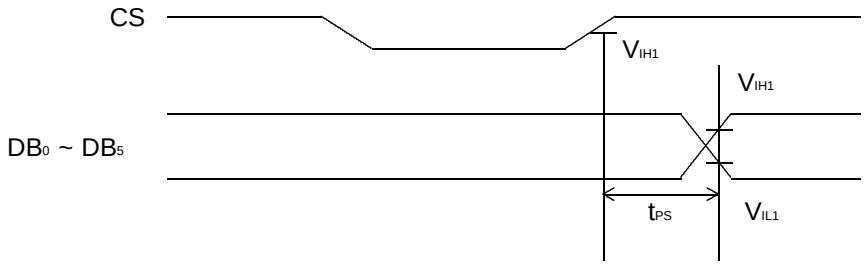
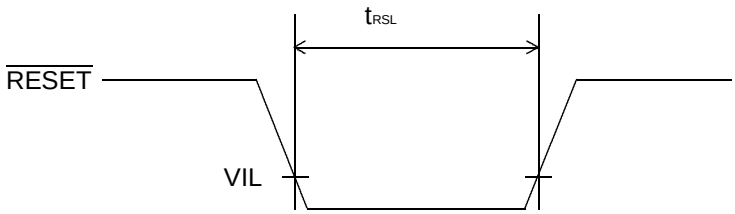


Fig. 2 I/O Port Sequence (Serial Interface)

-The input conditions of using hardware reset circuit.

Input Timing



P A R A M E T E R	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Reset Input RAW level width	t_{RSL}	-	1.2	-	-	ms

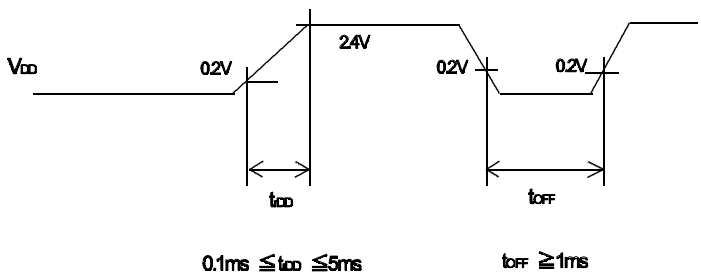
-The power supply conditions of using power on reset circuit.

(Ta = -20 ~ +75°C)

P A R A M E T E R	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
The power supply rise time	t_{rDD}	-	0.1	-	5	ms
The power OFF time	t_{OFF}	-	1	-	-	ms

Since the internal initialization circuits will not operate normally unless the above conditions are met, in such a case of initialized by instruction. (Refer to initialization by the instruction)

t_{OFF} specifies the power off time in a short period off or cyclical on/off.



* t_{OFF} specifies the power off time in a short period off or cyclical ON/OFF.

-Key Scan Sequence

P A R A M E T E R	SYMBOL	MIN.	TYP.	MAX.	CONDITION	UNIT
E/SCL-S_0 to S_7 Delay time	t_{KDS}	-	66.7	300	Fig. 3	uS
Key scan pulse width "H","L" level	t_{KP}	-	44.4	48	Fig. 3	uS
Key scan time	t_{KS}	-	0.36	0.38	Fig. 3	mS
REQ output delay time	t_{KDR}	-	-	1.0	Fig. 3	uS
Key in check signal frequency	t_{KF}	0.98	1.41	1.84	Fig. 3	KHz

-The load of K_0 to K_3 is CL = 20 pF

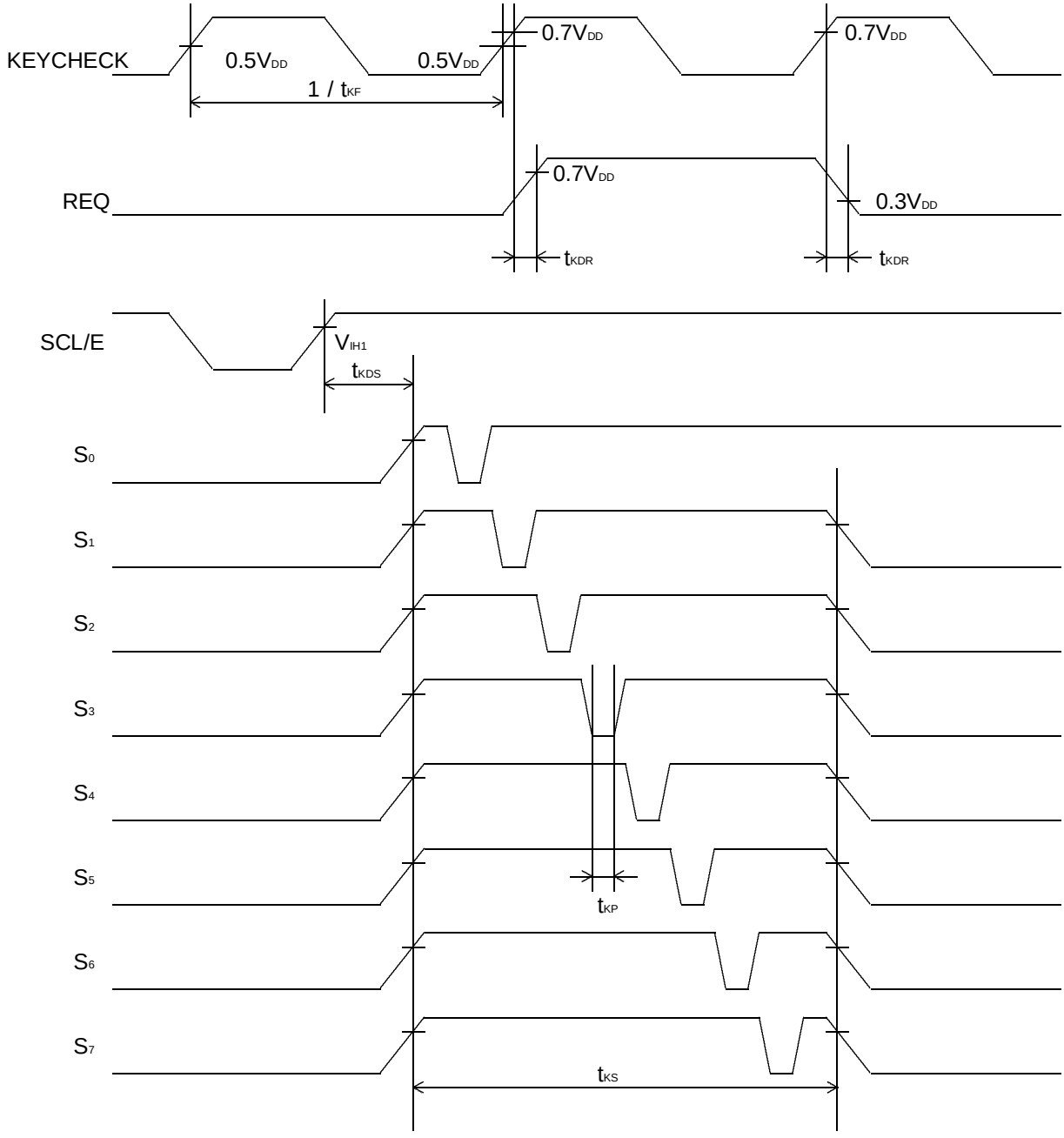


Fig. 3 Key scan sequence

-External clock input

P A R A M E T E R	SYMBOL	MIN.	MAX.	CONDITION	UNIT
External clock operating frequency	f_{CP}	125	235	Fig. 4	KHz
External clock duty	Duty	45	55	Fig. 4	%
External clock rise time	t_{CPr}	-	0.2	Fig. 4	uS
External clock fall time	t_{CPf}	-	0.2	Fig. 4	uS

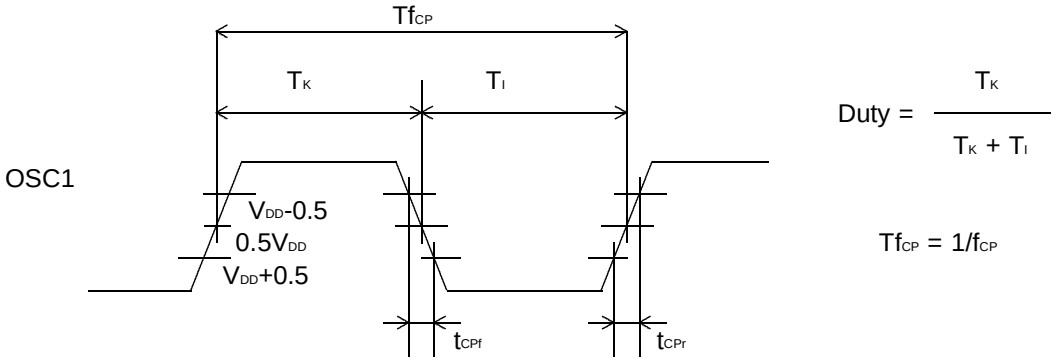
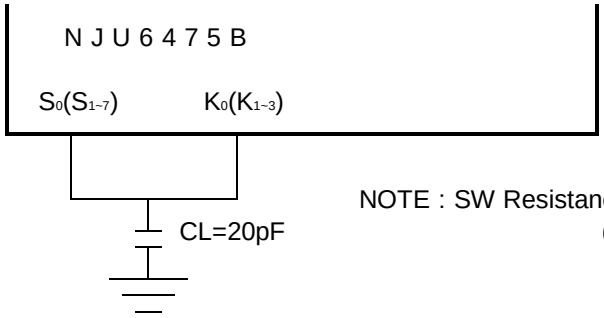


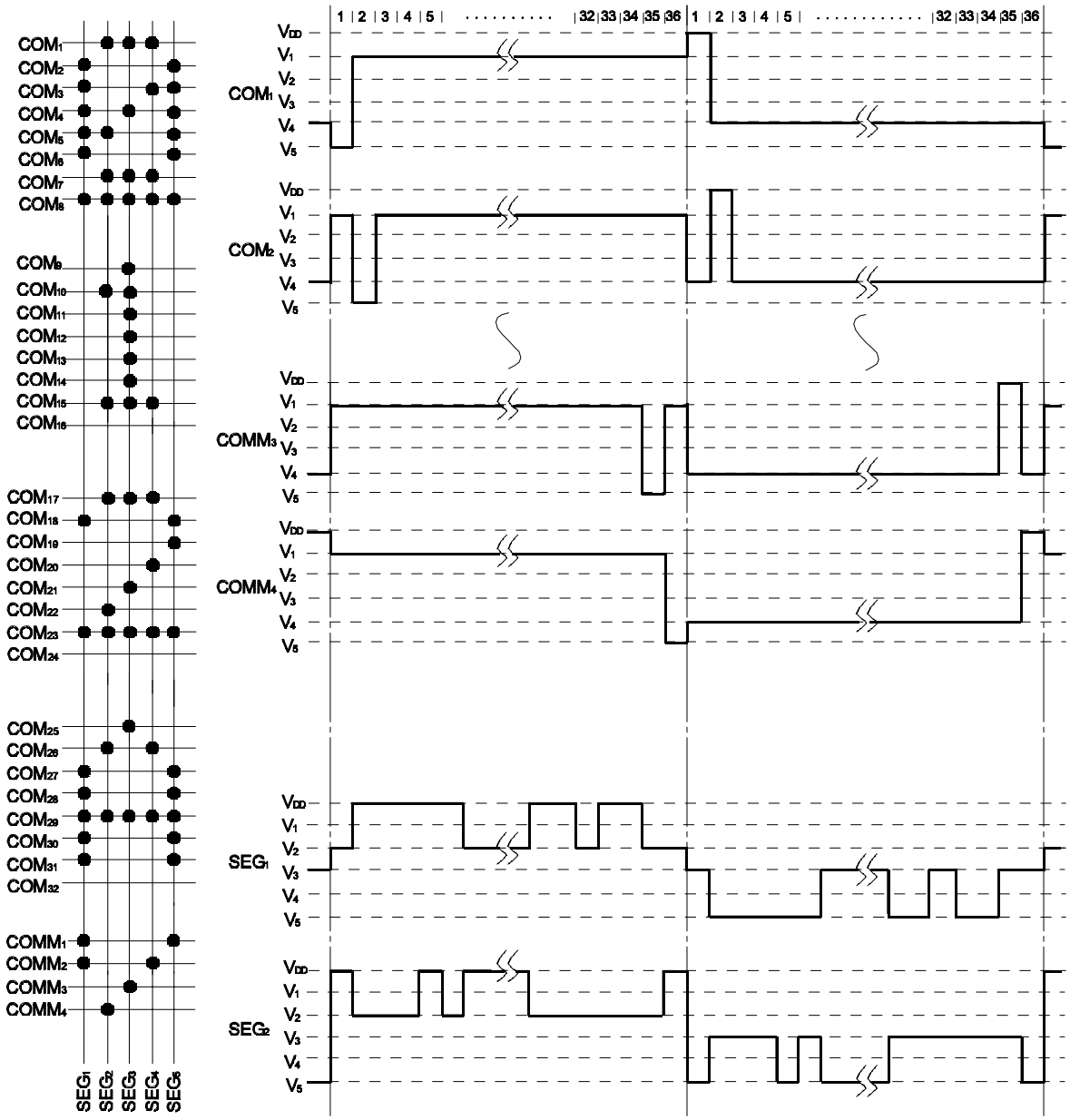
Fig.4 External clock input

-The key scan circuit timing characteristics measurement cricurit



NOTE : SW Resistance is 0Ω
(measurement : only pattern wires)

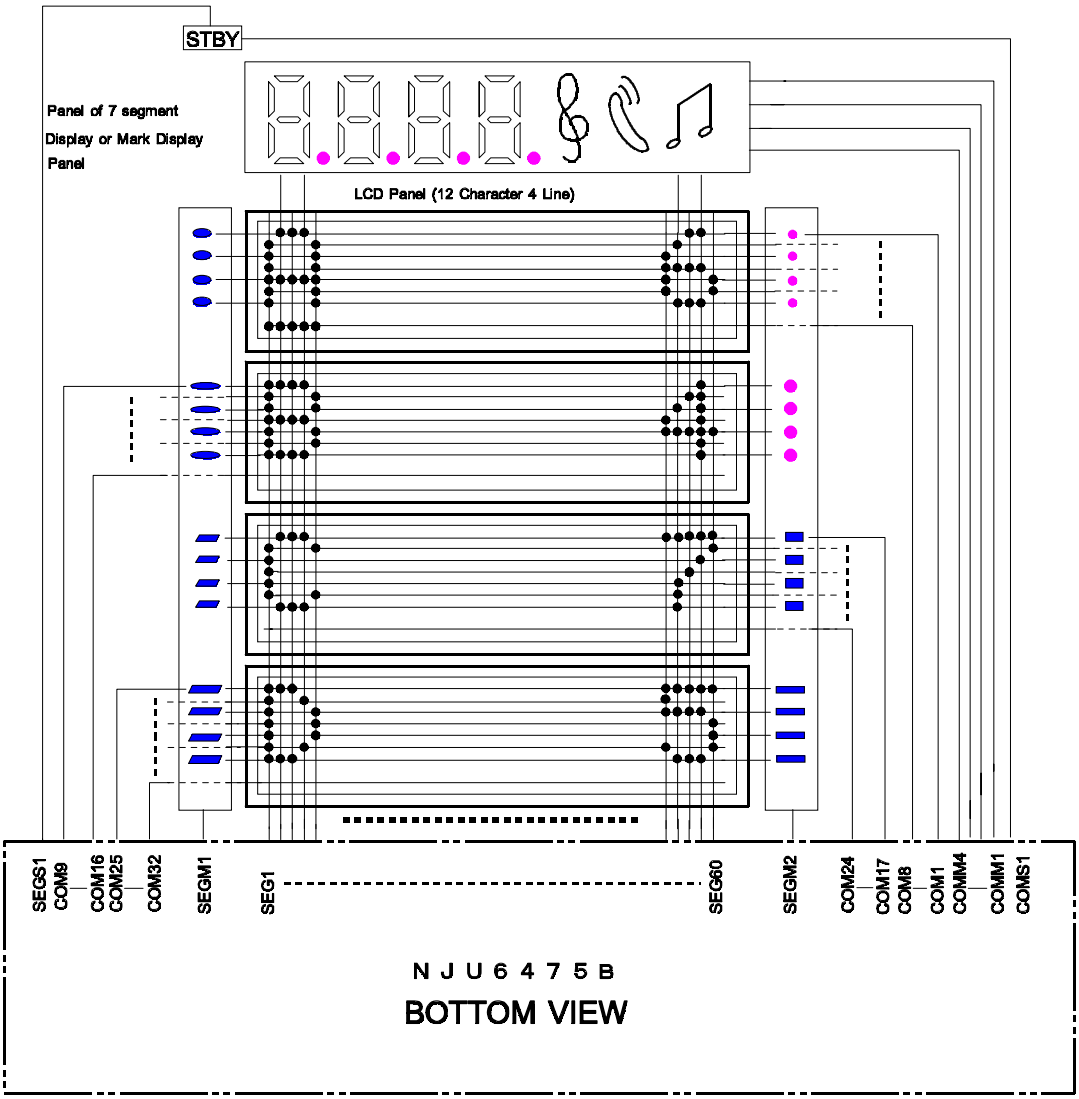
■ LCD DRIVING WAVE FORM



N J U 6 4 7 5 B

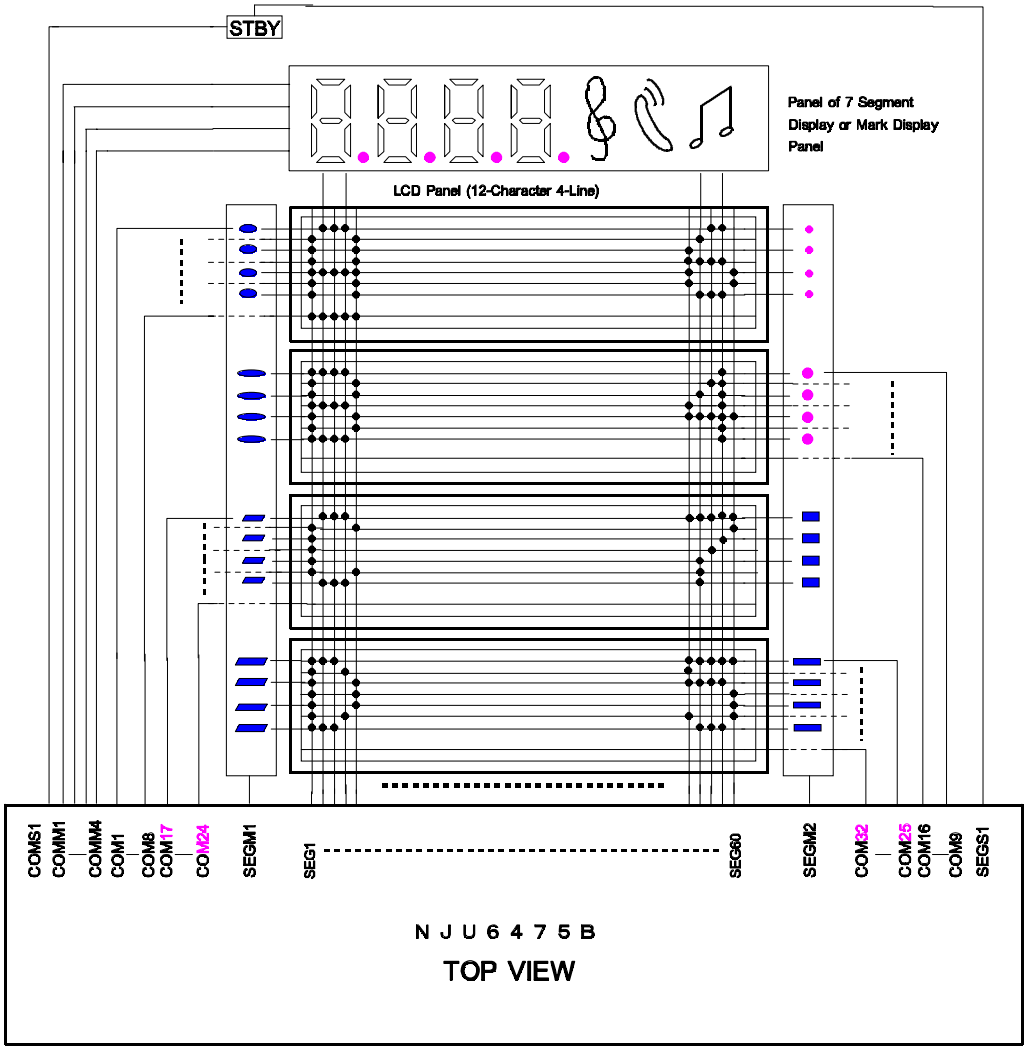
LCD Driving Wave Form 1/36 Duty

■ APPLICATION CIRCUIT (1)



12-Character 4-Line
(Terminal description, Mode A)

■ APPLICATION CIRCUIT (2)



12-Character 4-Line
(Terminal description, Mode B)

MEMO