NJU6675

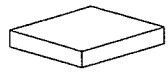
PRELIMINARY

BIT MAP LCD DRIVER

■ GENERAL DESCRIPTION

The NJU6675 is a bit map LCD driver to display graphics or characters.
It contains 5,568 bits display data RAM, microprocessor interface circuits, instruction decoder, 96-segment and 58-common drivers.
The bit image display data is transferred to the display data RAM by serial or 8-bit parallel interface.
The NJU6675 displays 58 x 96 dots graphics or 6-character 3-line by 16 x 16 dots character.
The operating voltage from 2.4V to 3.3V and low operating current are useful to apply small size battery operating items.
The build-in Electrical Variable Resistance is very precision.

■ PACKAGE OUTLINE



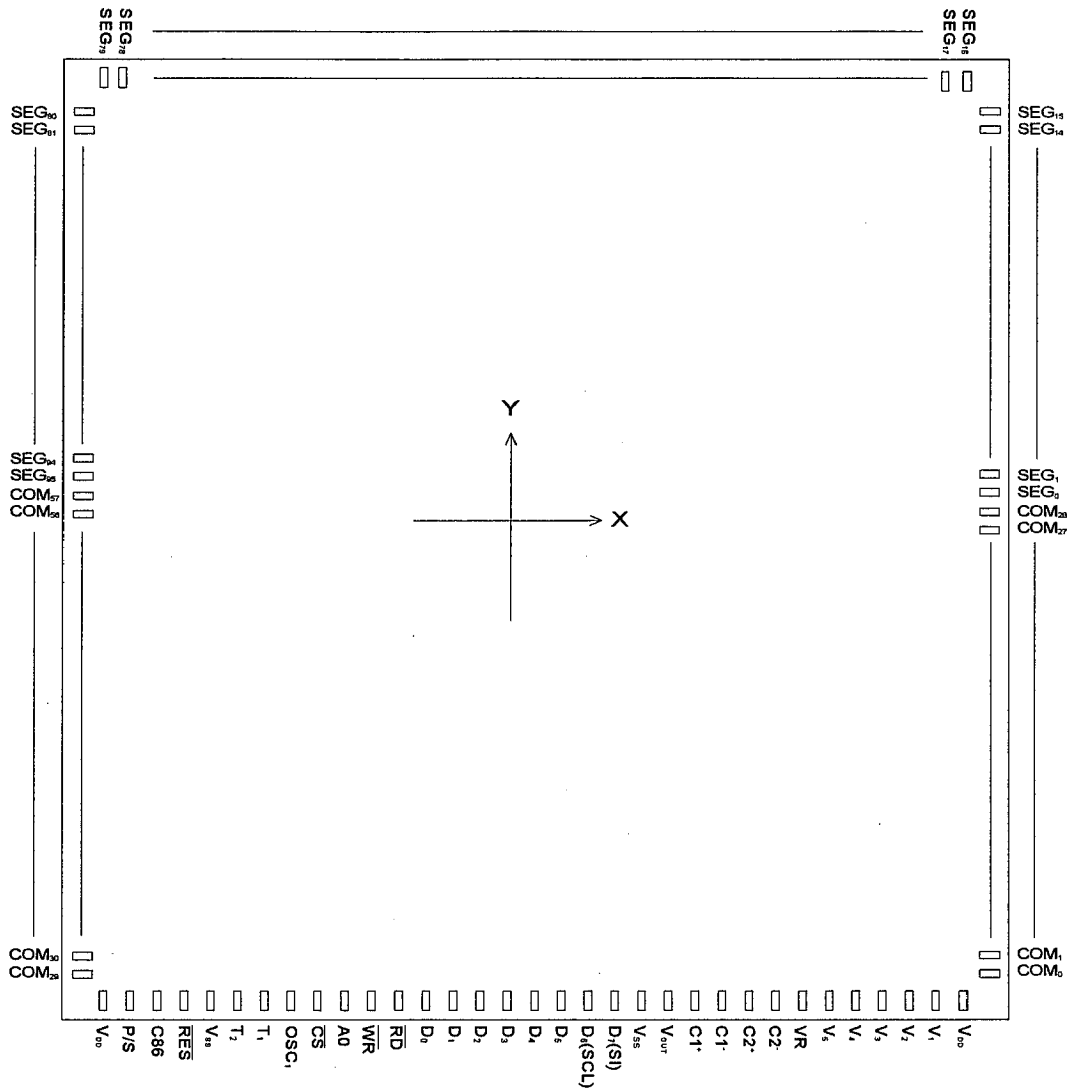
NJU6675CH

■ FEATURES

- Direct Correspondence between Display Data RAM and LCD Pixel
- Display Data RAM - 5,568 bits
- 135 LCD Drivers - 58-common and 96-segment
- Direct Microprocessor Interface for both of 68 and 80 type MPU
- Serial Interface
- Duty Ratio ; 1/58 Duty
- Useful Instruction Set
  Display Data Read/Write, Display ON/OFF Cont, Inverse Display, Page Address Set, Column Address Set, Status Read, All On/Off, Read Modify Write, Power Saving, etc.
- Power Supply Circuits for LCD Incorporated
  Step up Circuits, Regulator, Voltage Follower x 4
- Precision Electrical Variable Resistance
- Low Power Consumption
- Operating Voltage --- 2.4V to 3.3V
- LCD Driving Voltage --- 6.0V to 10V
- Package Outline --- TCP / Bumped Chip
- C-MOS Technology

Mar.1999
Ver.1

■ PAD LOCATION



Chip Center	X=0um, Y=0um
Chip Size	X=4.84mm, Y=4.2mm
Chip Thickness	400um ± 30um
Bump Size	53um x 113um
PAD Pitch	70um MIN.
Bump Height	25um TYP.
Bump Material	Au

■ PAD COORDINATES

Chip Size 4.84mm x 4.2mm(Chip Center X=0um,Y=0um)

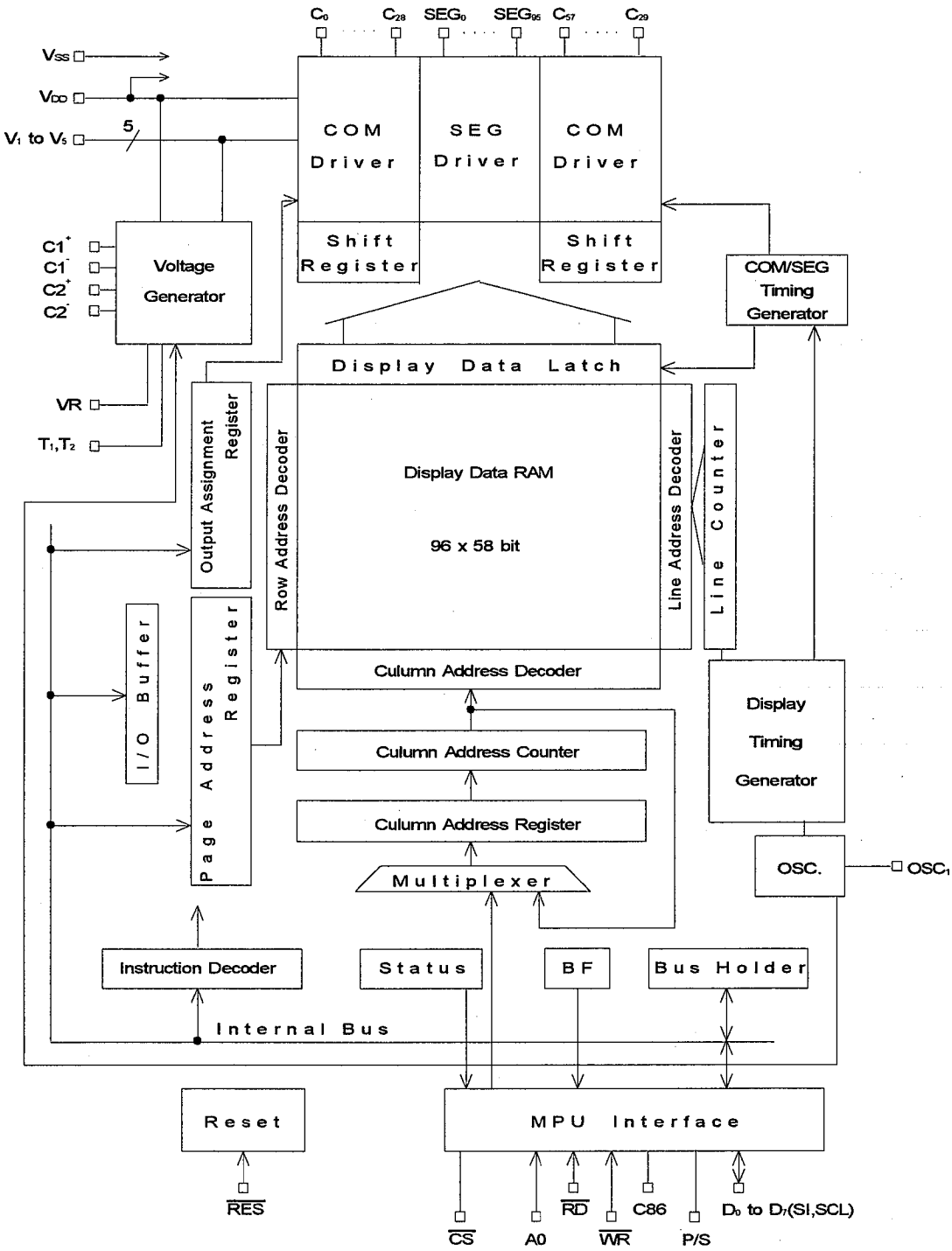
PAD No.	Terminal	X= um	Y= um
1	V_{DD}	-1532	-1947
2	P/S	-1442	-1947
3	C86	-1352	-1947
4	$\overline{RES}$	-1262	-1947
5	V_{SS}	-1172	-1947
6	T_2	-1082	-1947
7	T_1	-992	-1947
8	OSC_1	-902	-1947
9	$\overline{CS}$	-812	-1947
10	A0	-722	-1947
11	$\overline{WR}$	-632	-1947
12	$\overline{RD}$	-542	-1947
13	D_0	-452	-1947
14	D_1	-362	-1947
15	D_2	-272	-1947
16	D_3	-182	-1947
17	D_4	-92	-1947
18	D_5	-2	-1947
19	$D_{6(SCL)}$	88	-1947
20	$D_{7(SI)}$	178	-1947
21	V_{SS}	360	-1947
22	V_{OUT}	450	-1947
23	$C1^+$	540	-1947
24	$C1^-$	630	-1947
25	$C2^+$	720	-1947
26	$C2^-$	810	-1947
27	VR	900	-1947
28	V_5	990	-1947
29	V_4	1080	-1947
30	V_3	1170	-1947
31	V_2	1260	-1947
32	V_1	1350	-1947
33	V_{DD}	1440	-1947
34	C_0	2266	-1859
35	C_1	2266	-1789
36	C_2	2266	-1719
37	C_3	2266	-1649
38	C_4	2266	-1579
39	C_5	2266	-1508
40	C_6	2266	-1438
41	C_7	2266	-1368
42	C_8	2266	-1298
43	C_9	2266	-1228
44	C_{10}	2266	-1157
45	C_{11}	2266	-1087
46	C_{12}	2266	-1017
47	C_{13}	2266	-947
48	C_{14}	2266	-877
49	C_{15}	2266	-806
50	C_{16}	2266	-736

PAD No.	Terminal	X= um	Y= um
51	C_{17}	2266	-666
52	C_{18}	2266	-596
53	C_{19}	2266	-526
54	C_{20}	2266	-455
55	C_{21}	2266	-385
56	C_{22}	2266	-315
57	C_{23}	2266	-245
58	C_{24}	2266	-175
59	C_{25}	2266	-104
60	C_{26}	2266	-34
61	C_{27}	2266	36
62	C_{28}	2266	106
63	SEG_0	2266	219
64	SEG_1	2266	290
65	SEG_2	2266	360
66	SEG_3	2266	430
67	SEG_4	2266	500
68	SEG_5	2266	570
69	SEG_6	2266	641
70	SEG_7	2266	711
71	SEG_8	2266	781
72	SEG_9	2266	851
73	SEG_{10}	2266	921
74	SEG_{11}	2266	992
75	SEG_{12}	2266	1062
76	SEG_{13}	2266	1132
77	SEG_{14}	2266	1202
78	SEG_{15}	2266	1272
79	SEG_{16}	2211	1947
80	SEG_{17}	2141	1947
81	SEG_{18}	2071	1947
82	SEG_{19}	2001	1947
83	SEG_{20}	1931	1947
84	SEG_{21}	1860	1947
85	SEG_{22}	1790	1947
86	SEG_{23}	1720	1947
87	SEG_{24}	1650	1947
88	SEG_{25}	1580	1947
89	SEG_{26}	1509	1947
90	SEG_{27}	1439	1947
91	SEG_{28}	1369	1947
92	SEG_{29}	1299	1947
93	SEG_{30}	1229	1947
94	SEG_{31}	1158	1947
95	SEG_{32}	1088	1947
96	SEG_{33}	1018	1947
97	SEG_{34}	948	1947
98	SEG_{35}	878	1947
99	SEG_{36}	807	1947
100	SEG_{37}	737	1947

PAD No.	Terminal	X= um	Y= um
101	SEG38	667	1947
102	SEG39	597	1947
103	SEG40	527	1947
104	SEG41	456	1947
105	SEG42	386	1947
106	SEG43	316	1947
107	SEG44	246	1947
108	SEG45	176	1947
109	SEG46	105	1947
110	SEG47	35	1947
111	SEG48	-35	1947
112	SEG49	-105	1947
113	SEG50	-176	1947
114	SEG51	-246	1947
115	SEG52	-316	1947
116	SEG53	-386	1947
117	SEG54	-456	1947
118	SEG55	-527	1947
119	SEG56	-597	1947
120	SEG57	-667	1947
121	SEG58	-737	1947
122	SEG59	-807	1947
123	SEG60	-878	1947
124	SEG61	-948	1947
125	SEG62	-1018	1947
126	SEG63	-1088	1947
127	SEG64	-1158	1947
128	SEG65	-1229	1947
129	SEG66	-1299	1947
130	SEG67	-1369	1947
131	SEG68	-1439	1947
132	SEG69	-1509	1947
133	SEG70	-1580	1947
134	SEG71	-1650	1947
135	SEG72	-1720	1947
136	SEG73	-1790	1947
137	SEG74	-1860	1947
138	SEG75	-1931	1947
139	SEG76	-2001	1947
140	SEG77	-2071	1947
141	SEG78	-2141	1947
142	SEG79	-2211	1947
143	SEG80	-2266	1272
144	SEG81	-2266	1202
145	SEG82	-2266	1132
146	SEG83	-2266	1062
147	SEG84	-2266	992
148	SEG85	-2266	921
149	SEG86	-2266	851
150	SEG87	-2266	781

PAD No.	Terminal	X= um	Y= um
151	SEG88	-2266	711
152	SEG89	-2266	641
153	SEG90	-2266	570
154	SEG91	-2266	500
155	SEG92	-2266	430
156	SEG93	-2266	360
157	SEG94	-2266	290
158	SEG95	-2266	219
159	C57	-2266	106
160	C56	-2266	36
161	C55	-2266	-34
162	C54	-2266	-104
163	C53	-2266	-175
164	C52	-2266	-245
165	C51	-2266	-315
166	C50	-2266	-385
167	C49	-2266	-455
168	C48	-2266	-526
169	C47	-2266	-596
170	C46	-2266	-666
171	C45	-2266	-736
172	C44	-2266	-806
173	C43	-2266	-877
174	C42	-2266	-947
175	C41	-2266	-1017
176	C40	-2266	-1087
177	C39	-2266	-1157
178	C38	-2266	-1228
179	C37	-2266	-1298
180	C36	-2266	-1368
181	C35	-2266	-1438
182	C34	-2266	-1508
183	C33	-2266	-1579
184	C32	-2266	-1649
185	C31	-2266	-1719
186	C30	-2266	-1789
187	C29	-2266	-1859

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

<table>
<tr><th>No</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>1,33</td><td>V_{DD}</td><td>Power</td><td>V_{DD}=+3V</td></tr>
<tr><td>5,21</td><td>Vss</td><td>GND</td><td>Vss=0V</td></tr>
<tr><td>32
31
30
29
28</td><td>V_1
V_2
V_3
V_4
V_5</td><td>Power</td><td>LCD Driving Voltage Supplying Terminal. When the internal voltage tripler is not used, supply each level of LCD driving voltage from outside with following relation.
$V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$
When the internal power supply is on, the internal circuits generate and supply following LCD bias voltage from V_1 to V_4 terminals.
<table>
<tr><th>Terminal</th><th>V_1</th><th>V_2</th><th>V_3</th><th>V_4</th></tr>
<tr><td>Voltage</td><td>V_5+7/8V_{LCD}</td><td>V_5+6/8V_{LCD}</td><td>V_5+2/8V_{LCD}</td><td>V_5+1/8V_{LCD}</td></tr>
</table>
(V_{LCD}=V_{DD}-V_5)</td></tr>
<tr><td>23
24
25
26</td><td>$C1^+$
$C1^-$
$C2^+$
$C2^-$</td><td>O</td><td>Step up capacitor connecting terminals.
In case of tripler operation, connect the capacitor between $C1^+$ and $C1^-$, $C2^+$ and $C2^-$.
In case of doubler operation, connect the capacitor between $C2^+$ and $C2^-$, connect $C2^+$ to $C1^+$, and $C1^-$ should be open.</td></tr>
<tr><td>22</td><td>V_{OUT}</td><td>O</td><td>Step up voltage output terminal. Connect the step up capacitor between this terminal and Vss.</td></tr>
<tr><td>27</td><td>VR</td><td>I</td><td>Voltage adjust terminal. V_5 level is adjusted by external bleeder resistance connecting between V_{DD} and V_5 terminal.</td></tr>
<tr><td>7
6</td><td>T_1
T_2</td><td>I</td><td>LCD bias voltage control terminals. (*Don't Care)
<table>
<tr><th>T_1</th><th>T_2</th><th>Step up Cir.</th><th>Voltage Adj.</th><th>V/F Cir.</th></tr>
<tr><td>L</td><td>*</td><td>Available</td><td>Available</td><td>Available</td></tr>
<tr><td>H</td><td>L</td><td>Not Avail.</td><td>Available</td><td>Available</td></tr>
<tr><td>H</td><td>H</td><td>Not Avail.</td><td>Not Avail.</td><td>Available</td></tr>
</table></td></tr>
<tr><td>13 to 20
(20)
(19)</td><td>D_0 to D_7
(SI)
(SCL)</td><td>I/O</td><td>P/S="H" : Tri-state bi-directional Data I/O terminal in 8-bit parallel operation.
P/S="L" : D_7=Serial data input terminal. D_6=Serial data clock signal input terminal.
Data from SI is loaded at the rising edge of SCL and latched as the parallel data at 8th rising edge of SCL.</td></tr>
<tr><td>10</td><td>A0</td><td>I</td><td>Connect to the Address bus of MPU. The data on the D_0 to D_7 is distinguished between Display data and Instruction by status of A0.
<table>
<tr><th>A0</th><th>H</th><th>L</th></tr>
<tr><td>Distin.</td><td>Display Data</td><td>Instruction</td></tr>
</table></td></tr>
<tr><td>4</td><td>$\overline{RES}$</td><td>I</td><td>Reset terminal. When the $\overline{RES}$ terminal goes to "L", the initialization is performed.
Reset operation is executing during "L" state of $\overline{RES}$.</td></tr>
<tr><td>9</td><td>$\overline{CS}$</td><td>I</td><td>Chip select terminal. Data Input/Output are available during $\overline{CS}$ ="L".</td></tr>
<tr><td>12</td><td>$\overline{RD}$
(E)</td><td>I</td><td><In case of 80 type MPU>
$\overline{RD}$ signal of 80 type MPU input terminal. Active"L".
During this signal is "L", D_0 to D_7 terminals are output.
<In case of 68 type MPU>
Enable signal of 68 type MPU input terminal. Active "H".</td></tr>
<tr><td>11</td><td>$\overline{WR}$
(R/W)</td><td>I</td><td><In case of 80 type MPU>
Connect to the 80 type MPU $\overline{WR}$ signal. Active "L".
The data on the data bus input synchronizing the rise edge of this signal.
<In case of 68 type MPU>
Read/write control signal of 68 type MPU input terminal.
<table>
<tr><th>R/W</th><th>H</th><th>L</th></tr>
<tr><td>State</td><td>Read</td><td>Write</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>No</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>3</td><td>C86</td><td>I</td><td>MPU interface type selection terminal.
<table>
<tr><td>C86</td><td>H</td><td>L</td></tr>
<tr><td>Status</td><td>68 Type</td><td>80 Type</td></tr>
</table></td></tr>
<tr><td>2</td><td>P/S</td><td>I</td><td>Serial or parallel interface selection terminal.
<table>
<tr><th>P/S</th><th>Chip Select</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>Serial CLK</th></tr>
<tr><td>"H"</td><td>$\overline{CS}$</td><td>A0</td><td>D0 to D7</td><td>$\overline{RD}$,$\overline{WR}$</td><td>-</td></tr>
<tr><td>"L"</td><td>$\overline{CS}$</td><td>A0</td><td>SI(D7)</td><td>Write only</td><td>SCL(D6)</td></tr>
</table>
*RAM data and status read operation do not work in mode of the serial interface.

In case of the serial interface (P/S="L"), $\overline{RD}$ and $\overline{WR}$ must be fixed "H" or "L", and D0 to D5 are high impedance.</td></tr>
<tr><td>8</td><td>OSC1</td><td>I</td><td>System clock input terminal for Maker testing. (This terminal should be open.)</td></tr>
<tr><td>34 to 62</td><td>C0 to C28</td><td>O</td><td rowspan="3">LCD driving signal output terminals.
Segment output terminals : SEG 0 to SEG95
Common output terminals : C 0 to C57

Segment output terminal
The following output voltages are selected by the combination of FR and data in the RAM.
<table>
<tr><th rowspan="2">RAM Data</th><th rowspan="2">FR</th><th colspan="2">Output Voltage</th></tr>
<tr><th>Normal</th><th>Reverse</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>VDD</td><td>V2</td></tr>
<tr><td>L</td><td>V5</td><td>V3</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V2</td><td>VDD</td></tr>
<tr><td>L</td><td>V3</td><td>V5</td></tr>
</table>
Common Output Terminal
The following output voltages are selected by the combination of FR and status of common.
<table>
<tr><th>Status of Common</th><th>FR</th><th>Output Voltage</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V5</td></tr>
<tr><td>L</td><td>VDD</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>V4</td></tr>
</table></td></tr>
<tr><td>63 to 158</td><td>SEG0 to SEG95</td><td>O</td></tr>
<tr><td>187 to 159</td><td>C29 to C57</td><td>O</td></tr>
</table>

■ Functional Description

(1) Description for each blocks

(1-1) Busy Flag (BF)

While the internal circuits are operating, the busy flag (BF) is "1", and any instruction excepting for the status read are inhibited .

The busy flag goes to "1" from D_7 terminal when status read instruction is executed.

When enough cycle time over than t_{CYC} indicated in "BUS TIMING CHARACTERISTICS" is ensure, no need to check the busy flag for reduction of the MPU loaded.

(1-2) Line Counter

The Line Counter generates the line address of display data RAM by the count up operation synchronizing the common cycle after the operation at the status change of internal FR signal.

(1-3) Column Address Counter

The column address counter is 8-bit pre-settable counter addressing the column address of display data RAM as shown in Fig. 1. It is incremented (+1) up to $(60)_H$ by the Display Data Read/Write instruction execution. It stops the count up operation at $(60)_H$, and it does not count up non existing address area over than $(60)_H$ by the count lock function. This count lock is released by new column address set.

The column address counter is independent of the Page Register.

By the Address Inverse Instruction, the column address decoder inverse the column address of Display Data RAM corresponding to the Segment Driver.

(1-4) Page Register

The page register gives a page address of Display Data RAM as shown in Fig. 1. When the MPU accesses the data with the page change, the page address set instruction is required. Page address "7" is D_0,D_1 is valid.

(1-5) Display Data RAM

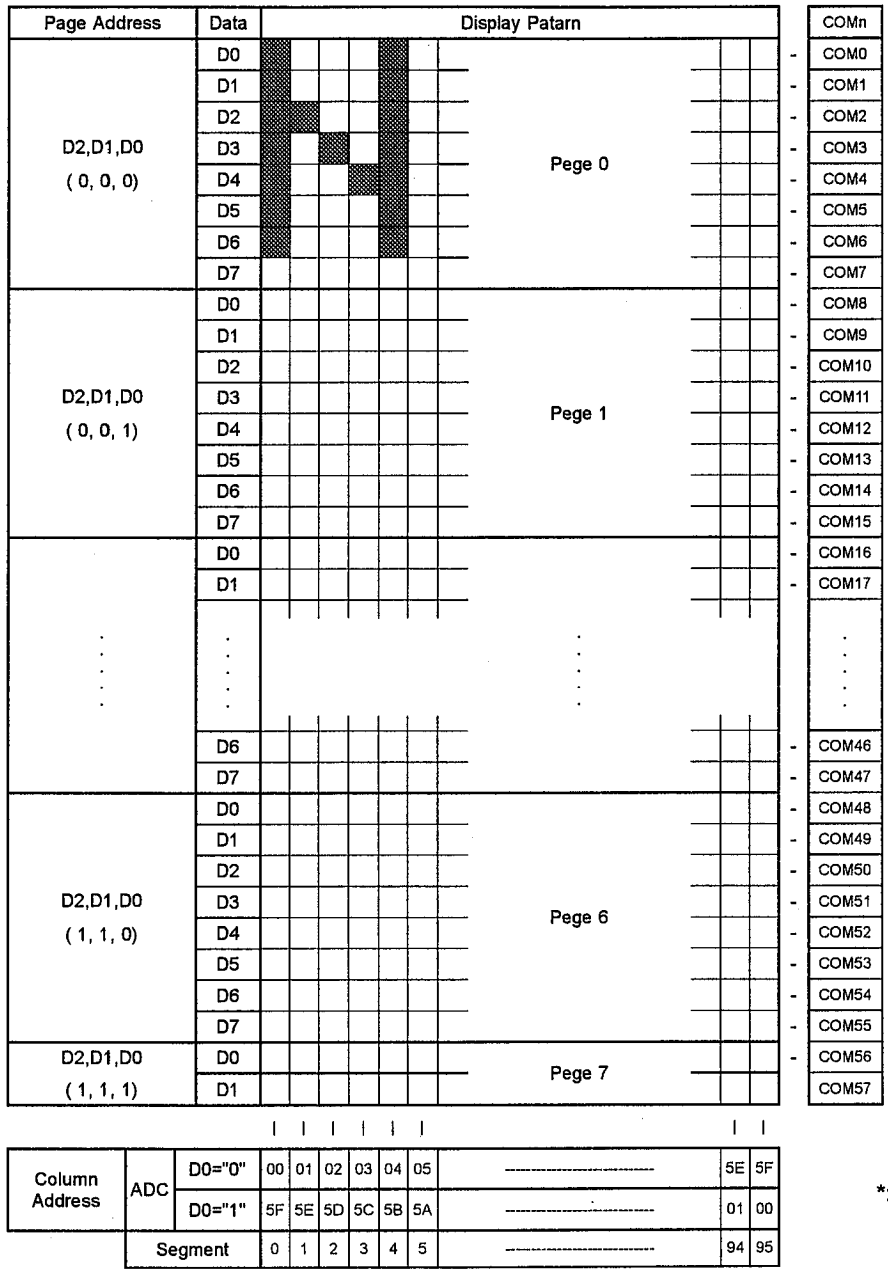
Display Data RAM is the bit map RAM consisting of 5,568 bits to memorize the display data corresponding to each pixel of LCD panel. The each bit in the Display Data RAM corresponds to the each pixel of the LCD panel and controls the display by following bit data.

When Normal Display : On="1" , Off="0"
When Inverse Display : On="0" , Off="1"

The Display Data RAM outputs 96-bit parallel data in the area addressed by the line counter, and these data are set into the Display Data Latch.

The access operation from MPU to the display data RAM and the data output from the display data RAM are so controlled to operate independently that the data rewriting does not influence with any malfunctions to the display.

The relation between column address and segment output can inverse by the Address Inverse Instruction ADC as shown in Fig. 1.



*:1/58Duty

Fig.1 Correspondence with Display Data RAM and Address
(COMI can be used in case of 1/58 duty set.)

(1-6) Common Driver Assignment
The scanning order can be assigned by setting A3 of the Output Assignment Register as shown Table 1.

Table 1

Register		COM Outputs Terminals			
A3	PAD No.	34	62	159	187
	Pin name	C0	C28	C57	C29
0	→	COM0 →	→ COM28	COM57 ←	← COM29
1	→	COM57 ←	← COM29	COM0 →	→ COM28

(1-7) Reset Circuit
Reset circuit operates the following initializations when the condition of $\overline{RES}$ terminal goes to "L" level.

Initialization
1 Display Off
2 Normal Display (Non-inverse display)
3 ADC Select : Normal (ADC Instruction D0="0")
4 Read Modify Write Mode Off
5 Internal Power supply (Step up) circuits Off
6 Clear the serial interface register
7 Set the address (00)H to the Column Address Counter
8 Set the page "0" to the Page Address Register
9 Select the D3 of the Output Assignment Register to "0"
10 Set the EVR register to (00)H

The $\overline{RES}$ terminal should be connected to the Reset terminal of MPU for the initialization at the mean time with MPU as shown "MPU Interface Example". The period of $\overline{RES}$ signal requires over than 10 μ s $\overline{RES}$="L" level input as shown in "Electrical Characteristics". After 1 μ s from the rise edge of $\overline{RES}$ signal, the operation goes to normal.
When the internal LCD power supply is not used, the external LCD power supply into the NJU6675 must be turned on during $\overline{RES}$ = "L". Although the condition of $\overline{RES}$="L" clear each registers and initialize as above, the oscillation circuit and the output terminal conditions (D0 to D7) are not influenced. The initialization must be performed using $\overline{RES}$ terminal at the power on, to prevent hung up or any incorrect operations. The reset Instruction performs the initialization procedures from No.7 to No.10 as shown in above.

Note) The noise into the $\overline{RES}$ terminal should be eliminated to avoid error on the application with the careful design.

(1-8) LCD Driving

(a) LCD Driving Circuits

LCD driving circuits are consisted of 154 multiplexers which operate as 96 Segment drivers and 58 Common drivers. 58 Common drivers with the shift register scan the common display signal. The combination of the Display data, COM scan signal and FR signal forms the LCD driving output voltage. The output wave form is shown in the Fig. 7.

(b) Display Data Latch Circuits

Display Data Latch stores 96-bit display data temporality which is output to LCD driver circuits at a common cycle from Display Data RAM addressed by Line Counter. The instructions of Display On/Off, Display inverse On/Off control only the data in Display Data Latch, therefore, the data in the Display Data RAM is not changed.

(c) Line Counter and Latch signal of Latch Circuits

The clock to Line Counter and latch signal to the Latch Circuits are generated from the internal display clock (CL). The line address of Display Data RAM is renewed synchronizing with display clock (CL). 96 bits display data are latched in display latch circuits synchronizing with display clock, and then output to the LCD driving circuits. The display data transfer to the LCD driving circuits is executed independently with RAM access by the MPU.

(d) Display Timing Generator

Display Timing Generator generates the timing signal for the display system by combination of the master clock CL and Driving Signal FR (refer to Fig.2). The Frame Signal FR and LCD alternative signal generate LCD driving waveform of the two frame alternative driving method.

(e) Common Timing Generation

The common timing is generated by display clock CL (refer to Fig.2).

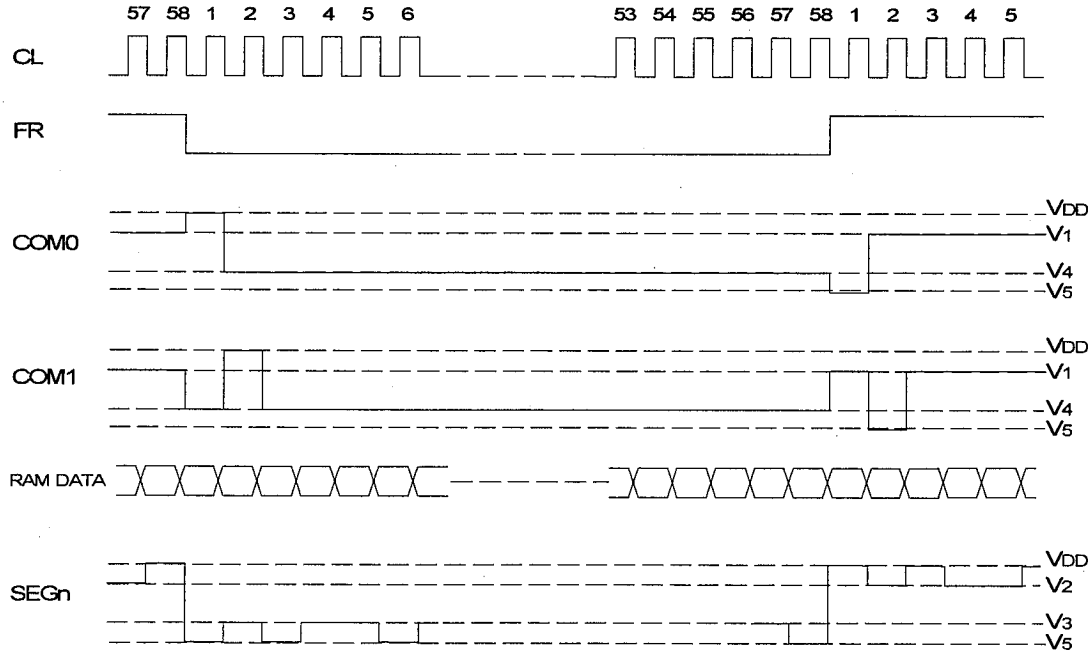


Fig.2 Waveform of Display Timing

(f) Oscillation Circuits

The Oscillation Circuit is a low power CR oscillator incorporating with a Resistor and a Capacitor. It generates clocks for display timing signal source and the clock for step up circuits for LCD driving. The oscillation circuit output frequency is divided by 4 which is used as display clock CL.

(g) Power Supply Circuits

Internal Power Supply Circuit generate the High voltage and Bias voltage for the LCD. The power Supply Circuits consists of Step up (Tripler or Doubler) Circuits, Regulator Circuits, and Voltage Followers. The internal Power Supply is designed for small size LCD panel, therefore it is not suitable for the large size LCD panel application. If the contrast is not good in the large size LCD panel application, please supply the external.

The suitable values of the capacitors connecting to the V_1 to V_5 terminals and the step up circuit, and the feed-back resistors for V_5 operational amplifier depend on the LCD panel. And the power consumption with the LCD panel is depending on the display pattern. Please evaluate with actual LCD module.

The operation of internal Power Supply Circuits is controlled by the Internal Power Supply On/Off Instruction. When the Internal Power Supply Off Instruction is executed, all of the step up circuits, regulator circuits, voltage follower circuits are turned off. In this time, the bias voltage of V_1, V_2, V_3, V_4, and V_5 for the LCD should be supplied from outside, terminals $C1^+$, $C1^-$, $C2^+$, $C2^-$, and VR should be open. The status of internal power supply is selected by T_1 and T_2 terminal. Furthermore the external power supply operates with some of internal power supply function.

Table.3 (* : Don't Care)

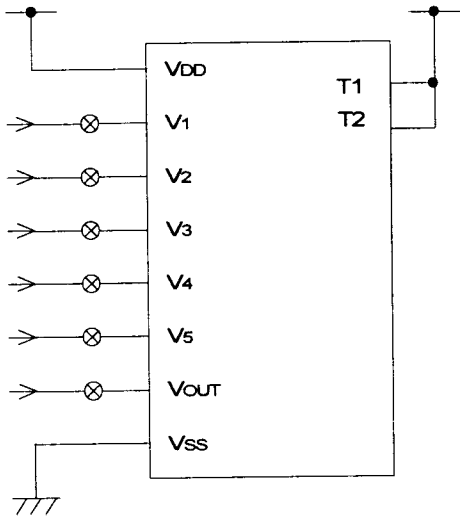
T_1	T_2	Step up	Voltage Adj.	Buffer (V/F)	Ext. Power Supply	$C1^+$,$C1^-$,$C2^+$,$C2^-$	VR Term.
L	*	O	O	O	-		
H	L	x	O	O	V_{OUT}	OPEN	
H	H	x	x	O	V_5, V_{OUT}	OPEN	OPEN

When (T_1, T_2)=(H, L), $C1^+$, $C1^-$, $C2^+$, $C2^-$ terminals for voltage booster circuits are open because the step up circuits doesn't operate. Therefore the LCD driving voltage to the V_{OUT} terminal should be supplied from outside.

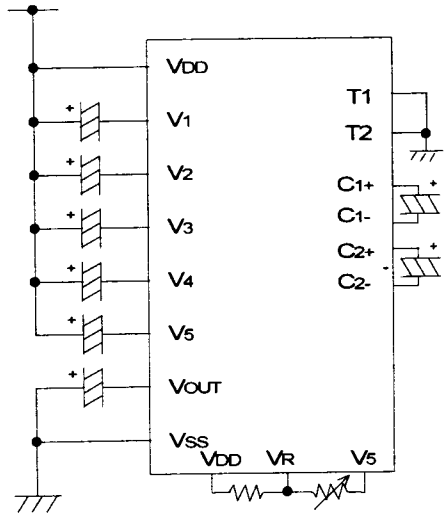
When (T_1, T_2)=(H, H), terminals for step up circuits and VR are open, because the Step up circuits and Voltage adjust circuits do not operate.

○ Power Supply applications

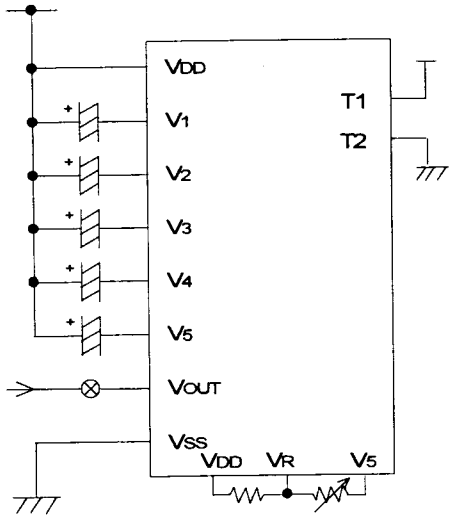
(1) External power supply operation.



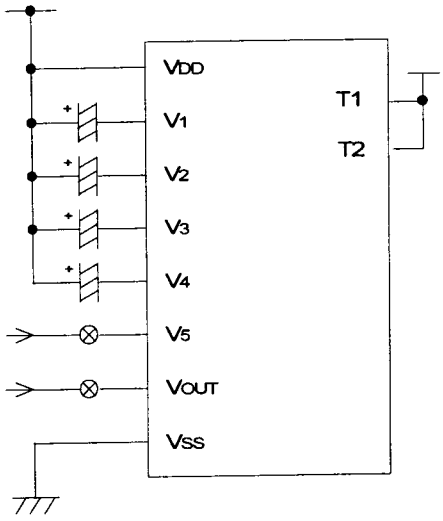
(2)Internal power supply operation.
(Voltage Booster, Voltage Adj., Buffer(V/F))
Internal power supply ON (instruction) (T1,T2)=(L,L)



(3)External power supply operation with
Voltage Adjustment, Buffer(V/F)
Internal power supply ON (Instruction) (T1,T2) = (H,L)



(4)External power supply operation adjusted
Voltage to V5.
Internal power supply ON (Instruction) (T1,T2) =(H,H)



* ⊗ : These switches should be open during the power save mode.

(2) Instruction

The NJU6675 distinguishes the signal on the data bus by combination of A0, $\overline{RD}$ and $\overline{WR}$. The decode of the instruction and execution are performs only depend on the internal timing only neither the external clock. In case of serial interface, the data input as MSB first serially.
The Table. 4 shows the instruction codes of the NJU6675.

Table 4. Instruction Code

Instruction		Code											Description
		A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD Display ON/OFF 0:OFF 1:ON
(2)	Page Address Set	0	1	0	1	0	1	1	*	Page Address			Set the page of DD RAM to the Page Address Register
(3)	Column Address Set High Order 3bits	0	1	0	0	0	0	1	0	High Order Column Add.			Set the Higher order 3 bits Column Address to the Reg.
(4)	Column Address Set Lower Order 4bits	0	1	0	0	0	0	0	Lower Order Column Add.				Set the Lower order 4 bits Column Address to the Reg.
(5)	Status Read	0	0	1	Status				0	0	0	0	Read out the internal Status
(6)	Write Display Data	1	1	0	Write Data								Write the data into the Display Data RAM
(7)	Read Display Data	1	0	1	Read Data								Read the data from the Display Data RAM
(8)	ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	Set the DD RAM vs Segment 0:Normal 1:Inverse
(9)	Normal or Inverse of ON/OFF Set	0	1	0	1	0	1	0	0	1	1	0 1	Inverse the ON and OFF Display 0:Normal 1:Inverse
(10)	Whole Display ON /Normal Display	0	1	0	1	0	1	0	0	1	0	0 1	Whole Display Turns ON 0:Normal 1:Whole Disp. ON
(11)	Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increment the Column Address Register when writing but no-change when reading
(12)	End	0	1	0	1	1	1	0	1	1	1	0	Release from the Read Modify write Mode
(13)	Reset	0	1	0	1	1	1	0	0	0	1	0	Initialize the internal Circuits
(14)	Output Assignment Register Set	0	1	0	1	1	0	0	A3	*	*	*	Set the scanning order of common drivers to the Register
(15)	Internal Power Supply ON/OFF	0	1	0	0	0	1	0	0	1	0	0 1	0:Int. Power Supply OFF 1:Int. Power Supply ON
(16)	LCD Driving Voltage Set	0	1	0	1	1	1	0	1	1	0	1	Set LCD Driving Voltage after the internal (external) power supply is turned on
(17)	EVR Register Set	0	1	0	1	0	0	0	Setting Data				Set the V5 output level to the EVR register
(18)	Power Save (Dual Command)	0 0	1 1	0 0	1 1	0 0	1 1	0 0	1 0	1 1	1 0	0 1	Set the Power Save Mode

(*:Don't Care)

(3) Explanation of Instruction Code

(a) Display On/Off

This instruction executes whole display On/Off without relationship of the data in the Display Data RAM and internal conditions.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

D 0:Display Off
1:Display On

(b) Page Address Set

When MPU accesses the Display Data RAM, the page address must be selected before the data writing. The access to the Display Data RAM is available by the page and column address set (Refer the Fig. 1.). The page address change does not influence with the display.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	*	A2	A1	A0

(*:Don't care)

A2	A1	A0	Page
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

(c) Column Address

When MPU accesses the Display Data RAM, the page address set(refer(b)) and column address set are required before the data writing. The column address set requires twice address set which are higher order 3 bits address set and lower order 4 bits. When the MPU accesses the Display Data RAM sequentially, the column address is increase one by one automatically, therefore, the MPU can access only the data sequentially without address set.

After writing 1page data ,page address setting is required due to page address doesn't increase automatically. The increment of the column address is stopped at the address of (60)H automatically, and the page address is not changed even if the column address increase to (60)H and stop. In this time the page address is not changed.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	0	0	1	*	A6	A5	A4	Higher Order
0	1	0	0	0	0	0	A3	A2	A1	A0	Lower Order

A6	A5	A4	A3	A2	A1	A0	Column Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			:				:
			:				:
1	0	1	1	1	1	1	5F

(d) Status Read

This instruction reads out the internal status of "BUSY", "ADC", "ON/OFF" and "RESET".

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY : BUSY=1 indicate the operating or the Reset cycle.
The instruction can be input after the BUSY status change to "0".

ADC : Indicate the output correspondence of column (segment) address and segment driver.
0 :Counterclockwise Output (Inverse) Column Address 95-n <----> Segment Driver n
1 :Clockwise Output (Normal) Column Address n <----> Segment Driver n
(Note) The data "0=Inverse" and "1=Normal" of ADC is inverted with the ADC select Instruction of "1=Inverse" and "0=Normal".

ON/OFF : Indicate the whole display On/Off status.
0 : Whole Display "On
1 : Whole Display "Off"
(Note) The data "0=On" and "1=Off" of Display On/Off status read out is inverted with the Display On/Off instruction data of "1=On" and "0=Off".

RESET : Indicate the initializing period by $\overline{RES}$ signal or reset instruction.
0 : -
1 : Initialization Period

(e) Write Display Data

This instruction writes the 8-bit data on the data bus into the Display Data RAM. The column address increases "1" automatically after data writing, therefore, the MPU can write the 8-bit data into the Display Data RAM continuously without any address setting after the start address setting.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	WRITE DATA							

(f) Read Display Data

This instruction reads out the 8-bit data from Display Data RAM which addressed by the column and page address. The column address increase "1" automatically after data reading out, therefore, the MPU can read out the 8-bit data from the Display Data RAM without any address setting after the start address setting. One time of dummy read must operate after column address set as the explanation in "(5-5) Access to the Display Data RAM and Internal Register". In the serial interface mode, the display data is not read out.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	READ DATA							

(g) ADC Select

This instruction set the correspondence of column address in the Display Data RAM and segment driver output. (See Fig. 1.) By this instruction, the order of segment output can be changed by the software, and no restriction of the LSI placement against the LCD panel.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

D 0 : Clockwise Output (Normal)

1 : Counterclockwise Output (Inverse)

(h) Normal or Inverse On/Off Set

This instruction changes the condition of display turn on and off as normal or inverse. The contents of Display Data RAM is not changed by this instruction execution.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

D 0 : Normal RAM data "1" correspond to "On"

1 : Inverse RAM data "0" correspond to "On"

(i) Whole Display On

This instruction turns on the all pixels independent of the contents of the Display Data RAM. In this time, the contents of Display Data RAM is not changed and kept. This instruction takes precedence over the "Normal or Inverse On/Off Set Instruction".

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

D 0 : Normal Display

1 : Whole Display turn on

When Whole Display On Instruction is executed in the Display Off status, the internal circuits go to the power save mode (refer to the (s) Power Save).

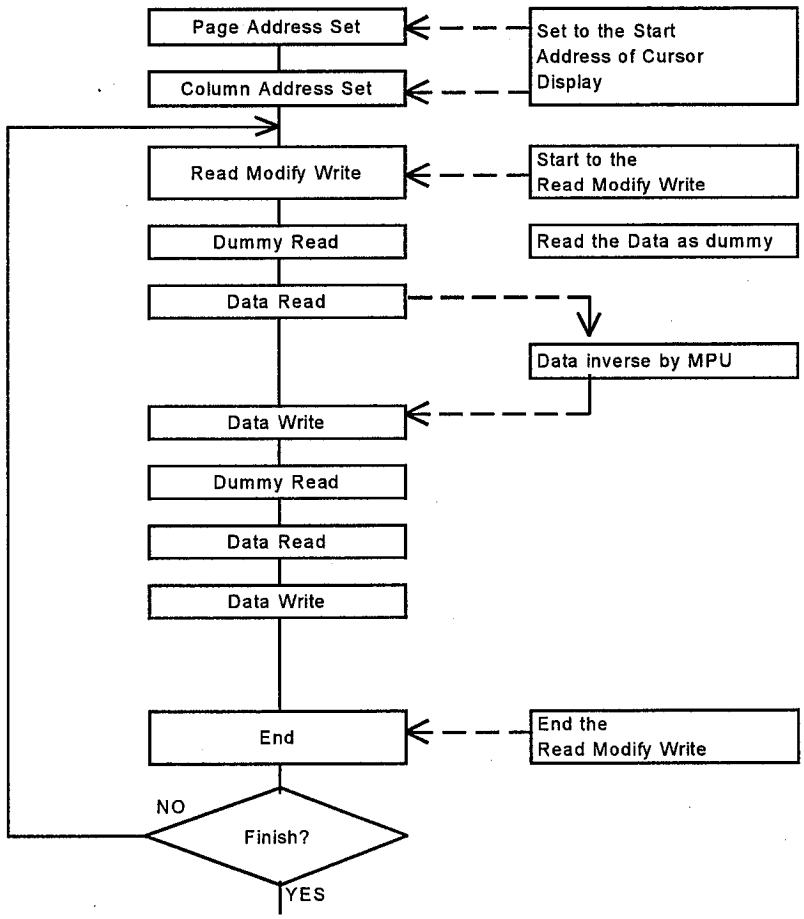
(j) Read Modify Write

This instruction sets the Read Modify Write Mode for the column address increment control. In mode of the Read Modify Mode Write, the column address increases "1" automatically when the Display Data Write Instruction is executed, but the address does not change when the Display Data Read Instruction is executed. This status is continued until End instruction execution. When the End instruction is input.,the column address goes back to the start address bufore the Read Modify Write instruction input. This function reduces the load of MPU for repeating the display data change in the fixed area (ex. cursor blink).

A0	$\overline{RD}$	R/$\overline{W}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	1	1	0	0	0	0	0

Note) In mode of the Read Modify Write, any instructions except forp Column Address Set can execute.

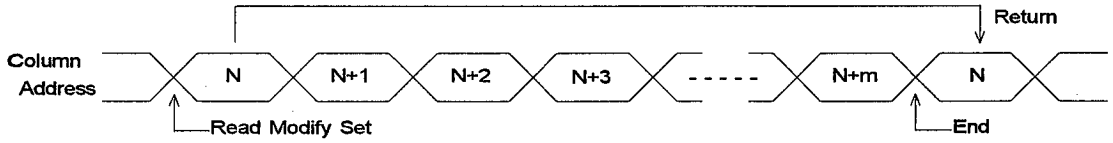
(k) Sequence of cursor blink display



(l) End

This instruction release the Read Modify Write mode and the column address back to the address where the read modify write mode setting.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0



(m) Reset

This instruction executes the following initialization.

Initialization

1 Set the Address (00)H into the Column Address Counter.
2 Set the page "0" into the Page Address Register.
3 Select the D3 of the Output Assignment Register to "0".
4 Set 0 to the EVR Register to (00)H.

In this time, the Display Data RAM is not influenced.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The reset signal input to the $\overline{RES}$ terminal (hardware reset) must be input for the power on initialization. Reset instruction does not perform completely instead of hardware reset using the $\overline{RES}$ terminal.

(n) Output Assignment Register

This instruction sets the common driver scanning order.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	A3	*	*	*

(*:Don't care)

A3 : Set the scanning order. (Refer to 1-6)

(o) Internal Power Supply

This instruction set the condition of internal Power Supply On/Off. Step up circuits, Voltage Regulator and Voltage Follower operate at On. To operate the step up circuits, the oscillation circuits must be operating.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	1	0	D

D 0 : Internal Power Supply Off
1 : Internal Power Supply On

The internal Power Supply must be Off when external power supply using.

(p) LCD Driving Voltage Set

This instruction controls LCD driving waveform output through the COM/SEG terminals.

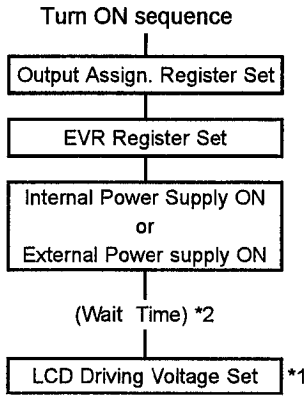
A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	0	1

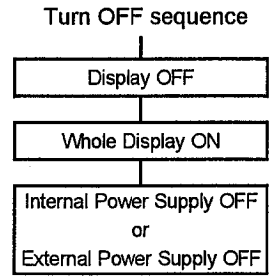
The NJU6675 contains low power LCD driving voltage generator circuit reducing own operation current. Therefore, it requires the following sequence procedures at power on for power source stabilized operation.

● LCD driving power supply ON/OFF sequences

The following sequences are required when the power supply is turned On/Off.

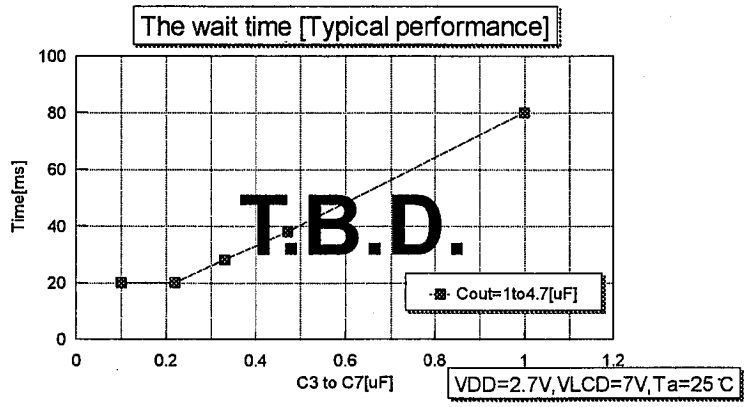
When the power supply is turned on again after the turn off (by the power save instruction), the power save release sequence (s) is required.





*1 This instruction is required in both cases of the internal and external power supply. Until "LCD driving voltage Set" execution, NJU6675 operating current is higher than usual state and all COM/SEG terminals output V_{DD} level continuously.

*2 The wait time depends on the C_3 to C_7, C_{OUT} capasitors (refer(4) (d)Fig.4), V_{DD} and V_{LCD} voltage. Therefore it requires the actual evaluation using the LCD module to get the correct time. (Refer to the following graph.)



(q) EVR Register Set

This instruction controls voltage adjustment circuits of internal LCD power supply and changes LCD driving voltage "V5". Finally, it adjusts the contrast of LCD display. By setting a data into EVR register. V_5 output voltage selects one condition out of 16-voltage conditions. The range of V_5 voltage is adjusted by setting external resistors as mentioned in "(4)(b) Voltage Adjust Circuits".

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	A3	A2	A1	A0

A3	A2	A1	A0	VLCD
0	0	0	0	Low
		:		:
		:		:
1	1	1	1	High

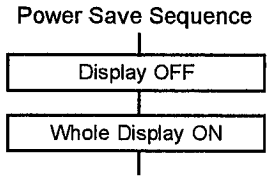
$V_{LCD}=V_{DD}-V_5$
When EVR doesn't use, set the EVR register to (0,0,0,0).

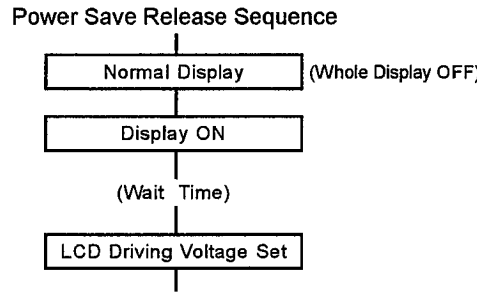
(r) Power Save(Dual Command)

When both of Display Off and Whole Display On are executed, the internal circuits go to the power save mode and the operating current is reduced as same as the stand by current.
The internal status in the Power Save Mode is shown in follows;

1 Stop the Oscillation Circuits and Internal Power Supply Circuits operation.
2 Stop the LCD driving. Segment and Common drivers output V_{DD} level.
3 Keep the display data and operating mode just before the power save mode.
4 All of LCD driving bias voltage fix to the V_{DD} level.

The power save and its release perform according to the following sequences.



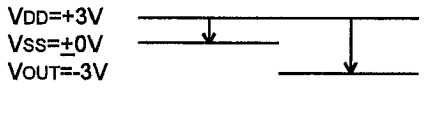


*1 In the power save sequence, the power save mode is started after the second instruction "whole Display ON".
*2 In the power save release sequence, the power save mode is released after the Normal Display instruction (Whole display OFF).
The instruction of display ON is input at any timing after the instruction of normal display in power save release sequence.
*3 Until "LCD driving voltage set to ON" execution, NJU6675 operating current is higher than usual state and all COM/SEG terminals output V_{DD} level continuously.
*4 In case of the external power supply for LCD driving, it should be turned off and made condition like as disconnection or connection to V_{DD} before the power save mode or at the same time. In this time, V_{OUT} terminal should be made condition like as disconnection or connection to the lowest voltage of the system. (V_5 level from the external power supply.)

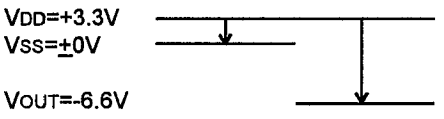
(4) Internal Power Supply

(a) Voltage tripler

Three times negative voltage (V_{DD} common) of the voltage V_{DD}-V_{SS} is output from V_{OUT} terminal when connecting three capacitor between $C1^+$ and $C1^-$, $C2^+$ and $C2^-$, V_{SS} and V_{OUT}. In case of the voltage doubler operation, connect the two capacitor between $C2^+$ and $C2^-$, V_{SS} and V_{OUT}, then connect the $C1^+$ and $C2^+$ terminals. Step up circuits like as Voltage Tripler or Doubler using a oscillation circuits output as its clock signal, therefore, the oscillation circuits operation is required when step up operation. The voltage relation regarding the step up circuits is shown in below. When voltage tripler operation, the operation voltage V_{DD} should be less than 3.3V.



Voltage relation in Doubler



Voltage relation in Tripler

(b)Voltage Adjust Circuits

The step up voltage of V_{OUT} output from V_5 through the voltage adjust circuits for LCD driving. The output voltage of V_5 is adjusted by changing the Ra and Rb within the range of $|V_5| < |V_{OUT}|$. The output voltage is calculated by the following formula.

$$V_{LCD} = V_{DD}-V_5 = (1+Rb/Ra) \times V_{REG} \quad \text{---- 1}$$

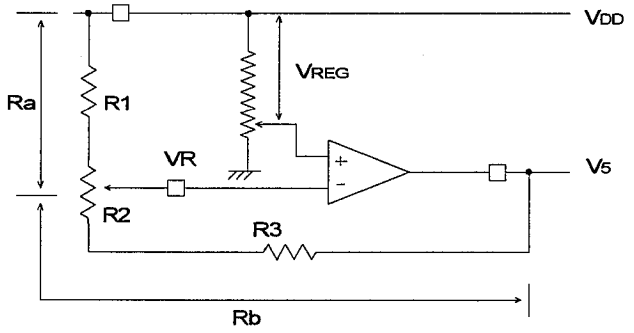


Fig.3

The voltage of V_{REG} is a standard voltage produced from built-in bleeder resistance. And V_{REG} is possible to be fine-adjusted by EVR functions mentioned in (c).

For fine-adjustment of V_5, R2 as variable resistor, R1 and R3 as fixed constant should be connected to V_{DD} terminal, VR and V_5, as shown in Fig3.

[Design example for R1, R2 and R3 / Reference]

- R1+R2+R3=5MΩ (Determined by the current flown between V_{DD}-V_5)
- Variable voltage range by the R2. -3V to -4.5V (V_{LCD}=V_{DD}-V_5 ---> 6.0V to 7.5V) (Determined by the LCD electrical characteristics)
- V_{REG}=3V(In case of EVR=(0F)H)
- R1, R2 and R3 are calculated by above conditions and the formula of 1 to mentioned below;

  R1=2.0MΩ, R2=0.5MΩ, R3=2.5MΩ

* If the power supply voltage between V_{DD} and V_{SS} changes, V_5 changes too. Therefore the power supply voltage should be stabilized for V_5 stable operation.

(c) Contrast Adjustment by using the EVR function

The EVR controls voltage of V_{REG} by instruction and changes voltage of V_5.

As result, LCD display contrast is adjusted by V_5. The EVR selects a voltage of V_{REG} in the following 16 conditions by setting 4bits data into the EVR register.

In case of EVR operation, T_1 terminal and T_2 require to set couples of value as (L,L), (L,H) and (H,L) excepting for (H,H) and the internal power supply must turn on by instruction.

EVR register		V_{REG} [V]	V_{LCD}
$(00)_H$	(0,0,0,0)	(135/150)x(V_{DD}-Vss)	Low
$(01)_H$	(0,0,0,1)	(136/150)x(V_{DD}-Vss)	:
$(02)_H$	(0,0,1,0)	(137/150)x(V_{DD}-Vss)	:
:	:	:	:
:	:	:	:
$(0D)_H$	(1,1,0,1)	(148/150)x(V_{DD}-Vss)	:
$(0E)_H$	(1,1,1,0)	(149/150)x(V_{DD}-Vss)	:
$(0F)_H$	(1,1,1,1)	(150/150)x(V_{DD}-Vss)	High

● Adjustable range of the LCD driving voltage by EVR function

The adjustable range is decided by the power supply voltage VDD and the ratio of external resistors Ra and Rb.

[Design example for the adjustable range / Reference]

- Condition V_{DD}=3.0V, V_{SS}=0V

  Ra=1MΩ, Rb=1MΩ (Ra:Rb=1:1)

The adjustable range and the step voltage are calculated as follows in the above condition.

In case of setting $(00)_H$ in the EVR register,

V_{LCD} = ((Ra+Rb)/Ra)xV_{REG}

= (2/1)x[(135/150)x3.0]

= 5.4V

In case of setting $(0F)_H$ in the EVR register,

V_{LCD} = ((Ra+Rb)/Ra)xV_{REG}

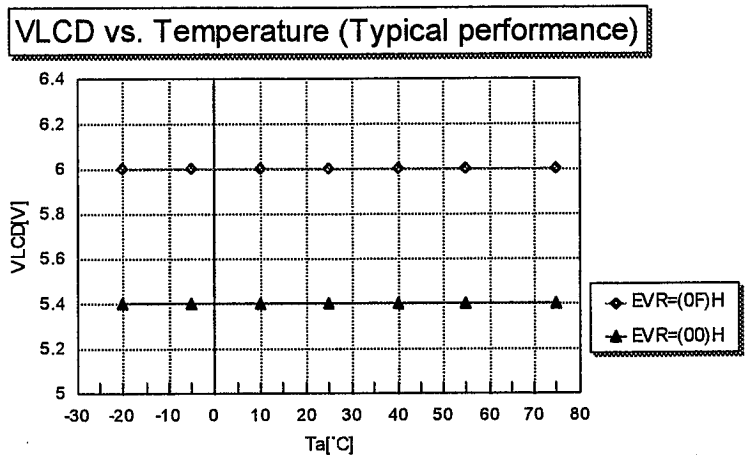
= (2/1)x[(150/150)x3.0]

= 6.0V

	Min.$(00)_H$	Max.$(0F)_H$	
Adjustable Range	5.4	6.0	[V]
Step Voltage	40		[mV]

*) The V_{LCD} operating temperature. Please refer to the following graphs.

(conditions) V_{DD} = 3V
Ra=1MΩ, Rb=1MΩ (Ra:Rb = 1:1)
Voltage tripler

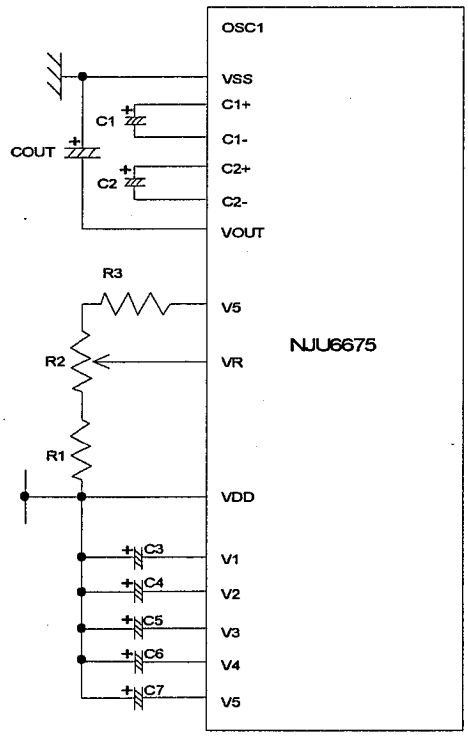


(d) LCD Driving Voltage Generation Circuits

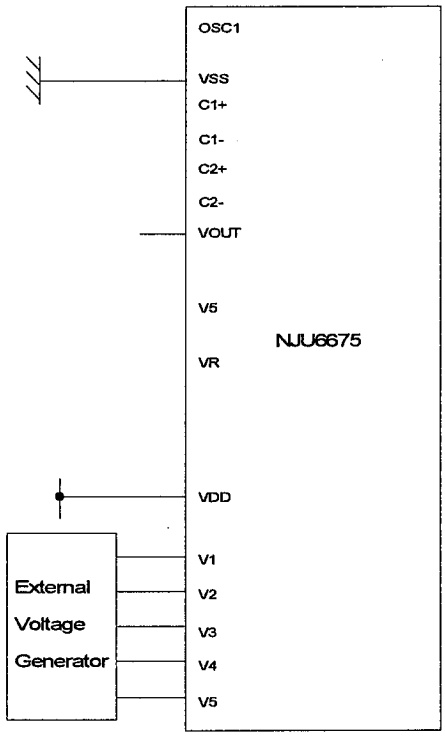
The LCD driving bias voltage of V_1,V_2,V_3,V_4 are generated internally by dividing the V_5 voltage with the internal bleeder resistance. And it is supplied to the LCD driving circuits after the impedance conversion with voltage follower circuit.

As shown in Fig. 4, Five capacitors are required to connect to each LCD driving voltage terminal for voltage stabilizing. And the value of capacitors C3, C4, C5, C6 and C7 are determined depending on the actual LCD panel display evaluation.

Using the internal Power Supply



Using the external Power Supply



Reference set up value

$V_{LCD} = V_{DD} - V_5 \fallingdotseq 6.0$ to $7.5V$

Item	Value
C_{OUT}	4.7 to 10uF
C1,C2	4.7 to 10uF
C3 to C7	0.1 to 0.47uF
R1	2.0MΩ
R2	0.5MΩ
R3	2.5MΩ

Fig.4

*1 Short wiring or sealed wiring to the VR terminal is required due to the high impedance of VR terminal.

*2 Following connection of V_{OUT} is required when external power supply using.

When $V_{SS} > V_5$ --- $V_{OUT}=V_5$

When $V_{SS} \leq V_5$ --- $V_{OUT}=V_{SS}$

(5) MPU Interface

(5-1) Interface type selection

NJU6675 interfaces with MPU by 8-bit bi-directional data bus (D_7 to D_0) or serial interface (SI). The 8-bit parallel or serial interface is determined by a condition of the P/S terminal connecting to "H" or "L" level as shown in Table 5. In case of the serial interface, status and RAM data read out operation is impossible.

Table 5

P/S	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	SI	SCL	D_0 to D_7
H	Parallel	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	-	-	D_0 to D_7
L	Serial	$\overline{CS}$	A0	-	-	-	SI	SCL	-

(5-2) Parallel Interface

The NJU6675 interfaces to 68 or 80 type MPU directly when setting the parallel interface (P/S="H") is selected. 68 type MPU or 80 is determined by the condition of C86 terminal connecting to "H" or "L" as shown in table 6.

Table 6

C86	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D_0 to D_7
H	68 type MPU	$\overline{CS}$	A0	E	R/W	D_0 to D_7
L	80 type MPU	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D_0 to D_7

(5-3) Discrimination of Data Bus Signal

The NJU6675 discriminates the mean of signal on the data bus by the combination of A0, E, R/W, and ($\overline{RD}$,$\overline{WR}$) signals as shown in Table 7.

Table 7

Common	68 type	80 type		Function
A0	R/W	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Read Display Data
1	0	1	0	Write Display Data
0	1	0	1	Status Read
0	0	1	0	Write into the Register(Instruction)

(5-4) Serial Interface.(P/S="L")

Serial interface circuits consist of 8 bits shift register and 3 bits counter. SI and SCL input are activated when the chip select terminal $\overline{CS}$ set to "L"and P/S terminal set to "L". The 8 bits shift register and 3 bits counter are reset to the initial condition when chip is not selected. The data input from SI terminal is MSB first like as the order of D_7,D_6,・・・・・D_0, and the data are entered into the shift register synchronizing with the rise edge of the serial clock SCL. The data in the shift register are converted to parallel data at the 8th serial clock rise edge input. Discrimination of the display data or instruction of the serial input data is executed by the condition of A0 at the 8th serial clock rise edge. A0="H" is display data and A0="L" is instruction. When $\overline{RES}$ terminal becomes "L" or $\overline{CS}$ terminal becomes "H" before 8th serial clock rise edge, NJU6675 recognizes them as a instruction data incorrectly. Therefore a unit of serial data must be structured by 8-bit. The time chart for the serial interface is shown in Fig. 5. To avoid the noise trouble, the short wiring is required for the SCL input.

Note) The read out function, such as the status or RAM data read out, is not supported in this serial interface .

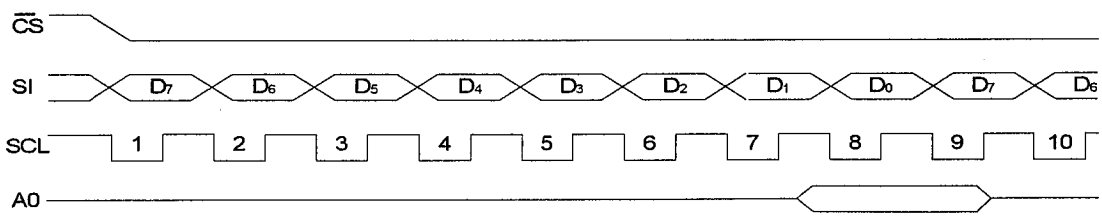


Fig.5

(5-5) Access to the Display Data RAM and Internal Register.

The NJU6675 is operating as one of pipe-line processor by the bus-holder connecting to the internal data bus to adjust the operation frequency between MPU and the Display Data RAM or Internal Register.

For example, when the MPU reads out the data from the Display Data RAM, the read out data in the data read cycle (dummy read) is held in the bus-holder, then it is read out from the bus-holder to the system bus at the next data read cycle. When the MPU writes the data into the Display Data RAM, the data is held in the bus-holder, then it is written into the Display Data RAM by the next data write cycle.

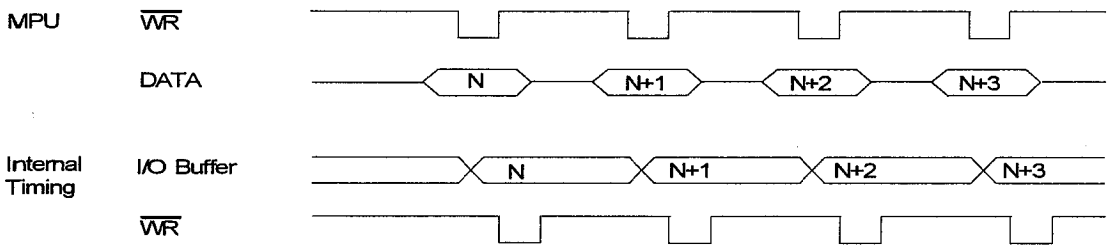
Therefore high speed data transmission between MPU and NJU6675 is available because of it is not limited by the t_{ACC} and t_{DS} as display data RAM access time and is limited by the system cycle time (R) or (W).

If the cycle time is not be kept in the MPU operation, NOP should be inserted to the system instead of the waiting operation.

The read out operation does not read out the data in the pointed address just after the address set operation. And second read out operation can read out the data correctly from the pointed address.

Therefore, one dummy read is required after address setting or write cycle as shown in Fig. 6.

● Write Operation



● Read Operation

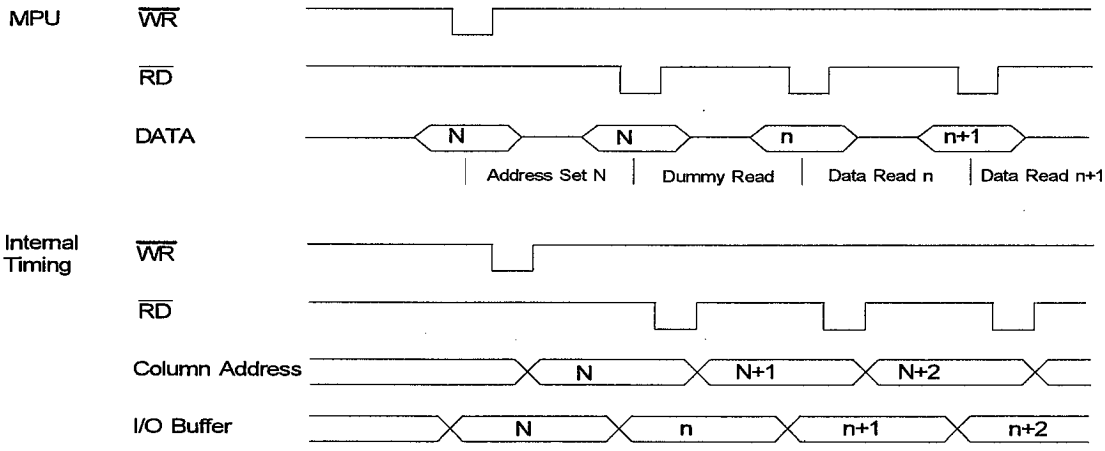


Fig.6

(5-6) Chip Select

$\overline{CS}$ is Chip Select terminal. In case of $\overline{CS}$="L". the interface with MPU is available. In case of $\overline{CS}$="H" ,the D_0 to D_7 are high impedance and A0, $\overline{RD}$, $\overline{WR}$, SI and SCL inputs are ignored. If the serial interface is selected when $\overline{CS}$="H", the shift register and counter are reset. However, the reset is always operated in any conditions of $\overline{CS}$.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (1)	V_{DD}	-0.3 to +7.0	V
		-0.3 to +3.6(used Tripler)	V
Supply Voltage (2)	V_5	V_{DD}-11.0 to V_{DD}+0.3	V
Supply Voltage (3)	V_1 to V_4	V_5 to V_{DD}+0.3	V
Input Voltage	V_{IN}	-0.3 to V_{DD}+0.3	V
Operating Temperature	T_{opr}	-30 to +80	°C
Storage Temperature	T_{stg}	-55 to +125 (Chip)	°C
		-55 to +100 (TCP)	

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 2) All voltage values are specified as V_{SS}=0 V.

Note 3) The relation : $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$; $V_{DD} > V_{SS} \geq V_{OUT}$ must be maintained.

Note 4) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the voltage converter.

■ ELECTRICAL CHARACTERISTICS (1)

(V_{DD}=2.4V to 3.3V, V_{SS}=0V, Ta=-30 to +80° C)

PARAMETE		SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	Note
Operating Voltage(1)		V_{DD}			2.4		3.3	V	5
Operating Voltage(2)		V_5			V_{DD}-10.0		V_{DD}-6.0	V	
		V_1,V_2	V_{LCD}= V_{DD}-V_5		V_{DD}-0.5V_{LCD}		V_{DD}		
		V_3,V_4			V_5		V_{DD}-0.5V_{LCD}		
Input Voltage	High Level	V_{IHC1}	D_0...D_7,A0, CS,$\overline{RES}$,$\overline{RD}$,$\overline{WR}$,C86,SI, SCL,P/S Terminals		0.8V_{DD}		V_{DD}	V	
	Low Level	V_{ILC1}			V_{SS}		0.2V_{DD}	V	
Output Voltage	High Level	V_{OHC11}	D_0...D_7 Terminals	I_{OH}=-0.5mA	0.8V_{DD}		V_{DD}	V	
	Low Level	V_{OLC11}		I_{OL}= 0.5mA	V_{SS}		0.2V_{DD}	V	
Input Leakage Current		I_{LIO}	All Input terminals		- 1.0		1.0	uA	
Driver On-resistance		R_{ON1}	Ta=25°C	V_{LCD}=10.0V		2.0	3.0	kΩ	7
		R_{ON2}		V_{LCD}=8.0V		3.0	4.5		
Stand-by Current		I_{DDQ}	during Power save Mode			0.05	5.0	uA	8
Operating Current		I_{DD12}	Display V_{LCD}=8.0V			16	25	uA	
		I_{DD21}	Accessing f_{CYC}=200kHz			170	240		9

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
Input Terminal Capacitance		C_{IN}	A0,$\overline{CS}$,$\overline{RES}$,$\overline{RD}$,$\overline{WR}$,C86,SI, SCL,P/S,T1,T2,D_0...D_7 Ta=25 °C		10		pF	
Oscillation Frequency		f_{OSC}	Ta=25 °C	14.5	18	21	kHz	
Voltage Tripler	Output Volt.	V_{OUT1}	Vss-V_{LCD}, used Tripler, V_{DD}=3.3V	- 6.6		-6.4	V	
	On-resistance	R_{TRI}	V_{DD}=3V;C_{OUT}=4.7uF used Tripler		600	1000	Ω	
	Adjustment range of LCD Driving Volt.	V_{OUT2}	Tripler Circuit "OFF"	V_{DD}-10.0V		V_{DD}-6.0V	V	11
	Voltage Follower	V_5	Voltage Adjustment Circuit "OFF"	V_{DD}-10.0V		V_{DD}-6.0V	V	
	Operating Current	I_{OUT1}	V_{DD}=3V, V_{LCD}=8V COM/SEG Terminals Open No Access Display Checkered pattern		62	148.8	uA	12
		I_{OUT2}			22	45		
		I_{OUT3}			21	43		
	Voltage Reg.	$V_{REG\%}$	V_{DD}=3V,Ta=25 °C			3	%	13

Note 5) NJU6675 can operate wide operating range, but it is not guarantee immediate voltage changing during the accessing of the MPU.

Note 6) Apply to the High-impedance state of the D_0 to D_7 terminals.

Note 7) R_{ON} is the resistance values between power supply terminals(V_1, V_2, V_3, V_4) and each output terminals of common and segment supplied by 0.1V. This is specified within the range of supply voltage (2).

Note 8,9,12) Apply to current after "LCD Driving Voltage Set".

Note 8) Apply to the external display clock operation in no access from the MPU and no use internal power supply circuits.

Note 9) Apply to the condition of cyclic (tcyc) inverted data input continuously in no use internal power supply circuits. The operating current during the accessing is proportionate to the access frequency. In the no accessing period, it is as same as I_{DD1X}.

Note 10) Supply voltage (V_{DD}) range for internal Voltage Tripler operation.

Note 11) LCD driving voltage V_5 can be adjusted within the voltage follower operating range.

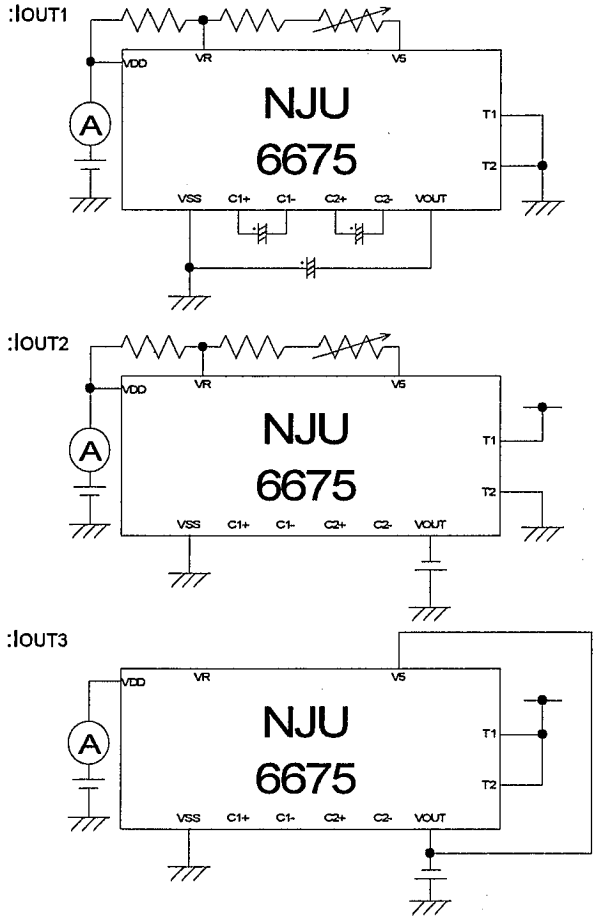
Note 12) Each operating current of voltage supply circuits block is specified under below table conditions.

SYMBOL	Status		Operating Condition				External Voltage Supply (Input Terminal)
	T_1	T_2	Internal Oscillator	Voltage Tripler	Voltage Adjustment	Voltage Follower	
I_{OUT1}	L	*	Validity	Validity	Validity	Validity	Unuse
I_{OUT2}	H	L	Validity	Invalidity	Validity	Validity	Use(V_{OUT})
I_{OUT3}	H	H	Validity	Invalidity	Invalidity	Validity	Use(V_{OUT},V_5)

(* = Don't Care)

Note 13) Apply to the precision of the voltage between V_{DD} and V_5 with EVR function.

■ MEASUREMENT BLOCK DIAGRAM



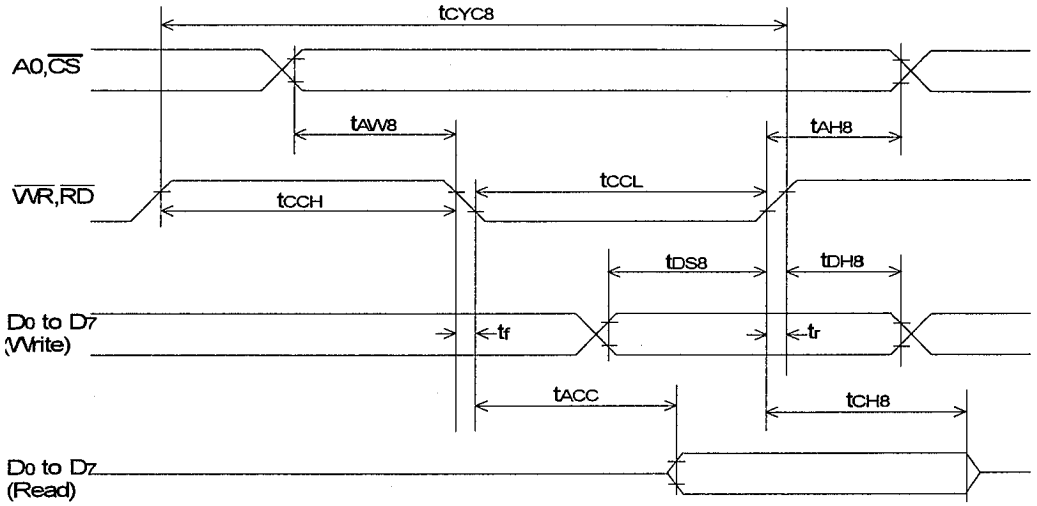
■ **ELECTRICAL CHARACTERISTICS (2)** (VDD=2.4V to 3.3V, VSS=0V, Ta=-30 to +80° C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
Reset time	t_R	$\overline{RES}$ Terminal	1.0			us	14
Reset "L" Level Pulse Width	t_{RW}	$\overline{RES}$ Terminal	10			us	15

Note 14) Specified from the rising edge of $\overline{RES}$ to finish the internal circuit reset.
Note 15) Specified minimum pulse width of $\overline{RES}$ signal. Over than t_{RW} "L" input should be required for correct reset operation.

■ BUS TIMING CHARACTERISTICS

- Read/Write operation sequence (80 Type MPU)



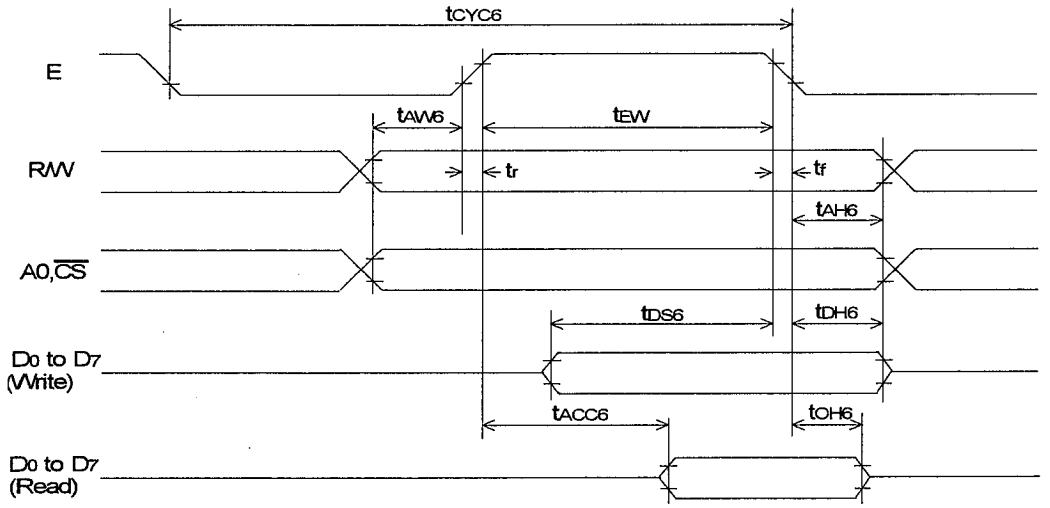
(VDD=2.4V to 3.3V,Ta=-30 to +80°C)

PARAMETER			SYMBOL	MIN.	MAX.	CONDITION	UNIT
Address Hold Time		A0,CS Terminals	tAH8	45			ns
Address Set Up Time			tAW8	45			ns
System Cycle Time	WR	WR,RD Terminals	tCYC8 (W)	770			ns
	RD		tCYC8 (R)	1025			ns
Control Pulse Width	WR,"L"		tCCL(W)	85			ns
	RD,"L"		tCCL(R)	340			ns
	"H"		tCCH	685			ns
Data Set Up Time		D0 to D7 Terminals	tDS8	210			ns
Data Hold Time			tDH8	70			ns
RD Access Time			tACC8		340	CL=100pF	ns
Output Disable Time			tCH8	0	85		ns
Rise Time, Fall Time		CS, WR, RD, A0, D0 to D7 Terminals	tr,tf		15		ns

Note 16) Rise time (tr) and fall time (tf) of input signal should be less than 15ns.

Note 17) Each timing is specified based on 0.2xVDD and 0.8xVDD.

- Read/Write operation sequence (68 Type MPU)



(V_{DD}=2.4V to 3.3V, Ta=-30 to +80°C)

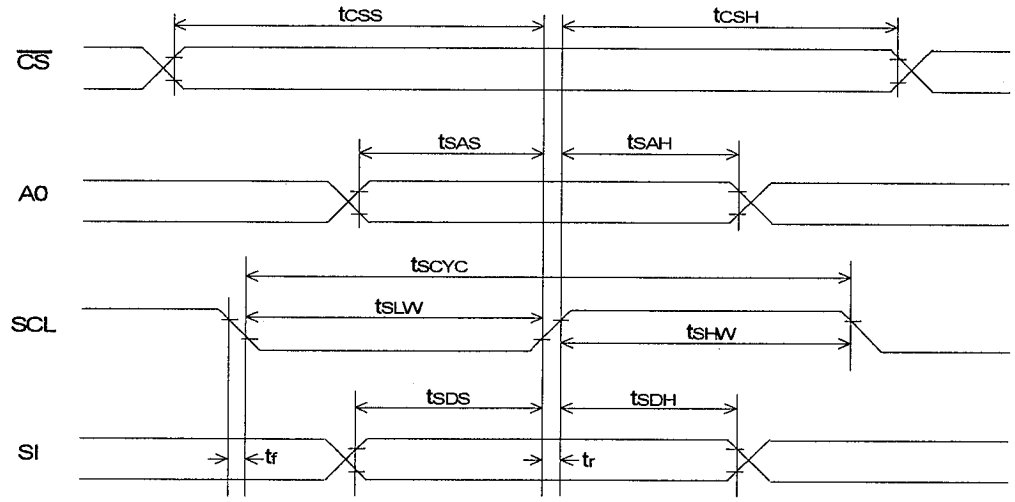
PARAMETER			SYMBOL	MIN.	MAX.	CONDITION	UNIT
Address Hold Time		A0,CS,R/W Terminals	t_{AH6}	45			ns
Address Set Up Time			t_{AW6}	45			ns
System Cycle Time(W)			t_{CYC6}(W)	770			ns
System Cycle Time(R)			t_{CYC6}(R)	1025			ns
Enable Pulse Width	Read"H"	E Terminal	t_{EWH}	85			ns
	Write"H"			340			ns
	"L"		t_{EWL}	685			
Data Set Up Time		D0 to D7 Terminals	t_{DS6}	210			ns
Data Hold Time			t_{DH6}	70			ns
Access Time			t_{ACC6}		240	CL=100pF	ns
Output Disable Time			t_{OH6}	0	80		ns
Rise Time, Fall Time		A0, CS, R/W, E, D0 to D7 Terminals	t_r,t_f		15		ns

Note 18) t_{CYC6} indicates the E signal cycle during the $\overline{CS}$ activation period. The System Cycle Time must be required after $\overline{CS}$ becomes active.

Note 19) Rise time (t_r) and fall time (t_f) of input signal should be less than 15ns.

Note 20) Each timing is specified based on 0.2xV_{DD} and 0.8xV_{DD}.

- Write operation sequence (Serial Interface)



(VDD=2.4V to 3.3V,Ta=-30 to +80°C)

PARAMETER		SYMBOL	MIN.	MAX.	CONDITION	UNIT
Serial Clock cycle	SCL Terminal	tSCYC	1000			ns
SCL "H" pulse width		tSHW	300			ns
SCL "L" pulse width		tSLW	300			ns
Address Set Up Time	A0 Terminal	tSAS	250			ns
Address Hold Time		tSAH	400			ns
Data Set Up Time	SI Terminal	tSDS	250			ns
Data Hold Time		tSDH	100			ns
$\overline{CS}$-SCL Time	$\overline{CS}$ Terminal	tCSS	60			ns
		tCSH	800			ns
Rise Time, Fall Time	SCL, A0, $\overline{CS}$, SI Terminals	tr,tf		15		ns

Note 21) Rise time (tr) and fall time (tf) of input signal should be less than 15ns.
Note 22) Each timing is specified based on 0.2xVDD and 0.8xVDD.

■ LCD DRIVING WAVEFORM

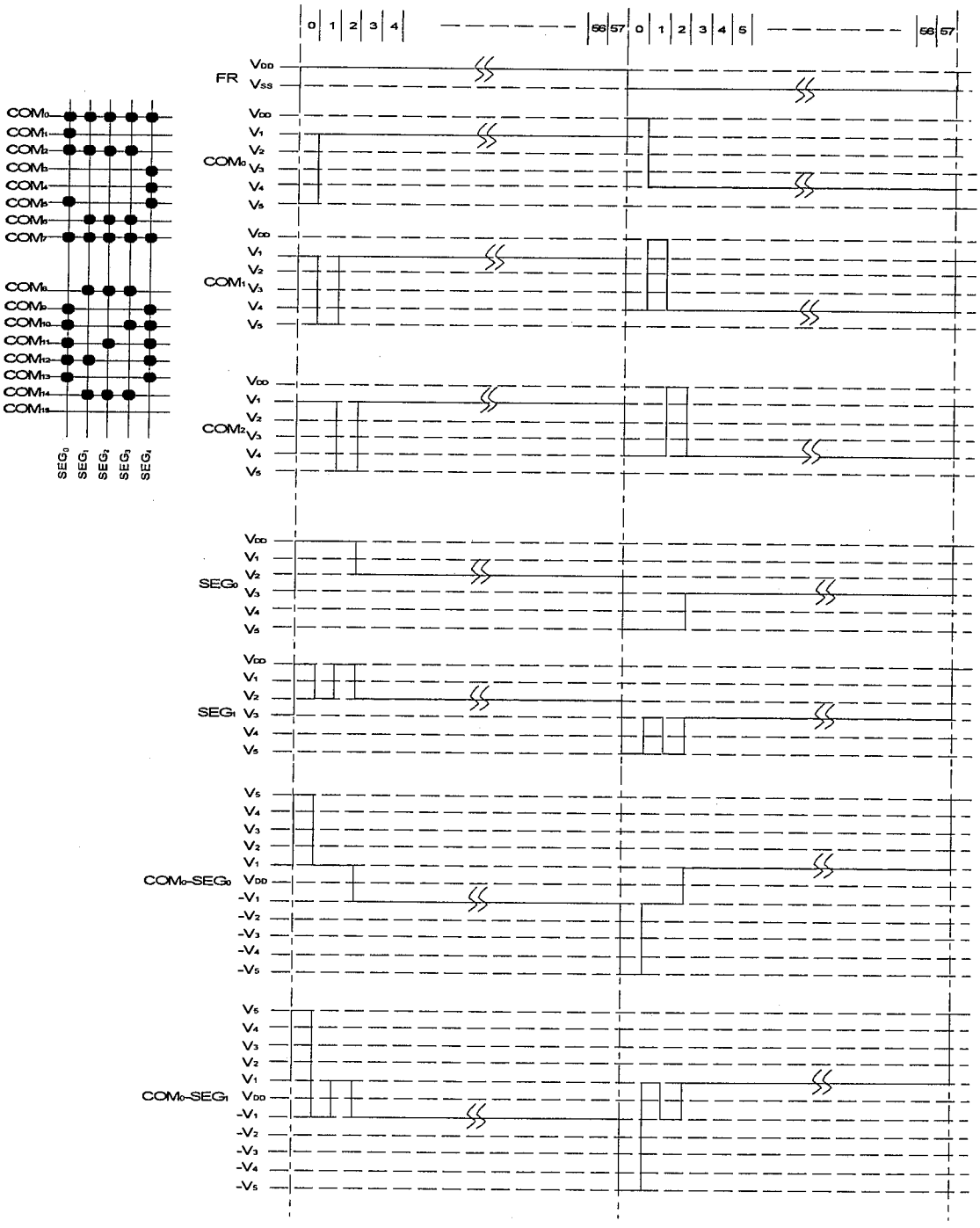


Fig.7

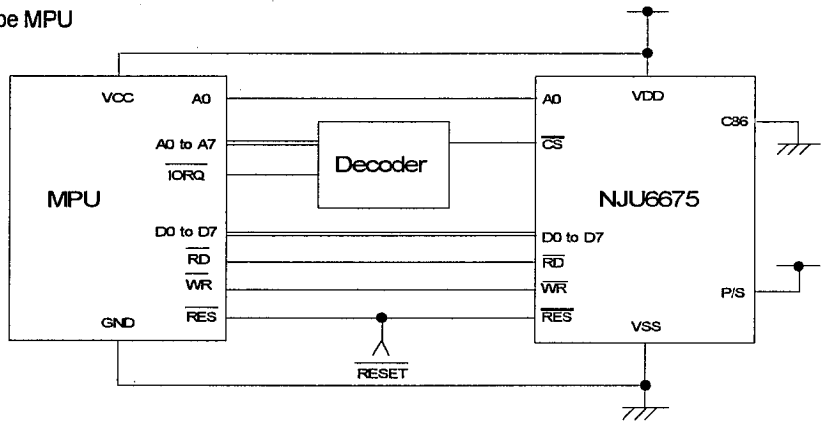
■ APPLICATION CIRCUIT

-Microprocessor Interface Example

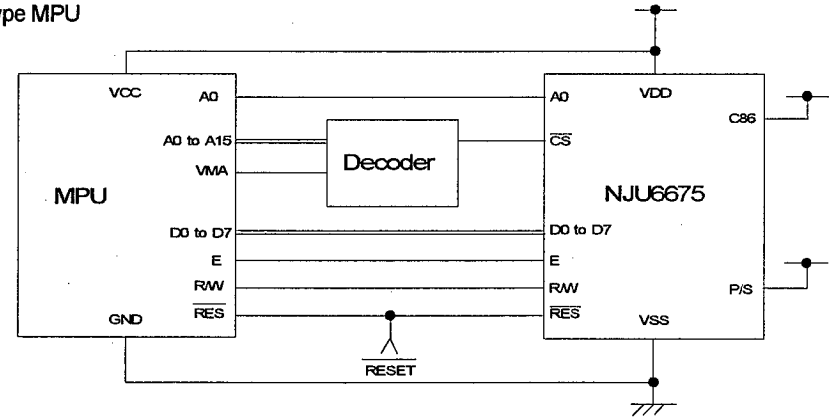
The NJU6675 interfaces to 80 type and 68 type MPU directly.

And the serial interface also communicate with MPU.

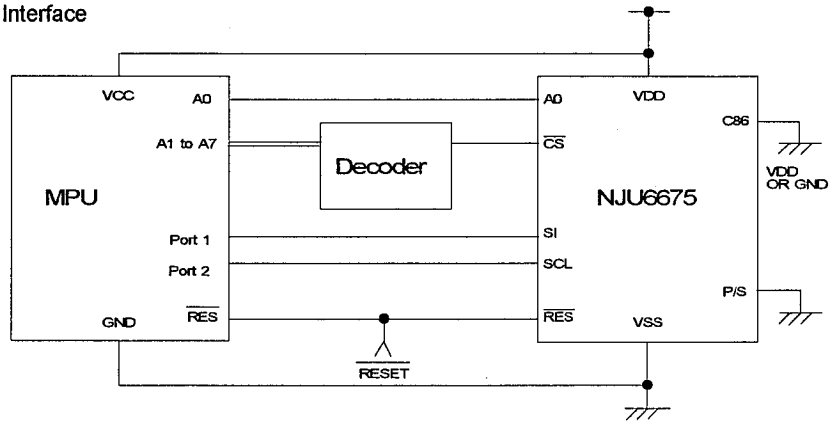
80 Type MPU



68 Type MPU



Serial Interface



MEMO

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