

OVERVIEW

The SM5013 Series crystal oscillator module ICs fabricated in NPC's Molybdenum-gate CMOS. They comprise low-voltage low-current consumption

oscillator circuits and output buffers. They incorporate built-in oscillation capacitance with superior frequency response to realize.

FEATURES

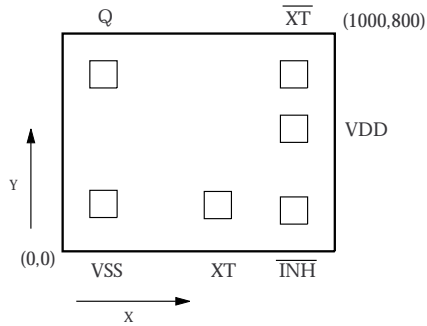
- 4.5 to 5.5 V supply voltage
- Oscillation capacitances built-in (C_G and C_D)
- Output drive capability : 8 mA ($V_{DD} = 4.5V$)
- Output duty level
 - SM5013KDH : CMOS
 - SM5013LDH : TTL
- 3rd overtone oscillation
- Output frequency : f_o (Oscillation frequency)
- Input level : TTL
- 3 state function
- 6 pin SOT (SM5013×DH)
- Chip form (CF5013×D)

ORDERING INFORMATION

Device	Package
SM5013×DH	6pinSOT
CF5013×D	Chip form

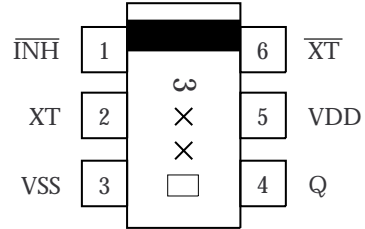
PAD DIMENSIONS

(UNIT : μm)



PIN OUT

(Top View)



PAD COORDINATES

Pad	Coordinate(μm)	
	X	Y
VSS	150	174
XT	570	170
$\overline{\text{INH}}$	850	150
VDD	850	450
$\overline{\text{XT}}$	850	650
Q	150	650

Chip size : $1.00 \times 0.80\text{mm}$
 Chip thickness : $250 \pm 30\mu\text{m}$
 Chip reverse side : V_{DD} level

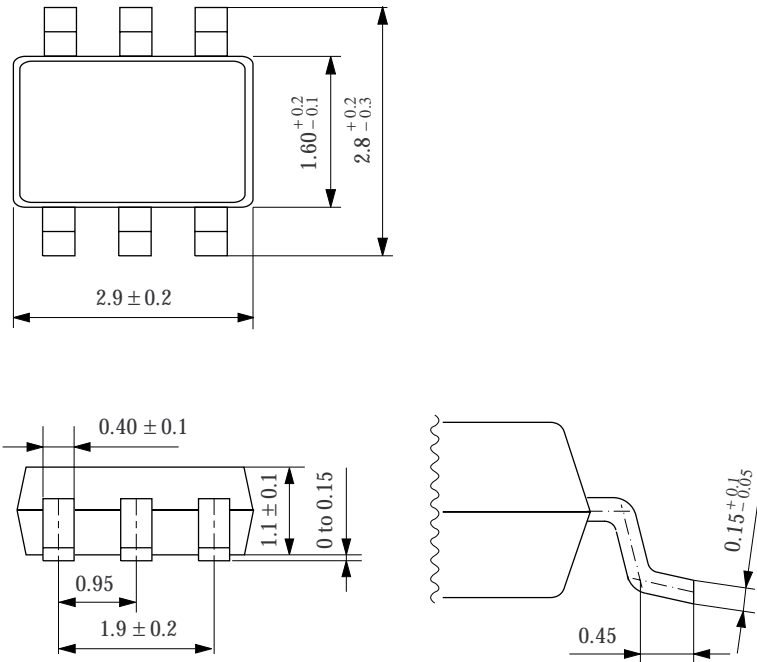
PIN DESCRIPTIONS

PIN	DESCRIPTION
XT	Oscillator input pin
$\overline{\text{XT}}$	Oscillator output pin
$\overline{\text{INH}}$	Output state control input pin (with built-in pull-up resistance
VDD	Supply voltage
VSS	Ground
Q	Output pin (fo : Oscillator frequency)

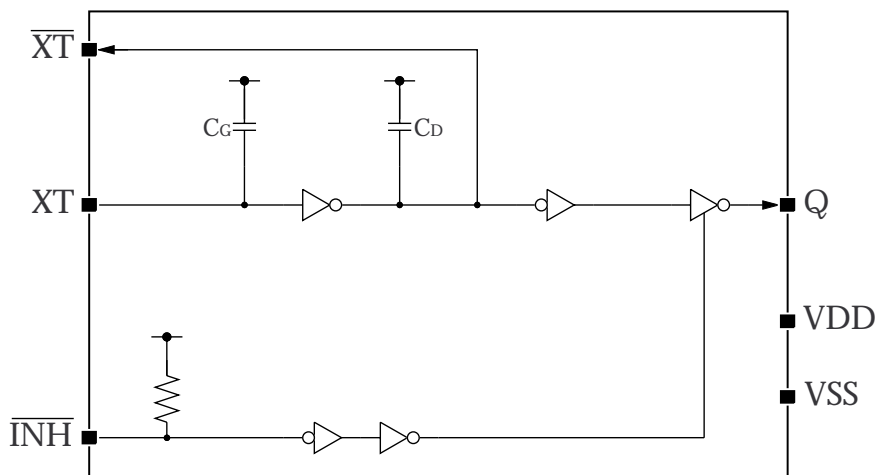
PACKAGE DIMENSIONS

(UNIT : mm)

- 6pin SOT



BLOCK DIAGRAM

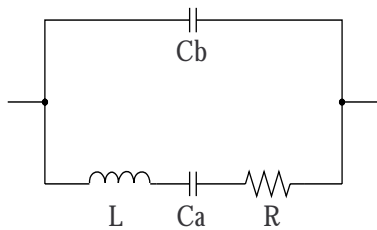


DEVICE LIST

Device	Target frequency range (MHz)	gm (relative value)	Output (stand by)	Internal capacitance	
				C _G (pf)	C _D (pf)
CF5013KD	22 to 70	CMOS	Hi-Z	8	15
CF5013LD	22 to 70	TTL	Hi-Z	8	15

Note that the operating frequency is highly dependent on the frequency of the crystal used.

Current consumption and Output waveform with NPC's standard crystal



f (MHz)	R (Ω)	L (mH)	Ca (fF)	Cb (pF)
30	18.62	16.24	1.733	5.337
40	20.53	11.34	1.396	3.989
50	22.17	7.40	1.370	4.105
60	22.20	5.05	1.388	4.226
70	25.42	4.18	1.254	5.170

SPECIFICATIONS

Absolute Maximum Ratings

$V_{SS} = 0V$, unless otherwise noted.

Parameter	Symbol	Condition	Rating	unit
Supply voltage range	V_{DD}		- 0.5 to + 7.0	V
Input voltage range	V_{IN}		- 0.5 to $V_{DD} + 0.5$	V
Output voltage range	V_{OUT}		- 0.5 to $V_{DD} + 0.5$	V
Operating temperature range	T_{opr}		- 40 to + 85	°C
Standard temperature range	T_{STG}	SOT6	- 55 to + 125	°C
		Chip form	- 65 to + 150	°C
Output current	I_{OUT}		13	mA
Power dissipation	P_W	SOT6	250	mW
Soldering temperature	T_{SLD}	SOT6	255	°C
Soldering time	t_{SLD}	SOT6	10	s

Recommended Operating Conditions

$V_{SS} = 0V$, unless otherwise noted.

Parameter	Symbol	Condition	Limit			unit
			min	typ	max	
Supply Voltage	V_{DD}		4.5	-	5.5	V
Input voltage	V_{IN}		V_{SS}	-	V_{DD}	V
Operating temperature	T_{OPR}		- 20	-	+ 80	°C

Electrical Characteristics

$V_{DD} = 4.5$ to $5.5V$, $V_{SS} = 0V$, $T_a = - 20$ to 80 °C, unless otherwise noted.

Parameter	Symbol	Condition	Limit			unit	
			min	typ	max		
HIGH - level output voltage	V_{OH}	Q pin, test circuit 1, $V_{DD} = 4.5V$, $I_{OH} = 8mA$	3.9	4.2	-	V	
LOW - level output voltage	V_{OL}	Q pin, test circuit 2, $V_{DD} = 4.5V$, $I_{OL} = 8mA$	-	0.3	0.4	V	
Output leakage current	I_Z	Q pin, test circuit 2, $\overline{INH} = Low$, $V_{DD} = 5.5V$	$V_{OH} = V_{DD}$	-	-	10	μA
			$V_{OL} = V_{SS}$	-	-	10	μA
HIGH - level input voltage	V_{IH}	\overline{INH} pin	2.0	-	-	V	
LOW - level input voltage	V_{IL}	\overline{INH} pin	-	-	0.8	V	
Current consumption	I_{DD}	$\overline{INH} = OPEN$, test circuit 3, $C_L = 15pF$, $f = 70MHz$	CF5013KD, load circuit 1	-	28	45	mA
			CF5013LD, load circuit 2	-	28	45	mA
Pull - up resistance	R_{UP}	\overline{INH} pin, test circuit 4	25	100	250	kΩ	
Internal capacitance	C_G	Design value, determined by the internal wafer pattern	7.2	8	8.8	pF	
	C_D		13.5	15	16.5	pF	

Switching Characteristics**CF5013KD (Duty level CMOS)**

$V_{DD} = 4.5$ to $5.5V$, $V_{SS} = 0V$, $T_a = -20$ to $80\text{ }^\circ\text{C}$, unless otherwise noted.

Parameter	Symbol	Condition	Limit			unit
			min	typ	max	
Output rise time	t_r	Test circuit 5, load circuit 1, $C_L = 15\text{pF}$, $0.1V_{DD} \rightarrow 0.9V_{DD}$	–	3.5	7	ns
Output fall time	t_f	Test circuit 5, load circuit 1, $C_L = 15\text{pF}$, $0.9V_{DD} \rightarrow 0.1V_{DD}$	–	3.5	7	ns
Output duty cycle ¹	DUTY	Test circuit 5, $T_a = 25^\circ\text{C}$, $V_{DD} = 5.0V$ load circuit 1, $C_L = 15\text{pF}$, $f = 70\text{MHz}$	45	–	55	%
Output disable delay time	t_{PLZ}	Test circuit 5, $T_a = 25^\circ\text{C}$, $V_{DD} = 5.0V$, load circuit 1, $C_L = 15\text{pF}$	–	–	100	ns
Output enable delay time	t_{PZL}		–	–	100	ns

1. Determined by the lot monitor.

CF5013LD (Duty level TTL)

$V_{DD} = 4.5$ to $5.5V$, $V_{SS} = 0V$, $T_a = -20$ to $80\text{ }^\circ\text{C}$, unless otherwise noted.

Parameter	Symbol	Condition	Limit			unit
			min	typ	max	
Output rise time	t_r	Test circuit 5, load circuit 2, $C_L = 15\text{pF}$, $0.4V \rightarrow 2.4V$	–	2.5	7	ns
Output fall time	t_f	Test circuit 5, load circuit 2, $C_L = 15\text{pF}$, $2.4V \rightarrow 0.4V$	–	2.5	7	ns
Output duty cycle ¹	DUTY	Test circuit 5, $T_a = 25^\circ\text{C}$, $V_{DD} = 5.0V$ load circuit 2, $C_L = 15\text{pF}$, $f = 70\text{MHz}$	45	–	55	%
Output disable delay time	t_{PLZ}	Test circuit 5, $T_a = 25^\circ\text{C}$, $V_{DD} = 5.0V$, load circuit 2, $C_L = 15\text{pF}$	–	–	100	ns
Output enable delay time	t_{PZL}		–	–	100	ns

1. Determined by the lot monitor.

FUNCTIONAL DESCRIPTION**Stand – by Function**

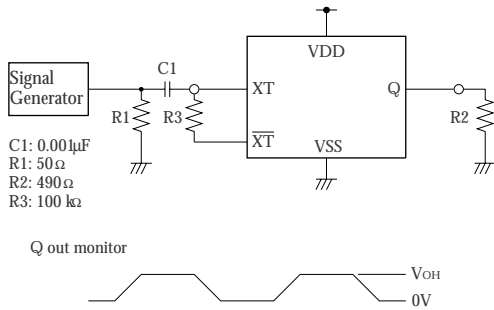
When $\overline{\text{INH}}$ pin is Low-level, Q pin will be high-impedance.

$\overline{\text{INH}}$	Q
High(open)	Output
Low	Hi - Z

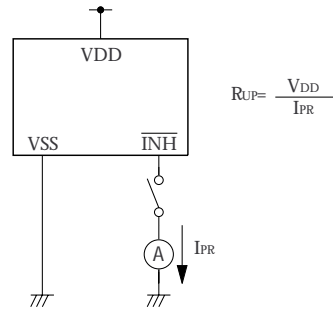
TEST CIRCUITS

Test Circuit 1

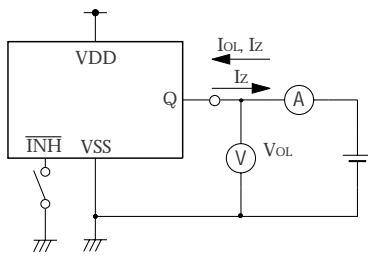
3.5 V_{P-P}, 10MHz sine wave input signal



Test Circuit 4

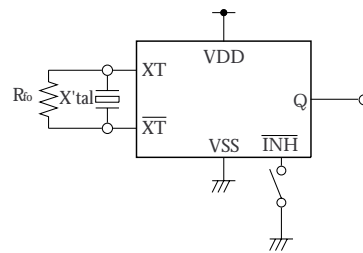


Test Circuit 2



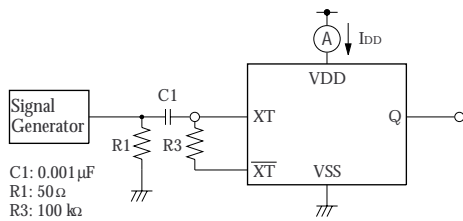
Test Circuit 5

X'tal = 70MHz
Rfo = 2.7kΩ

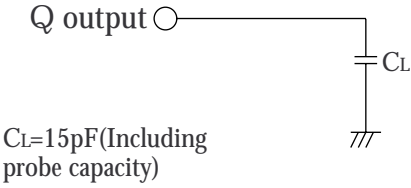


Test Circuit 3

3.5 V_{P-P}, 70MHz sine wave input signal

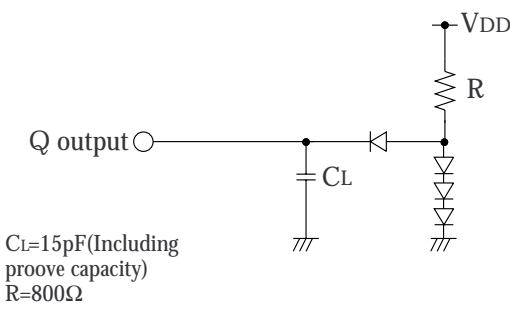


Load Circuit 1



$C_L=15\text{pF}$ (Including probe capacity)

Load Circuit 2

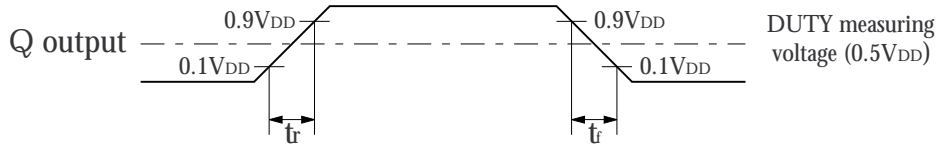


$C_L=15\text{pF}$ (Including probe capacity)
 $R=800\Omega$

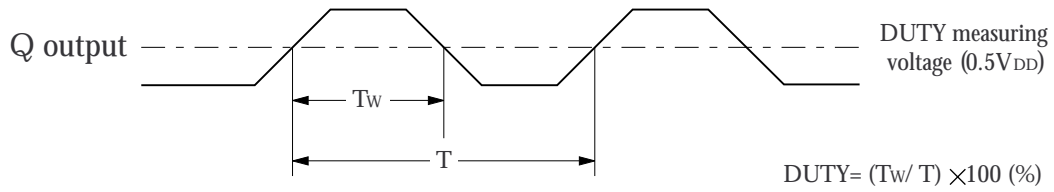
Switching Time Test Waveforms

(1) SM5013KD (Duty level CMOS)

- t_r , t_f , DUTY

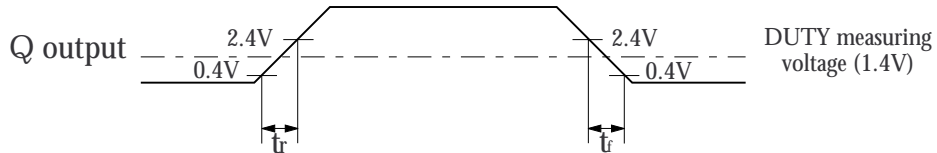


- Output duty cycle time

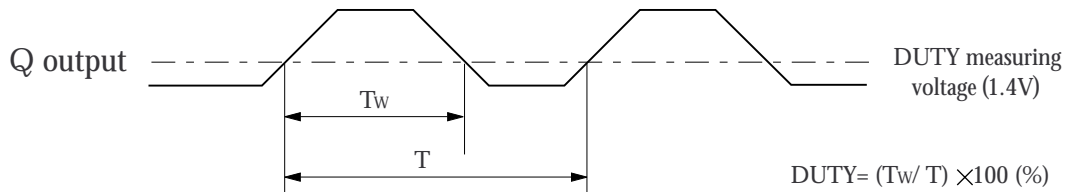


(2) CF5013LD (Duty level TTL)

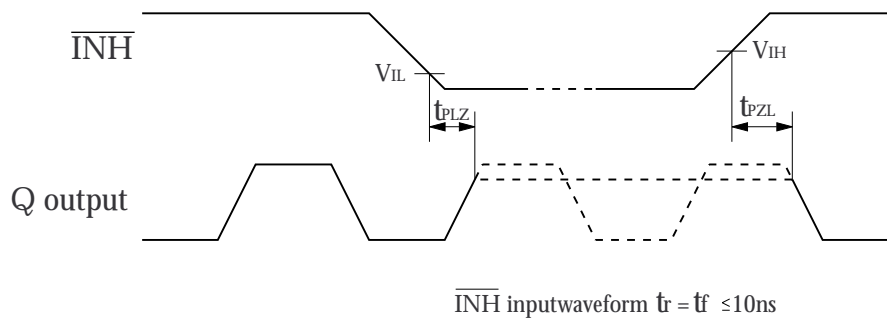
- t_r , t_f , DUTY



- Output duty cycle time



• Output Disable/Enable Delay Times



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