NIPPON PRECISION CIRCUITS INC.

SM8750AV

Data Jitter Measurement IC

OVERVIEW

The SM8750AV is a data jitter measurement CMOS LSI for adaptive control.

FEATURES

- RDCLK and DATA signal phase difference to voltage converter (75mV/ns (typ) coefficient)
- RDCLK duty auto-adjust function (rising edge reference)
- DATA signal delay auto-adjust function (independently adjusted on rising and falling edges)
- Offset auto-calibration function
- 3-wire serial interface mode control
- Sleep function
- Single 5V supply
- 16-pin VSOP

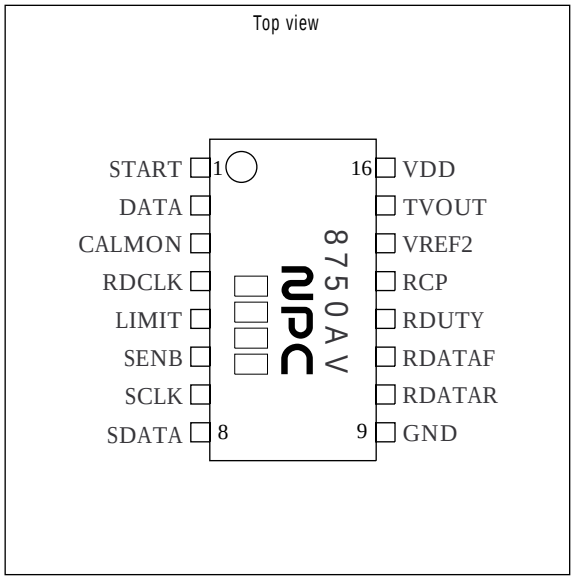
APPLICATIONS

- Optical disc equipment
  - CD-R
  - CD-RW
  - DVD-RAM
  - Others
- Control/governing equipment

ORDERING INFORMATION

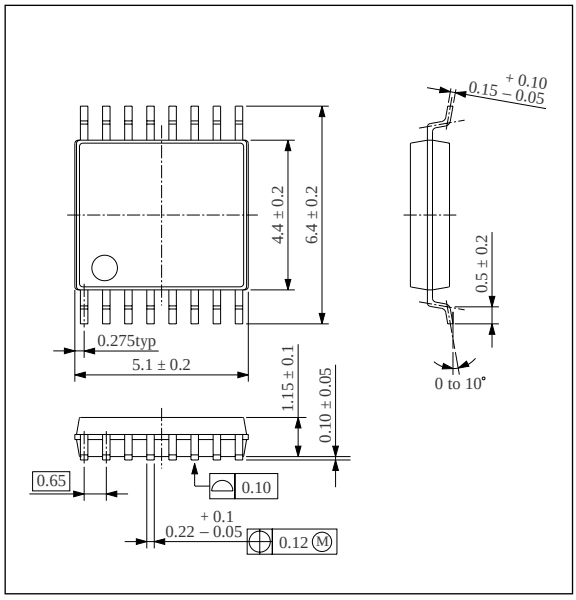
Device	Package
SM8750AV	16-pin VSOP

PINOUT

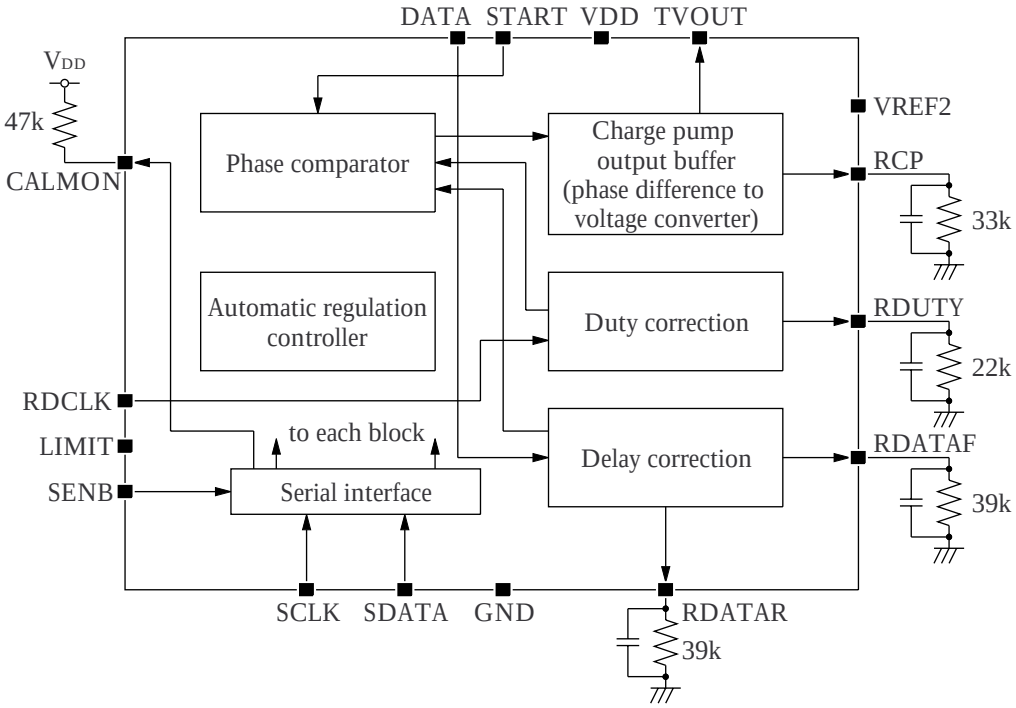


PACKAGE DIMENSIONS

Unit: mm



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Description
1	START	I	Measurement start control. Phase difference to voltage conversion starts on the falling edge.
2	DATA	I	Two-valued signal input
3	CALMON	O	Internal calibration state signal monitor output. N-channel open drain. Active when calibrated.
4	RDCLK	I	PLL clock input
5	LIMIT	I	TVOUT output voltage-limit control voltage input
6	SENB	I	Serial interface: enable signal input
7	SCLK	I	Serial interface: clock signal input
8	SDATA	I/O	Serial interface: data signal input/acknowledge signal output. N-channel open drain.
9	GND	–	Ground
10	RDATAR	O	DATA rising edge: delay adjust circuit reference-current setting resistor connection
11	RDATAF	O	DATA falling edge: delay adjust circuit reference-current setting resistor connection
12	RDUTY	O	RDCLK duty adjust circuit reference-current setting resistor connection
13	RCP	O	Phase difference to voltage converter coefficient reference-current setting resistor connection
14	VREF2	I	2V reference voltage input
15	TVOUT	O	Phase difference to voltage converter output
16	VDD	–	5V supply

SPECIFICATIONS

Absolute Maximum Ratings

GND = 0V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.5 to 7.0	V
Input voltage range	V_{IN}	–0.5 to V_{DD} + 0.5	V
Storage temperature range	T_{stg}	–40 to 125	°C
Power dissipation	P_D	250	mW

Recommended Operating Conditions

GND = 0V

Parameter	Symbol	Rating	Unit
Supply voltage (specifications guaranteed)	V_{DD}	4.75 to 5.25	V
Supply voltage (operation guaranteed)	V_{DD}	4.5 to 5.5	V
Reference voltage input	V_{REF2}	1.89 to 2.11	V
Operating temperature range	T_{opr}	0 to 70	°C

DC Electrical Characteristics

V_{DD} = 5V ± 5%, GND = 0V, T_a = 0 to 70°C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Current consumption[1]	I_{DD1}	Normal operating mode	–	9.0	13.0	mA
	I_{DD2}	Sleep mode	–	0.5	0.7	
HIGH-level logic input voltage[2]	V_{IH}		2.4	–	–	V
LOW-level logic input voltage[2]	V_{IL}		–	–	0.6	V
HIGH-level logic input current[2]	I_{IH}	$V_{IN} = V_{DD}$	–	–	3	µA
LOW-level logic input current[2]	I_{IL}	V_{IN} = GND	–3	–	–	µA
SDATA, CALMON logic output voltage	V_{OL}	I_{OL} = 10mA	–	–	1.0	V
VREF2 input current	I_{REF}	VRFE2 = 2V	–	50	100	µA

1. 39kΩ resistor connected between RDATAR and GND
   39kΩ resistor connected between RDATAF and GND
   22kΩ resistor connected between RDUTY and GND
   33kΩ resistor connected between RCP and GND
   60MHz RDCLK input frequency
   7.5MHz DATA input frequency
   200kHz START input frequency
   0ns DATA and RDCLK phase difference
   Serial interface not operating.
2. Pins START, DATA, RDCLK, SENB, SCLK, SDATA.

Phase Difference to Voltage Converter Characteristics

V_{DD} = 5V ± 5%, GND = 0V, T_a = 0 to 70°C

Parameter	Condition	Rating			Unit
		min	typ	max	
RDCLK input frequency	FCG = LOW	–	58.38	70	MHz
	FCG = HIGH	–	29.19	35	
Phase difference to voltage converter coefficient 1	Normal operation, FCG = LOW	50	75	100	mV/ns
Phase difference to voltage converter coefficient 2	Converter coefficient measurement mode, FCG = LOW	25	37.5	50	mV/ns
	Normal operation, FCG = HIGH	25	37.5	50	
Phase difference to voltage converter coefficient 3	Converter coefficient measurement mode, FCG = HIGH	12.5	18.75	25	mV/ns
Converter coefficient relative accuracy	See note.[1]	–	–	±5	%
Converter coefficient relative accuracy	See note.[2]	–	–	±5	%
Output offset voltage	After VREF2 reference calibration	–	–	±25	mV
Converter voltage settling time	Time from measurement object DATA edge to final set value ± 0.5%	–	–	0.75	µs
Converter voltage reset time	Time from START signal rising edge to final reset value ± 1mV	–	–	3	µs
Output load regulation	I_L = 0.5mA	–	–	20	mV
HIGH-level output voltage range	LIMIT pin voltage reference	+0.15	–	+0.45	V
LOW-level output voltage range		0.8	–	–	V
Output voltage droop		–	–	1	mV/µs
START-DATA setup time[3]	START signal rising edge to DATA signal edge	1T	–	–	ns

1. {[(converter coefficient 2) × 2 / (converter coefficient 1)] – 1} × 100
2. {[(converter coefficient 3) × 2 / (converter coefficient 2)] – 1} × 100
3. T = RDCLK cycle time

Auto-adjust Characteristics

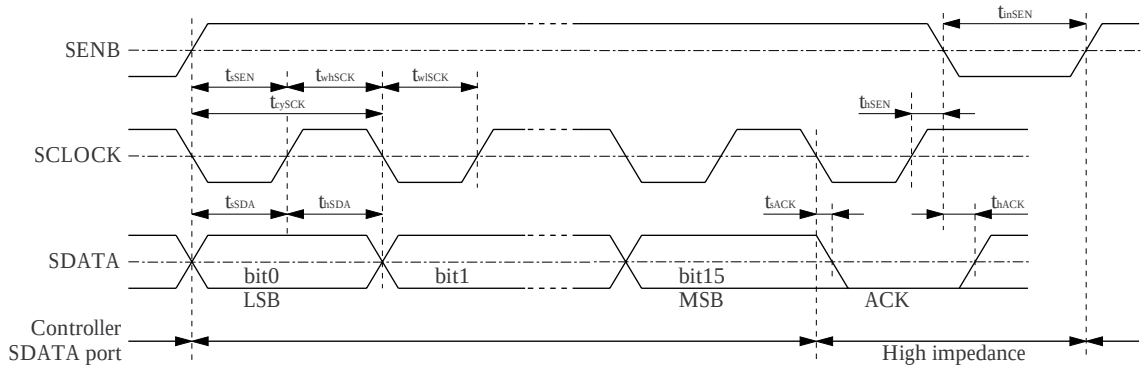
V_{DD} = 5V ± 5%, GND = 0V, T_a = 0 to 70°C

Parameter	Condition	Rating			Unit
		min	typ	max	
Maximum DATA edge delay adjust range		–	29	–	ns
Minimum DATA edge delay adjust range		–	12.5	–	ns
Maximum RDCLK pulsewidth adjust range	FCG = LOW	–	15	–	ns
Minimum RDCLK pulsewidth adjust range		–	3	–	ns
Maximum RDCLK pulsewidth adjust range	FCG = HIGH	–	28	–	ns
Minimum RDCLK pulsewidth adjust range		–	4	–	ns
Auto-adjustment time	After CS = HIGH, until settling	–	5	8	ms
RCP voltage	Converter coefficients set	–	1	–	V
HIGH-level RDATAR/RDATAF voltage	Minimum DATA delay	–	1.92	–	V
LOW-level RDATAR/RDATAF voltage	Maximum DATA delay	–	0.69	–	V
HIGH-level RDUTY voltage	Minimum RDCLK pulsewidth	–	1.88	–	V
LOW-level RDUTY voltage	Maximum RDCLK pulsewidth	–	0.24	–	V

Serial Interface Characteristics

Parameter	Symbol	Rating			Unit
		min	typ	max	
SCLK pulse cycle time	t_{cySCK}	100	–	–	ns
SCLK HIGH-level pulsewidth	t_{whSCK}	40	–	–	ns
SCLK LOW-level pulsewidth	t_{wlSCK}	40	–	–	ns
SENB setup time	t_{sSEN}	20	–	–	ns
SENB hold time	t_{hSEN}	40	–	–	ns
SDATA setup time	t_{sSDA}	15	–	–	ns
SDATA hold time	t_{hSDA}	15	–	–	ns
ACK setup time[1]	t_{sACK}	0	–	20	ns
ACK hold time[1]	t_{hACK}	–	–	50	ns
SENB interval	t_{inSEN}	100	–	–	ns

1. SDATA output signal (ACK) acknowledge output (N-channel open drain), receive data is valid, LOW-level output, 15pF SDATA load capacitance.



FUNCTIONAL DESCRIPTION

Serial Interface

The SM8750AV has a dedicated serial interface port over which data can be written and the various operating modes can be controlled. The port address and bit configuration are shown in table 1, and the data bits are described in table 2.

Table 1. Port address and bit configuration

Bit number															
15 (msb)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (lsb)
Data								Address							
TEST1	TEST0	CSDIS	CS	SP	POLAR	GMES	FCG	×	LOW	HIGH	HIGH	HIGH	HIGH	HIGH	×

×: Don't care.

Table 2. Data bit description

Bit	Description	Default	
TEST[1:0]	Test mode setting	LOW:LOW	(normal operation)
CSDIS	Auto-adjust disable	LOW	(enabled)
CS	Auto-adjust start	LOW	(wait)
SP	Sleep mode settings	LOW	(normal operation)
POLAR	DATA edge settings for phase measurement Polarity setting for converter coefficient measurement	LOW	(falling edge) (1T discharge)
GMES	Converter coefficient measurement mode setting	LOW	(normal operation)
FCG	RDCLK pulsewidth auto-adjust mode Phase difference to voltage converter coefficient switching	LOW	(minimum pulsewidth) (maximum converter coefficient)

Table 3. GMES and POLAR operating modes

GMES	POLAR	Operating mode
LOW	LOW	DATA signal falling edge and RDCLK rising edge phase difference conversion
LOW	HIGH	DATA signal rising edge and RDCLK rising edge phase difference conversion
HIGH	LOW	Output converter voltage for phase difference equivalent to –0.5T
HIGH	HIGH	Output converter voltage for phase difference equivalent to +0.5T

Serial data comprising 16 bits is input with the LSB first. Valid data is read in on the 16th rising edge of the SCLK input. On the next SCLK falling edge, the SDATA N-channel open drain is turned ON and SDATA goes LOW, performing the function of an acknowledge signal.

If 15 or less SCLK rising edge pulses occur during the interval when SENB is HIGH, the data received up to the point when SENB goes LOW is ignored and the internal port data is not updated. If 17 or more SCLK rising edge pulses occur, the received data is latched in the internal port on the 16th rising edge and the acknowledge signal is output on the next falling edge. The acknowledge signal is held constant until SENB goes LOW again.

Phase Difference to Voltage Converter

The phase difference to voltage converter circuit takes the converts the phase difference between the RDCLK rising edge and the DATA signal to a voltage. When START goes LOW, the phase difference between the first active DATA signal edge, where the active edge polarity is determined by the serial interface bit POLAR, and the next RDCLK rising edge is converted to a voltage signal. The converted voltage signal is output on TVOUT while START is LOW, and is reset to the VREF2 reference level when START goes HIGH again.

The START signal must go LOW for a minimum interval of 1 RDCLK cycle before any DATA signal edge to be converted, regardless of the number of DATA signal edges. If the START interval is shorter than 1 cycle, there is a possibility that the next edge might be misinterpreted as the conversion object.

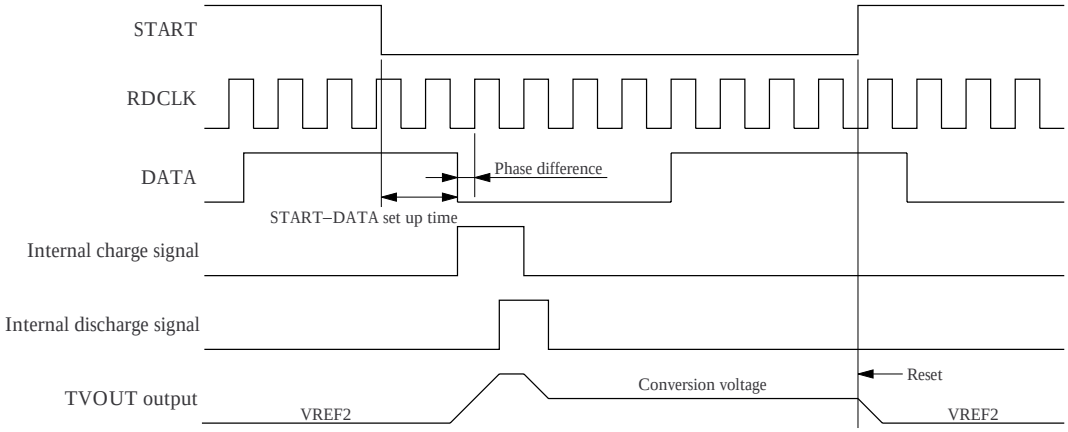


Figure 1. Converter operation timing (POLAR = LOW, DATA leading phase)

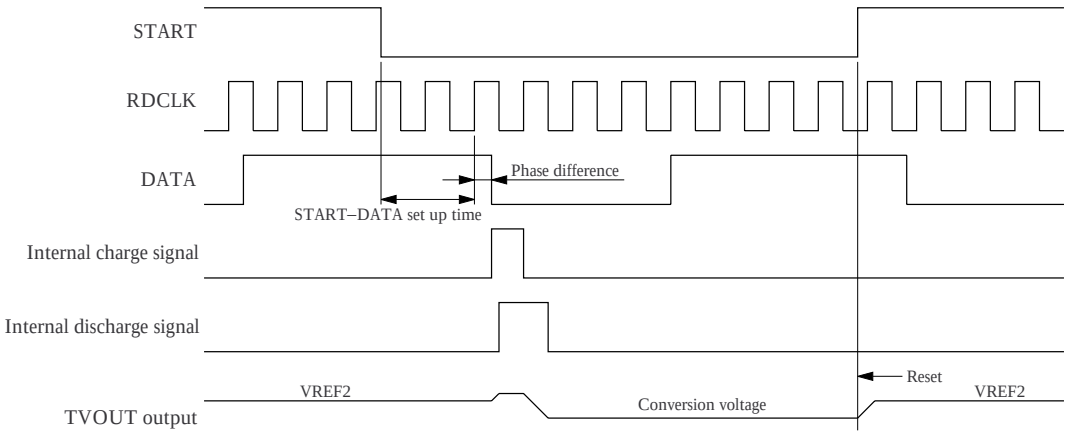


Figure 2. Converter operation timing (POLAR = LOW, DATA lagging phase)

Converter Coefficient Measurement Mode

When the serial interface bit GMES is set HIGH, converter coefficient measurement mode is invoked. In this mode, a voltage equivalent to a phase difference of ±0.5T, determined by the POLAR input bit, is output on TVOUT. Internally, the difference in pulsewidth between the charge/discharge signals is ±1T, where the charge pump circuit capacitance is double the capacitance during normal operation in order to generate outputs equivalent to phase differences of ±0.5T.

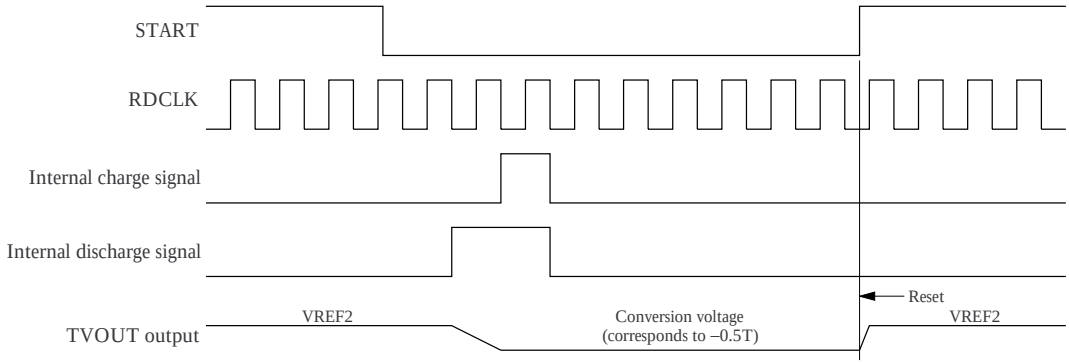


Figure 3. Converter coefficient measurement mode timing (POLAR = LOW)

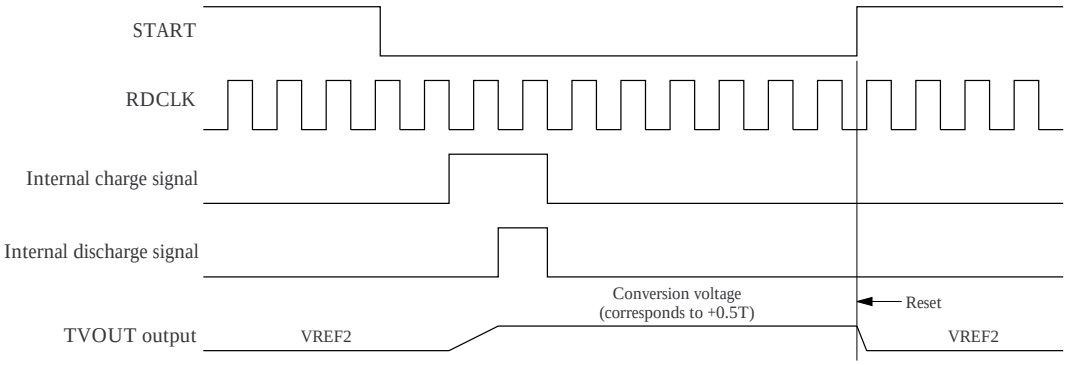


Figure 4. Converter coefficient measurement mode timing (POLAR = HIGH)

Auto-adjust Function

When the serial interface bit CS is set HIGH, the auto-adjust function starts and operates on the objects in the sequence described below. In the auto-adjust sequence cycle, the RDCLK pulsewidth and DATA delay are set to approximately the center of the adjustment range.

1. Charge pump circuit and output buffer offset cancellation
   An identical 0.5T signal is added to the charge/discharge signals and the output on TVOUT is calibrated to an output voltage of VREF2.
2. RDCLK pulsewidth
   Signals equivalent to the RDCLK HIGH-level pulsewidth and LOW-level pulsewidth are added to the internal charge/discharge signals, and the RDCLK pulsewidths are adjusted to recover a TVOUT output voltage of VREF2.
3. DATA rising edge delay
   The phase difference between the RDCLK rising edge and DATA rising edge is converted to a voltage, and the RDCLK rising edge delay is adjusted to recover a TVOUT output voltage of VREF2.
4. DATA falling edge delay
   The phase difference between the RDCLK rising edge and DATA falling edge is converted to a voltage, and the RDCLK rising edge delay is adjusted to recover a TVOUT output voltage of VREF2.

The CALMON calibration monitor output is high impedance during the auto-adjust sequence interval. When auto-adjustment is completed, the CALMON N-channel open drain turns ON and CALMON goes LOW, and the CS bit is cleared to LOW.

When the serial interface bit CSDIS is set HIGH, the auto-adjustment result is disabled, and the external inputs on RDCLK and DATA are input to the phase comparator without adjustment. If CS and CSDIS are both simultaneously set HIGH, the auto-adjust sequence still takes place but that the result is disabled as soon as the sequence is completed.

When power is switched ON, the auto-adjust sequence is enabled, and the adjusted values are approximately in the center of the corresponding adjustment range.

Sleep Mode

When the serial interface bit SP is set HIGH, sleep mode is invoked. In this mode, all circuits other than the power-ON detection circuit and serial interface circuit are shutdown to reduce current consumption.

When operation transfers from sleep mode to normal operating mode, the auto-adjust settings from the most recent auto-adjust cycle are restored.

Power-ON Reset

When power is switched ON, a built-in power-ON reset circuit sets all serial interface bit settings to LOW (factory preset default), and the auto-adjust circuit settings are set to the middle of the corresponding adjustment range.

Test Mode

When the serial interface bit TEST1 or TEST0 is set HIGH, a test mode is invoked. In these modes, the phase comparator input signals and internal charge/discharge signals are output on CALMON and TVOUT.

Table 4. Test modes

TEST1	TEST0	CALMON	TVOUT
LOW	LOW	Normal operation	Normal operation
LOW	HIGH	Internal charge signal	Internal discharge signal
HIGH	LOW	Phase comparator RDCLK signal	Phase comparator DATA signal

NPC
NIPPON PRECISION CIRCUITS INC.

NIPPON PRECISION CIRCUITS INC.

4-3, Fukuzumi 2-chome
Koto-ku, Tokyo 135-8430, Japan
Telephone: 03-3642-6661
Facsimile: 03-3642-6698

NC9916AE 2000.07