

■ OVERVIEW

The SM5617 series are C-MOS ICs for quartz crystal oscillating module. Each IC has a high frequency oscillating circuit and an output buffer with low current consumption.

There are many kinds of type - output level-TTL or CMOS, output driverbility - 10TTL or 10LSTTL. (Refer to the SERIES TABLE).

The SM5617 series also incorporate built-in feed back resistance made of high accuracy Thin Film resistance and built-in capacitor having excellent frequency characteristics, so it enables stable third overtone oscillation without any external parts.

■ FEATURES

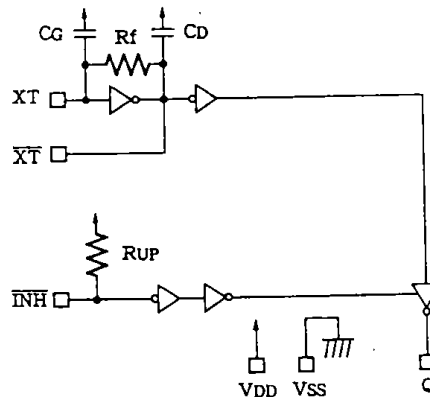
- Available up to 70MHz
- For a third overtone wave use
- Built-in feed back resistance of oscillating circuit
- Built-in capacitor of oscillating circuit
- 3-state function
- TTL compatible I/O interface
- Low current consumption
- Operating voltage
4.0 to 6.0V ($22\text{MHz} \leq f_0 \leq 50\text{MHz}$)
4.5 to 5.5V ($50\text{MHz} < f_0 \leq 70\text{MHz}$)
- Chip form
- Molybdenum gate C-MOS

■ PIN DESCRIPTION

NAME	FUNCTION
XT	Input terminal for oscillating
$\overline{\text{XT}}$	Output terminal for oscillating
$\overline{\text{INH}}$	"L" High impedance On-chip pull-up resistance
V _{DD}	Power supply
V _{SS}	Ground
Q	Output (f ₀)

f₀: Oscillating frequency

■ BLOCK DIAGRAM



■ SERIES TABLE

VERSIONS	Frequency Range (MHz)	Output Duty Level	Output Driverbility
SM5617NA	30 to 42	CMOS	10TTL
NB	33 to 45	CMOS	10TTL
NC	36 to 48	CMOS	10TTL
ND	39 to 52	CMOS	10TTL
NE	48 to 70	CMOS	10TTL
NF	22 to 34	CMOS	10TTL
HA	30 to 42	CMOS	10LSTTL
HB	33 to 45	CMOS	10LSTTL
HC	36 to 48	CMOS	10LSTTL
HD	39 to 52	CMOS	10LSTTL
HE	48 to 60	CMOS	10LSTTL
HF	22 to 34	CMOS	10LSTTL
KA	30 to 42	TTL	10TTL
KB	33 to 45	TTL	10TTL
KC	36 to 48	TTL	10TTL
KD	39 to 52	TTL	10TTL
KE	48 to 70	TTL	10TTL
KF	22 to 34	TTL	10TTL

■ ABSOLUTE MAXIMUM RATING ($V_{SS}=0V$)

ITEM	SYMBOL	CONDITIONS	UNIT
Supply voltage	V_{DD}	-0.5 to +7.0	V
Input voltage	V_{IN}	-0.5 to $V_{DD}+0.5$	V
Output voltage	V_{OUT}	-0.5 to $V_{DD}+0.5$	V
Storage temperature	T_{STG}	-65 to +150	°C

■ RECOMMENDED OPERATIONAL CONDITIONS ($V_{SS}=0V$)

ITEM	CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
Supply voltage	$22MHz \leq f_o \leq 40MHz, C_L \leq 50pF$	V_{DD}	4.0	5.0	6.0	V
	$40MHz \leq f_o \leq 50MHz, C_L \leq 50pF$					
	$40MHz \leq f_o \leq 50MHz, 15pF < C_L \leq 50pF$					
	$50MHz \leq f_o \leq 60MHz, C_L \leq 15pF$					
	$50MHz \leq f_o \leq 70MHz, C_L \leq 15pF$ (H versions)					
	$50MHz \leq f_o \leq 70MHz, C_L \leq 15pF$ (K, N versions)		4.5	5.0	5.5	
Input voltage		V_{IN}	V_{SS}		V_{DD}	V
Operating temperature	$22MHz \leq f_o \leq 50MHz$	T_{OPR}	-20		+80	°C
	$50MHz \leq f_o \leq 60MHz$ (H versions)					
	$50MHz \leq f_o \leq 70MHz$ (K, N versions)					

■ ELECTRICAL CHARACTERISTICS

1. N Versions

(24MHz ≤ f_o ≤ 50MHz, V_{SS}=0V, T_a=-20 to +80°C) or
 (50MHz ≤ f_o ≤ 60MHz, V_{SS}=0V, T_a=-15 to +75°C) unless otherwise noted

ITEM	SYMBOL	CONDITIONS		LIMITS			UNIT	
				MIN	TYP	MAX		
Output voltage ("H" level)	V _{OH}	Q terminal Fig. 1	V _{DD} =4.5V, I _{OH} =16.0mA	3.9	4.2		V	
Output voltage ("L" level)	V _{OL}		V _{DD} =4.0V, I _{OH} =14.4mA	3.4	3.7			
Output voltage ("L" level)	V _{OL}	Q terminal, Fig. 1	V _{DD} =4.5V, I _{OH} =16.0mA		0.3	0.4	μA	
Output leak current	I _Z		V _{OH} =V _{DD}			10		
Output leak current	I _Z	INH=L, V _{DD} =6.0V	V _{OL} =V _{SS}			10	μA	
Input voltage ("H" level)	V _{IH}	INH terminal	V _{DD} =5±0.5V	20			V	
Input voltage ("L" level)	V _{IL}		V _{DD} =5±1.0V	2.2				
Input voltage ("L" level)	V _{IL}		V _{DD} =5±1.0V			0.8		
Current consumption	I _{DD1}	Load Circuit 1 Fig. 2 CL=15pF INH=OPEN	SM5617NA,N,B,NC f=40MHz	V _{DD} = 4.0-6.0V		20	40	mA
			SM5617ND f=50MHz	V _{DD} = 4.0-6.0V		23	45	
			SM5617NE f=70MHz	V _{DD} = 4.5-5.5V		33	50	
			SM5617NE f=30MHz	V _{DD} = 4.0-6.0V		15	35	
	I _{DD2}	Load Circuit 1 Fig. 2 CL=50pF INH=OPEN	SM5617NA,NB,NC f=40MHz	V _{DD} = 4.0-6.0V		30	50	mA
			SM5617ND f=50MHz	V _{DD} = 4.5-5.5V		33	50	
			SM5617NF f=30MHz	V _{DD} = 4.0-6.0V		25	45	
Pull-up resistance	R _{UP}	INH terminal, Fig. 3		50		250	kΩ	
Feed back resistance	R _f	Fig. 4	SM5617NA, NF	4.1	4.5	5.0	kΩ	
			SM5617NB	3.5	3.9	4.3		
			SM5617NC	3.0	3.3	3.6		
			SM5617ND, NE	2.4	2.7	3.0		
Built-in capacitor	C _G	SM5617NA, NB, NC, ND, NF		8.5	12	15.5	pF	
	C _D			12	17	22		
	C _G	SM5617NE		7.0	10	13	pF	
	C _D			7.0	10	13		

SM5617

2. H Versions

(24MHz ≤ fo ≤ 50MHz, V_{SS}=0V, Ta=-20 to +80°C) or
(50MHz ≤ fo ≤ 60MHz, V_{SS}=0V, Ta=-15 to +75°C) unless otherwise noted

ITEM	SYMBOL	CONDITIONS		LIMITS			UNIT	
				MIN	TYP	MAX		
Output voltage ("H" level)	V _{OH}	Q terminal Fig. 1	V _{DD} =4.5V, I _{OH} =4.0mA	3.9	4.2		V	
			V _{DD} =4.0V, I _{OH} =3.6mA	3.4	3.7			
Output voltage ("L" level)	V _{OL}		V _{DD} =4.5V, I _{OH} =4.0mA		0.3	0.5		
			V _{DD} =4.0V, I _{OH} =3.6mA		0.3	0.5		
Output leak current	I _z	Q terminal, Fig. 1	V _{OH} =V _{DD}			10	μA	
		INH=L, V _{DD} =6.0V	V _{OL} =V _{SS}			10		
Input voltage ("H" level)	V _{IH}	INH terminal	V _{DD} =5±0.5V	20			V	
			V _{DD} =5±1.0V	2.2				
Input voltage ("L" level)	V _{IL}		V _{DD} =5±1.0V			0.8		
Current consumption	I _{DD1}	Load Circuit 1 Fig. 2 CL=15pF INH=OPEN	SM5617HA, HB, HC f=40MHz	V _{DD} = 4.0 to 6.0V		18	36	mA
			SM5617HD f=50MHz	V _{DD} = 4.0 to 6.0V		20	40	
			SM5617HE f=70MHz	V _{DD} =4.5 to 5.5V Ta=-15 to +75°C		25	40	
			SM5617HE f=30MHz	V _{DD} = 4.0 to 6.0V		13	33	
Pull-up resistance	R _{UP}	INH terminal, Fig. 3		50		250	kΩ	
Feed back resistance	R _f	Fig. 4	SM5617HA, HF	4.1	4.5	5.0	kΩ	
			SM5617HB	3.5	3.9	4.3		
			SM5617HC	3.0	3.3	3.6		
			SM5617HD, HE	2.4	2.7	3.0		
Built-in capacitor	C _G	SM5617HA, HB, HC, HD, HF		8.5	12	15.5	pF	
	C _D			12	17	22		
	C _G	SM5617HE		7.0	10	13	pF	
	C _D			7.0	10	13		

3. K Versions

(24MHz ≤ fo ≤ 50MHz, V_{SS}=0V, Ta=-20 to +80°C) or
(50MHz ≤ fo ≤ 60MHz, V_{SS}=0V, Ta=-15 to +75°C) unless otherwise noted

ITEM	SYMBOL	CONDITIONS		LIMITS			UNIT	
				MIN	TYP	MAX		
Output voltage ("H" level)	V _{OH}	Q terminal Fig. 1	V _{DD} =4.5V, I _{OH} =16.0mA	3.9	4.2		V	
			V _{DD} =4.0V, I _{OH} =14.4mA	3.4	3.7			
Output voltage ("L" level)	V _{OL}		V _{DD} =4.5V, I _{OH} =16.0mA		0.3	0.4		
			V _{DD} =4.0V, I _{OH} =14.4mA		0.3	0.4		
Output leak current	I _z	Q terminal, Fig. 1	V _{OH} =V _{DD}			10	μA	
		INH=L, V _{DD} =6.0V	V _{OL} =V _{SS}			10		
Input voltage ("H" level)	V _{IH}	INH terminal	V _{DD} =5±0.5V	20			V	
			V _{DD} =5±1.0V	2.2				
Input voltage ("L" level)	V _{IL}		V _{DD} =5±1.0V			0.8		
Current consumption	I _{DD1}	Load Circuit 1 Fig. 2 CL=15pF INH=OPEN	SM5617KA, KB, KC f=40MHz	V _{DD} = 4.0 to 6.0V		20	40	mA
			SM5617KD f=50MHz	V _{DD} = 4.0 to 6.0V		23	45	
			SM5617KE f=70MHz	V _{DD} =4.5 to 5.5V Ta=-15 to +75°C		33	50	
			SM5617KE f=30MHz	V _{DD} = 4.0 to 6.0V		13	35	
Pull-up resistance	R _{UP}	INH terminal, Fig. 3		50		250	kΩ	
Feed back resistance	R _f	Fig. 4	SM5617KA, KF	4.1	4.5	5.0	kΩ	
			SM5617KB	3.5	3.9	4.3		
			SM5617KC	3.0	3.3	3.6		
			SM5617KD, KE	2.4	2.7	3.0		
Built-in capacitor	C _G	SM5617KA, KB, KC, KD, KF		8.5	12	15.5	pF	
	C _D			12	17	22		
	C _G	SM5617KE		7.0	10	13	pF	
	C _D			7.0	10	13		

SWITCHING CHARACTERISTICS

1. N Versions

(24MHz ≤ f ≤ 50MHz, V_{SS}=0V, T_a=-20 to +80°C) or
(50MHz ≤ f ≤ 60MHz, V_{SS}=0V, T_a=-15 to +75°C) unless otherwise noted

ITEM	SYMBOL	CONDITIONS			LIMITS			UNIT
					MIN	TYP	MAX	
Output rise time	T _{r1}	Fig. 2 Load Circuit 1	C _L =15pF	V _{DD} =5 ± 0.5V	2.0	4.0	ns	
				V _{DD} =5 ± 1.0V		4.6		
	T _{r2}	0.1V _{DD} → 0.9V _{DD}	C _L =50pF	V _{DD} =5 ± 0.5V	4.0	8.0		
				V _{DD} =5 ± 1.0V		9.5		
Output fall time	T _{f1}	Fig. 2 Load Circuit 1	C _L =15pF	V _{DD} =5 ± 0.5V	2.0	4.0	ns	
				V _{DD} =5 ± 1.0V		4.6		
	T _{f2}	0.9V _{DD} → 0.1V _{DD}	C _L =50pF	V _{DD} =5 ± 0.5V	4.0	8.0		
				V _{DD} =5 ± 1.0V		9.5		
Duty factor of fundamental output	DUTY	V _{DD} =5.0V T _a =25°C Fig. 2 Load Circuit 1	SM5617NA, NB, NC C _L =50pF f=40MHz	45		55	%	
			SM5617ND C _L =50pF f=50MHz					
			SM5617NE C _L =15pF f=70MHz	40		60		
			SM5617NF C _L =50pF f=30MHz	45		55		
Output disable time	T _{PLZ}	Fig. 2, T _a =25°C, V _{DD} =5±1.0V				100	ns	
	T _{PLZ}	Load C _L ≤ 50pF (SM5617NE: V _{DD} =5±0.5V)				100		
Operating frequency range	f	Fig. 2 Load Circuit 1 *1	SM5617NA	30		42	MHz	
			SM5617NB	33		45		
			SM5617NC	36		48		
			SM5617ND	39		52		
			SM5617NE	48		70		
			SM5617NF	22		34		

2. H Versions

(24MHz ≤ f ≤ 50MHz, V_{SS}=0V, T_a=-20 to +80°C) or
(50MHz ≤ f ≤ 60MHz, V_{SS}=0V, T_a=-15 to +75°C) unless otherwise noted

ITEM	SYMBOL	CONDITIONS			LIMITS			UNIT
					MIN	TYP	MAX	
Output rise time	T _{r1}	Fig. 2 Load Circuit 1	C _L =15pF	V _{DD} =5 ± 0.5V	5.0	8.0	ns	
				V _{DD} =5 ± 1.0V		10.0		
	T _{r2}	0.1V _{DD} → 0.9V _{DD}	C _L =50pF	V _{DD} =5 ± 0.5V	13.0	21.0		
				V _{DD} =5 ± 1.0V		26.0		
Output fall time	T _{f1}	Fig. 2 Load Circuit 1	C _L =15pF	V _{DD} =5 ± 0.5V	5.0	8.0	ns	
				V _{DD} =5 ± 1.0V		10.0		
	T _{f2}	0.1V _{DD} → 0.9V _{DD}	C _L =50pF	V _{DD} =5 ± 0.5V	13.0	21.0		
				V _{DD} =5 ± 1.0V		26.0		
Duty factor of fundamental output	DUTY	V _{DD} =5.0V T _a =25°C Fig. 2 Load Circuit 1	SM5617HA, HB, HC C _L =50pF f=40MHz	45		55	%	
			SM5617HD C _L =50pF f=50MHz	45		55		
			SM5617HE C _L =15pF f=60MHz	40		60		
			SM5617HF C _L =50pF f=30MHz	45		55		
Output disable time	T _{PLZ}	Fig. 2, T _a =25°C, V _{DD} =5±1.0V				100	ns	
	T _{PLZ}	Load C _L ≤ 50pF (SM5617HE: V _{DD} =5±0.5V)				100		
Operating frequency range	f	Fig. 2 Load Circuit 1 *1	SM5617HA	30		42	MHz	
			SM5617HB	33		45		
			SM5617HC	36		48		
			SM5617HD	39		52		
			SM5617HE	48		60		
			SM5617HF	22		34		

*1: Recommended operating conditions will change in accordance with operating frequency.
(See Recommended Operating Conditions.)

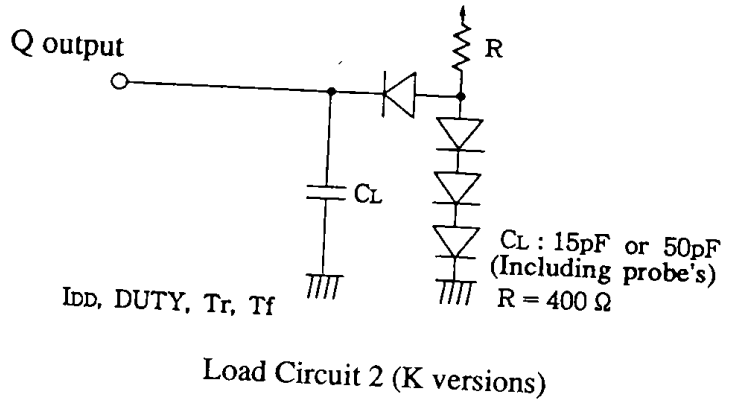
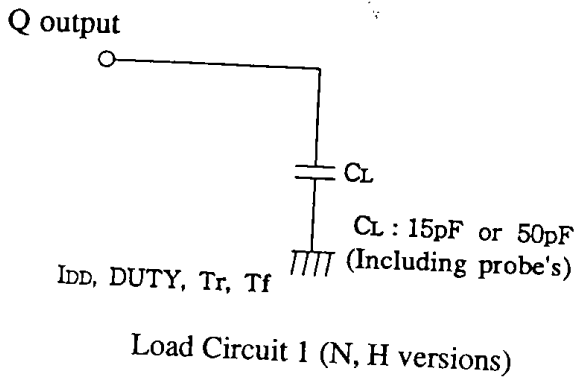
3. K Versions

($24\text{MHz} \leq f_o \leq 50\text{MHz}$, $V_{SS}=0\text{V}$, $T_a=-20$ to $+80^\circ\text{C}$) or
 ($50\text{MHz} \leq f_o \leq 60\text{MHz}$, $V_{SS}=0\text{V}$, $T_a=-15$ to $+75^\circ\text{C}$) unless otherwise noted

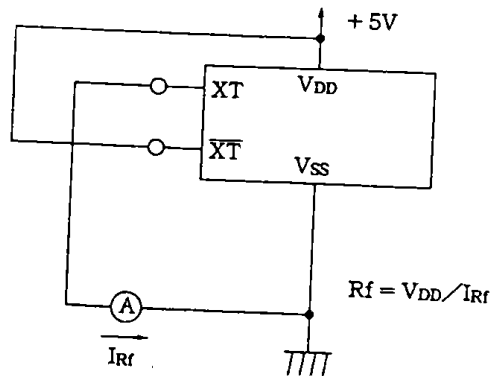
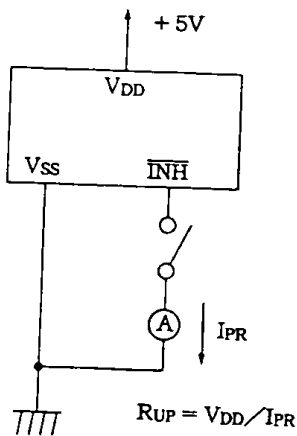
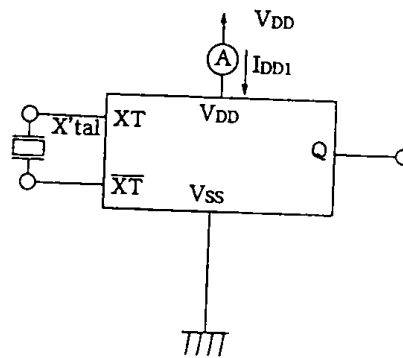
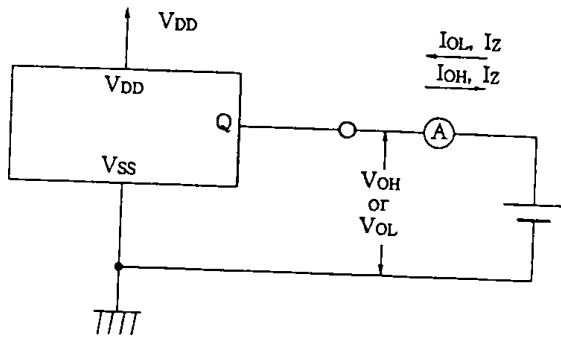
ITEM	SYMBOL	CONDITIONS		LIMITS			UNIT
				MIN	TYP	MAX	
Output rise time	T_{r1}	Fig. 2 Load Circuit 2	$C_L=15\text{pF}$	$V_{DD}=5 \pm 0.5\text{V}$	1.5	3.0	ns
				$V_{DD}=5 \pm 1.0\text{V}$		3.5	
	T_{r2}	$0.4V_{DD} \rightarrow$ $2.4V_{DD}$	$C_L=50\text{pF}$	$V_{DD}=5 \pm 0.5\text{V}$	3.0	6.0	
				$V_{DD}=5 \pm 1.0\text{V}$		7.0	
Output fall time	T_{f1}	Fig. 2 Load Circuit 2	$C_L=15\text{pF}$	$V_{DD}=5 \pm 0.5\text{V}$	1.5	3.0	ns
				$V_{DD}=5 \pm 1.0\text{V}$		3.5	
	T_{f2}	$2.4V_{DD} \rightarrow$ $0.4V_{DD}$	$C_L=50\text{pF}$	$V_{DD}=5 \pm 0.5\text{V}$	3.0	6.0	
				$V_{DD}=5 \pm 1.0\text{V}$		7.0	
Duty factor of fundamental output	DUTY	$V_{DD}=5.0\text{V}$ $T_a=25^\circ\text{C}$ Fig. 2 Load Circuit 2	SM5617KA, KB, KC	45	55	%	
			$C_L=50\text{pF}$ $f=40\text{MHz}$	45	55		
			SM5617KD	40	60		
			$C_L=15\text{pF}$ $f=60\text{MHz}$	45	55		
			SM5617KF				
Output disable time	T_{PLZ}	Fig. 2, $T_a=25^\circ\text{C}$, $V_{DD}=5 \pm 1.0\text{V}$ Load $C_L \leq 50\text{pF}$ (SM5617KE: $V_{DD}=5 \pm 0.5\text{V}$)			100	ns	
	T_{PLZ}				100		
Operating frequency range	f	Fig. 2 Load Circuit 1 *1	SM5617KA	30	42	MHz	
			SM5617KB	33	45		
			SM5617KC	36	48		
			SM5617KD	39	52		
			SM5617KE	48	70		
			SM5617KF	22	34		

*1: Recommended operating conditions will change in accordance with operating frequency.
 (See Recommended Operating Conditions.)

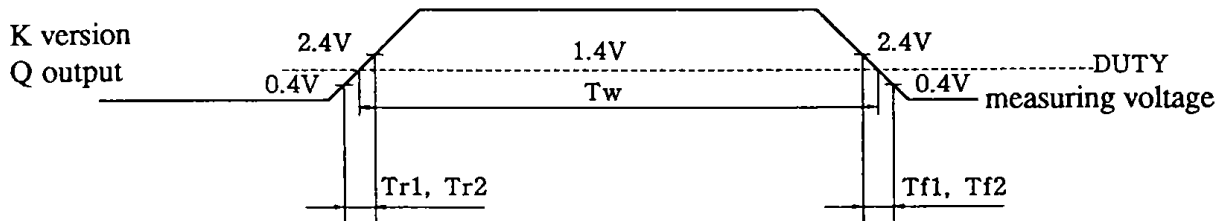
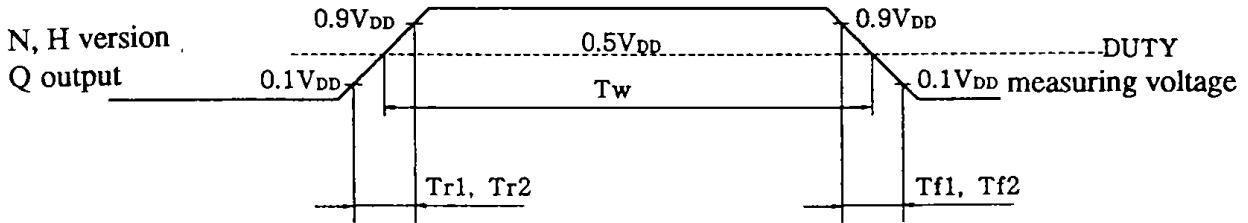
LOAD CIRCUIT



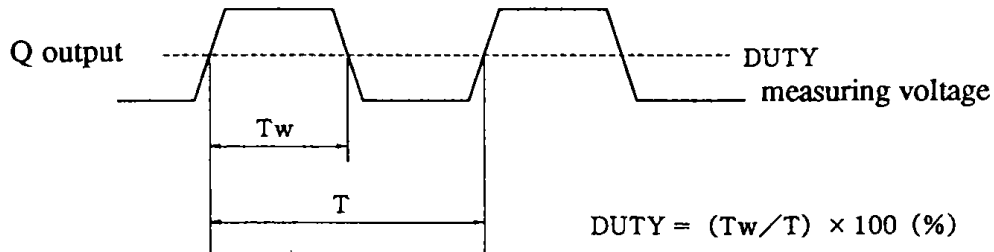
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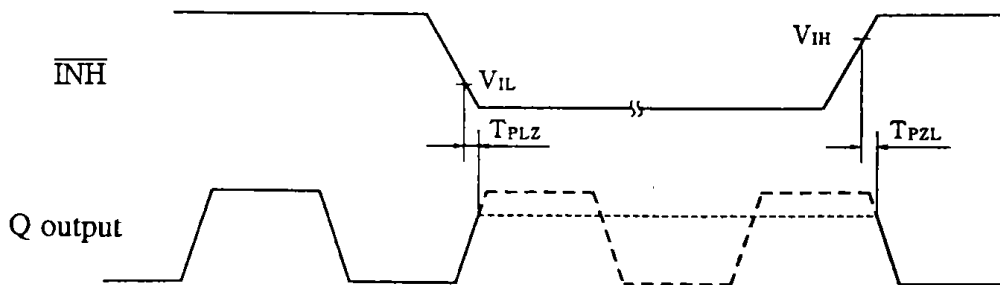
■ WAVEFORMS FOR SWITCHING TIME



■ DUTY FACTOR



■ OUTPUT DISABLE TIME

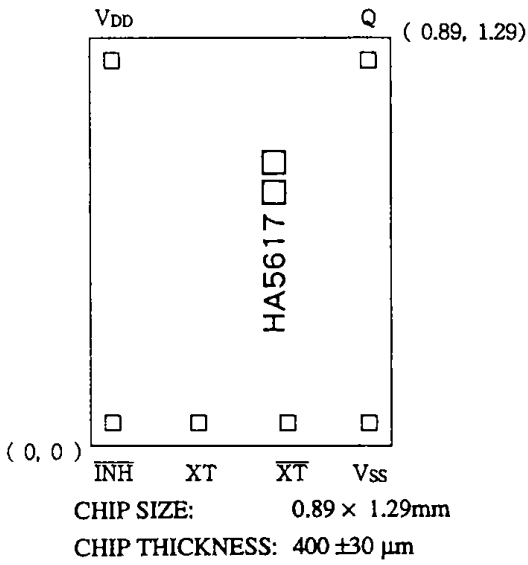


■ FUNCTION

VERSIONS	Output frequency
INH	Q
H (OPEN)	Output (fo)
L	High impedance

fo : Oscillating frequency

■ PAD LOCATION (Unit: mm)



■ PAD COORDINATES

UNIT: μm

NAME	X	Y
INH	145	140
XT	345	140
XT	545	140
VSS	745	140
Q	745	1150
VDD	145	1155