■ OVERVIEW

The SM5619 series is a range of quartz crystal oscillator ICs fabricated using NPC's original molybdenum-gate CMOS technology. Each IC consists of a low-current oscillator circuit and output buffer. With master slice, the output level can be selected between TTL and CMOS, and the output current between 16 mA and 4 mA. The IC also incorporates a high-precision, thin-film feedback resistor and oscillation capacitors having excellent frequency characteristics.

■ FEATURES

- Up to 30 MHz
- Fundamental wave
- Built-in feedback resistor in inverter amplifier
- Built-in loading capacitors CG and CD
- Output tristate function
- Low quartz current
- Chip form
- Input TTL compatible
- Operating voltage 4.5 to 5.5 V
- Low current consumption
- Chip form
- Molybdenum-gate® CMOS construction

■ PIN DESCRIPTION

Name	Function
XT	Oscillation input
$\overline{XT}$	Oscillation output
$\overline{INH}$	"L": output high impedance. Internal pull-up resistor.
V_{DD}	Supply voltage
Vss	Ground
Q	Output (One of fo, fo/2, fo/4 and fo/8 is output according to internal wiring.)

■ SERIES LINEUP

Version	Output frequency	Output duty level	Output current (mA)
SM5619 N1	fo	CMOS	16
N3	fo/2	CMOS	16
N5	fo/4	CMOS	16
N7	fo/8	CMOS	16
H1	fo	CMOS	4
H3	fo/2	CMOS	4
H5	fo/4	CMOS	4
H7	fo/8	CMOS	4
K1	fo	TTL	16

■ FUNCTIONAL DESCRIPTION

Control pin	Output pin
$\overline{INH}$	Q
H (open)	One of fo, fo/2, fo/4 and fo/8
L	High impedance

fo: fundamental frequency

■ ABSOLUTE MAXIMUM RATINGS

(Vss = 0V)

Item	Symbol	Rating		Unit
Supply voltage	V_{DD}	-0.5 to +7.0		V
Input voltage	V_{IN}	-0.5 to V_{DD} +0.5		V
Output voltage	V_{OUT}	-0.5 to V_{DD} +0.5		V
Storage temperature	T_{STG}	-65 to +150		°C
Output current	I_{OUT}	H series	10	mA
		N series	25	
		K1 servion		

■ RECOMMENDED OPERATING CONDITIONS

(Vss = 0V)

Item	Symbol	MIN	TYP	MAX	Unit
Supply voltage	V_{DD}	4.5	5.0	5.5	V
Input voltage	V_{IN}	Vss		V_{DD}	V
Operating temperature	T_{OPR}	-20		+80	°C

■ ELECTRICAL CHARACTERISTICS

1. N series, K1 version

(V_{DD} = 5 ± 0.5 V, V_{SS} = 0 V and Ta= -20 to +80°C unless otherwise specified)

ITEM	SYMBOL	CONDITIONS			LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
H-level output voltage	V_{OH}	Q pin, Fig. 1	V_{DD}=4.5V. I_{OH}=16.0mA		3.9	4.2		V
L-level output voltage	V_{OL}		V_{DD}=4.5V. I_{OL}=16.0mA			0.3	0.4	
Output leak current	I_Z	Q pin, Fig. 1, $\overline{INH}$ pin="L", V_{DD}=5.5V		V_{OH}=V_{DD}			10	µA
				V_{OL}=V_{SS}			10	
H-level input voltage	V_{IH}	$\overline{INH}$ pin			2.0			V
L-level input voltage	V_{IL}						0.8	
Current consumption	I_{DD1}	Load circuit 1, Fig. 2, C_L=15pF, $\overline{INH}$=OPEN, f=30MHz	SM5619N1	C_L=15pF		13	23	mA
				C_L=50pF		18	32	
			SM5619N3	C_L=15pF		9	16	
				C_L=50pF		12	21	
			SM5619N5	C_L=15pF		7	13	
				C_L=50pF		9	16	
			SM5619N7	C_L=15pF		6	11	
				C_L=50pF		7	13	
			SM5619K1	C_L=15pF		13	23	
Pull-up resistor	R_{UP}	$\overline{INH}$ pin, Fig. 3			50		250	kΩ
Feedback resistor	R_f	Fig. 4			90	100	110	kΩ
Inverter amplifier output resistor	R_D	Calculated from Rf			740	820	900	Ω
Internal capacitor	C_G				18.9	21	23.1	pF
	C_D				18.9	21	23.1	

2. H series

(V_{DD} = 5 ± 0.5 V, V_{SS} = 0 V and Ta= -20 to +80°C unless otherwise specified)

ITEM	SYMBOL	CONDITIONS			LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
H-level output voltage	V_{OH}	Q pin, Fig. 1	V_{DD}=4.5V. I_{OH}=4.0mA		3.9	4.2		V
L-level output voltage	V_{OL}		V_{DD}=4.5V. I_{OL}=4.0mA			0.3	0.5	
Output leak current	I_Z	Q pin, Fig. 1, $\overline{INH}$ pin="L", V_{DD}=5.5V		V_{OH}=V_{DD}			10	µA
				V_{OL}=V_{SS}			10	
H-level input voltage	V_{IH}	$\overline{INH}$ pin			2.0			V
L-level input voltage	V_{IL}						0.8	
Current consumption	I_{DD1}	Load circuit 1, Fig. 2, C_L=15pF, $\overline{INH}$=OPEN, f=30MHz	SM5619H1			11	20	mA
			SM5619H3			8	14	
			SM5619H5			6	11	
			SM5619H7			5	9	
Pull-up resistor	R_{UP}	$\overline{INH}$ pin, Fig. 3			50		250	kΩ
Feedback resistor	R_f	Fig. 4			90	100	110	kΩ
Inverter amplifier output resistor	R_D	Calculated from Rf			740	820	900	Ω
Internal capacitor	C_G				18.9	21	23.1	pF
	C_D				18.9	21	23.1	

■ SWITCHING CHARACTERISTICS

1. N series

(V_{DD} = 5 ± 0.5 V, V_{SS} = 0 V and Ta= -20 to +80°C unless otherwise specified)

ITEM	SYMBOL	CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Output rise time	T_r	Load circuit 1, Fig. 2 0.1V_{DD} to 0.9V_{DD}	C_L=15pF		2.0	4.0	ns
			C_L=50pF		4.0	8.0	
Output fall time	T_f	Load circuit 1, Fig. 2 0.9V_{DD} to 0.1V_{DD}	C_L=15pF		2.0	4.0	ns
			C_L=50pF		4.0	8.0	
Output duty cycle	DUTY	Load circuit 1, Fig. 2, V_{DD}=5.0V, Ta=25°C, C_L≤50pF		45		55	%
Output disable delay time	T_{PLZ}	Fig. 2, V_{DD}=5.0V, Ta=25°C, Load C_L≤50pF				100	ns
Output enable delay time	T_{PZL}					100	
Maximum operating frequency	f_{MAX}	Load circuit 1, Fig. 2, C_L=50pF, Checked with lot monitor		30			MHz

2. H series

(V_{DD} = 5 ± 0.5 V, V_{SS} = 0 V and Ta= -20 to +80°C unless otherwise specified)

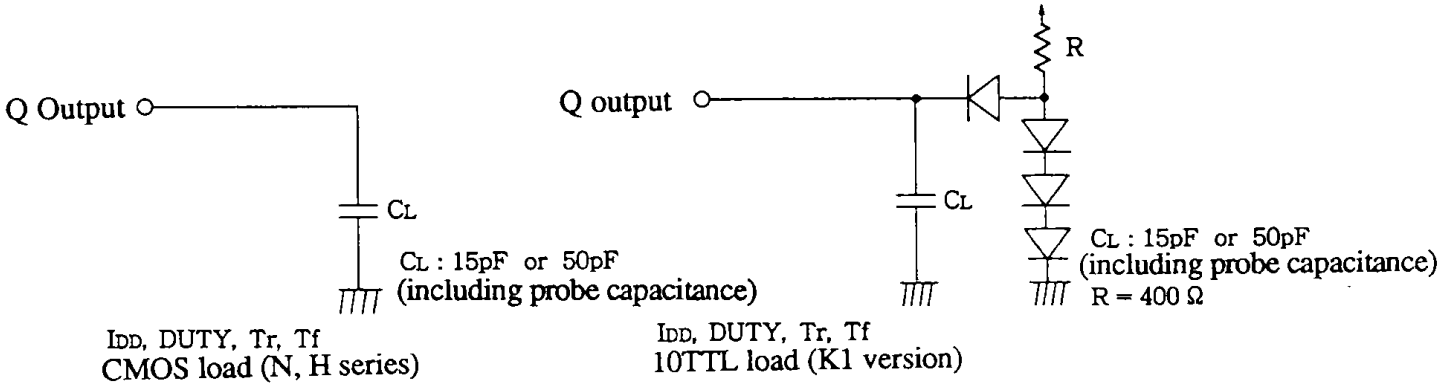
ITEM	SYMBOL	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Output rise time	T_r	Load circuit 1, Fig. 2 0.1V_{DD} to 0.9V_{DD}, C_L=15pF		5.0	10	ns
Output fall time	T_f	Load circuit 1, Fig. 2 0.9V_{DD} to 0.1V_{DD}, C_L=15pF		5.0	10	ns
Output duty cycle	DUTY	Load circuit 1, Fig. 2, V_{DD}=5.0V, Ta=25°C, f=30MHz, C_L=50pF	45		55	%
Output disable delay time	T_{PLZ}	Fig. 2, V_{DD}=5.0V, Ta=25°C, Load C_L≤15pF			100	ns
Output enable delay time	T_{PZL}				100	
Maximum operating frequency	f_{MAX}	Load circuit 1, Fig. 2, C_L=15pF, Checked with lot monitor	30			MHz

3. K1 version

(V_{DD} = 5 ± 0.5 V, V_{SS} = 0 V and Ta= -20 to +80°C unless otherwise specified)

ITEM	SYMBOL	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Output rise time	T_r	Load circuit 2, Fig. 2 0.4V to 2.4V. C_L=15pF		2.0	4.0	ns
Output fall time	T_f	Load circuit 2, Fig. 2 2.4V to 0.4V. C_L=15pF		2.0	4.0	ns
Output duty cycle	DUTY	Load circuit 2, Fig. 2, V_{DD}=5.0V, Ta=25°C, f=30MHz, C_L=15pF	45		55	%
Output disable delay time	T_{PLZ}	Fig. 2, V_{DD}=5.0V, Ta=25°C, Load C_L≤15pF			100	ns
Output enable delay time	T_{PZL}				100	
Maximum operating frequency	f_{MAX}	Load circuit 2, Fig. 2, C_L=15pF, Checked with lot monitor	30			MHz

■ LOAD CIRCUIT



Load circuit 1 Load circuit 2

■ MEASURING CIRCUIT

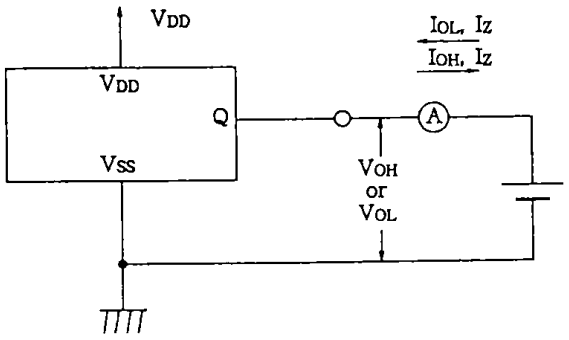


Figure 1

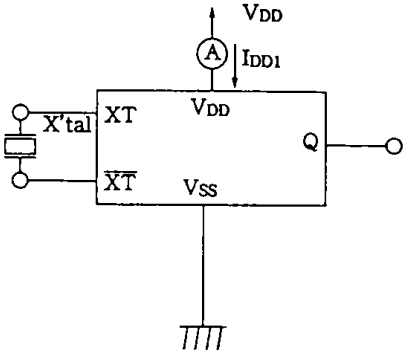


Figure 2

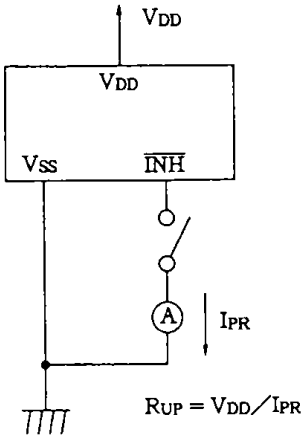


Figure 3

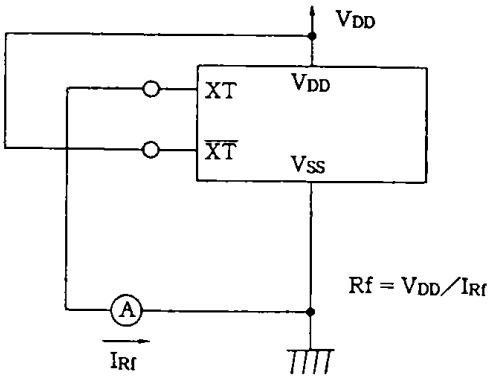
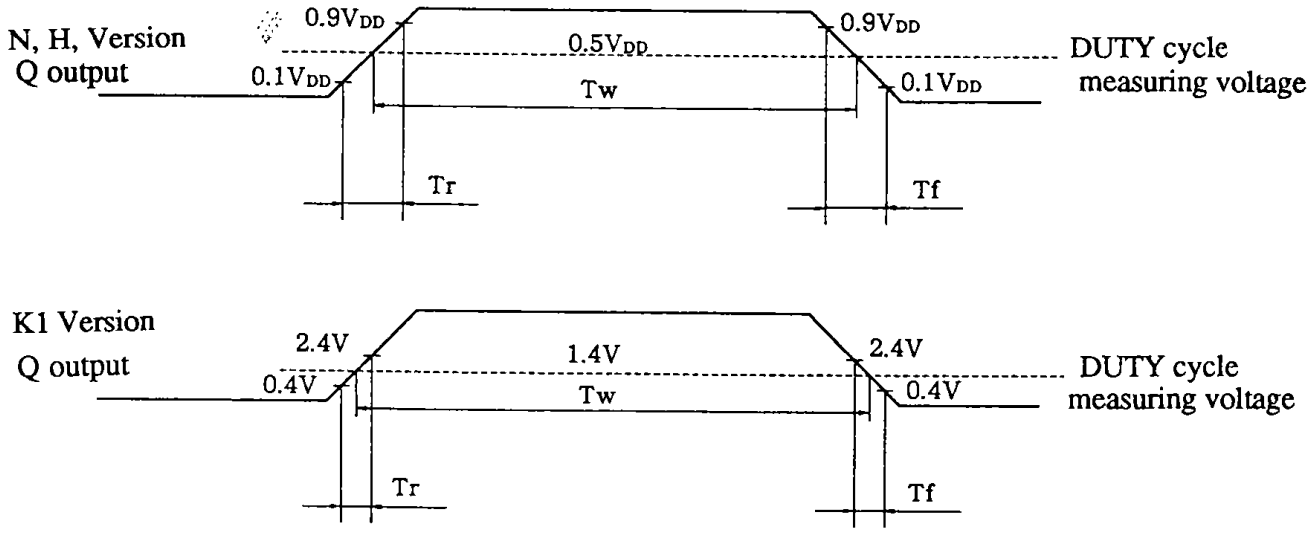
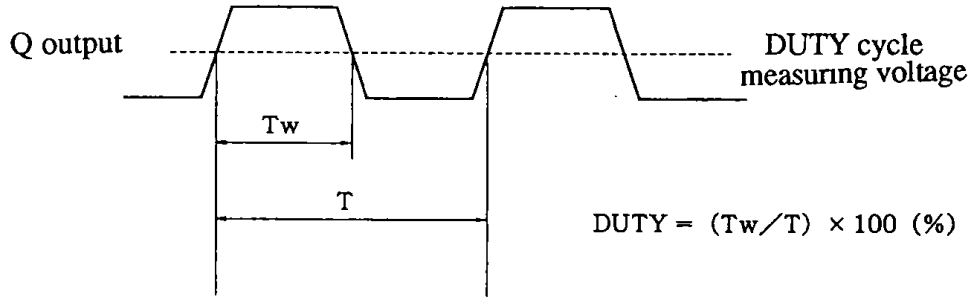


Figure 4

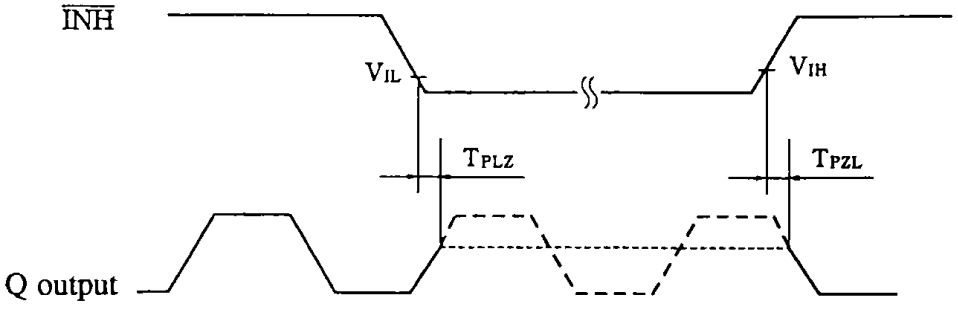
■ SWITCHING TIME WAVEFORM



■ OUTPUT DUTY CYCLE TIME

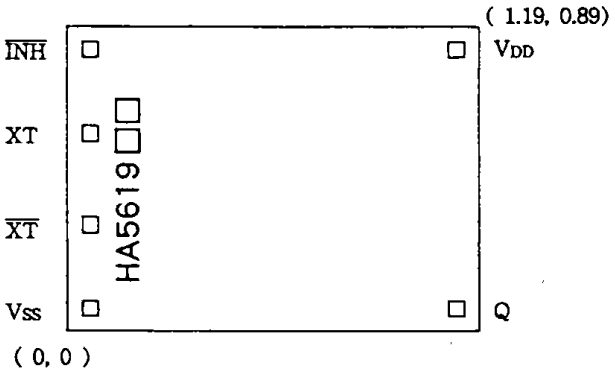


■ OUTPUT DISABLE DELAY TIME, OUTPUT ENABLE DELAY TIME V_{IL}



Q output, $\overline{INH}$ input waveform Tr = Tf 10 ns or less

■ PAD LAYOUT



Chip size: 1.19 × 0.89mm
Chip thickness: 400±30 µm

* □□ version name

■ PAD COORDINATES (Unit: µm)

Pin name	X	Y
$\overline{INH}$	183.5	707.5
XT	183.5	517.5
$\overline{XT}$	183.5	327.5
Vss	183.5	137.5
Q	1042.5	141.5
VDD	1042.5	742.5

Step number	S5	S4	S3	S2	S1	S0
63	HIGH	HIGH	HIGH	HIGH	LOW	LOW
⋮	⋮	⋮	⋮	⋮	⋮	⋮
36	HIGH	LOW	LOW	LOW	LOW	HIGH
35	HIGH	LOW	LOW	LOW	LOW	LOW
34	LOW	HIGH	HIGH	HIGH	HIGH	HIGH
⋮	⋮	⋮	⋮	⋮	⋮	⋮
5	LOW	LOW	LOW	LOW	HIGH	LOW
4	LOW	LOW	LOW	LOW	LOW	HIGH
3	LOW	LOW	LOW	LOW	LOW	LOW

Note
Pins S0 to S5 have internal pull-up resistances. Therefore, only LOW-level pins need be tied to ground. However, it is recommended that HIGH-level inputs be tied to VDD for applications using fixed-length shifting.

Input/Output Control

Inputs				Shift register (internal)	Outputs
RSTN	ENRC	CLK	OE		OUT0 to OUT7
×	×	×	LOW		High impedance
×	×	×	HIGH		Enable
HIGH	HIGH	LOW-to-HIGH	×	Rotate shift	
HIGH	LOW	LOW-to-HIGH	×	Non-rotate shift	
LOW	×	×	×	Reset	

Note
× = don't care