

**OVERVIEW**

The SM6102 is a high-speed, 8-bit A/D converter fabricated in Molybdenum-gate CMOS. It uses a 2-step flash conversion method and features low current consumption.

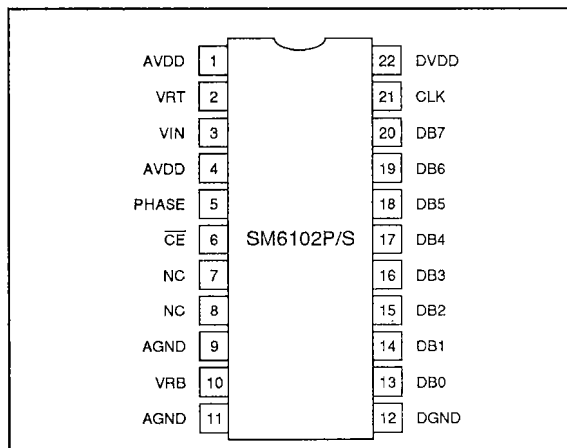
**FEATURES**

- 8-bit resolution
- 8 MSPS maximum conversion rate
- 1.5 LSB non-linearity error (when  $V_{RT} - V_{RB} = 2.0\text{ V}$ )
- 1.0 LSB non-linearity error (when  $V_{RT} - V_{RB} = 5.0\text{ V}$ )
- Low current consumption
- Monotonic with guaranteed no code omission
- External sample-and-hold circuit not required
- Built-in output latch
- Output tristate control pin
- Single 5 V supply
- 22-pin plastic DIP (SM6102P) and 22-pin plastic SOP (SM6102S)
- Molybdenum-gate CMOS process

**APPLICATIONS**

- High-speed facsimile machines
- Data acquisition systems
- High-speed, low-current applications

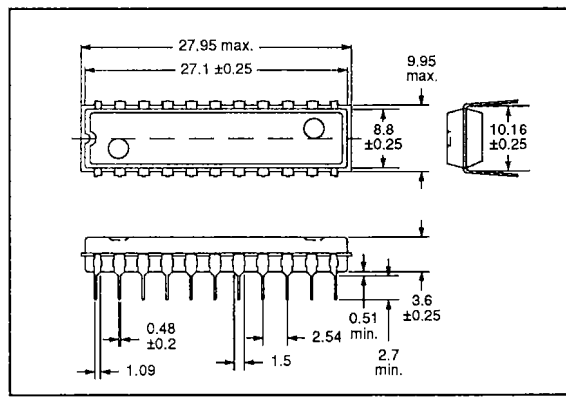
**PINOUT**



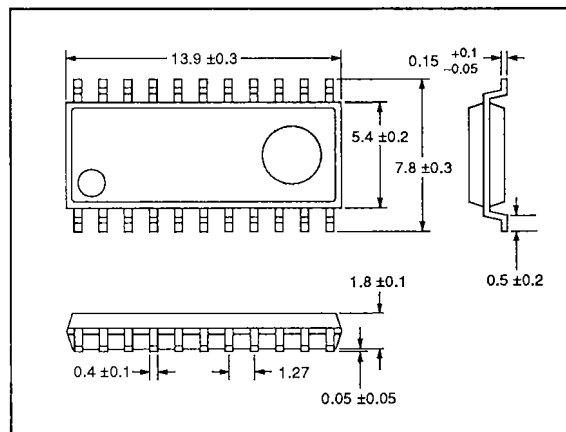
**PACKAGE DIMENSIONS**

Unit: mm

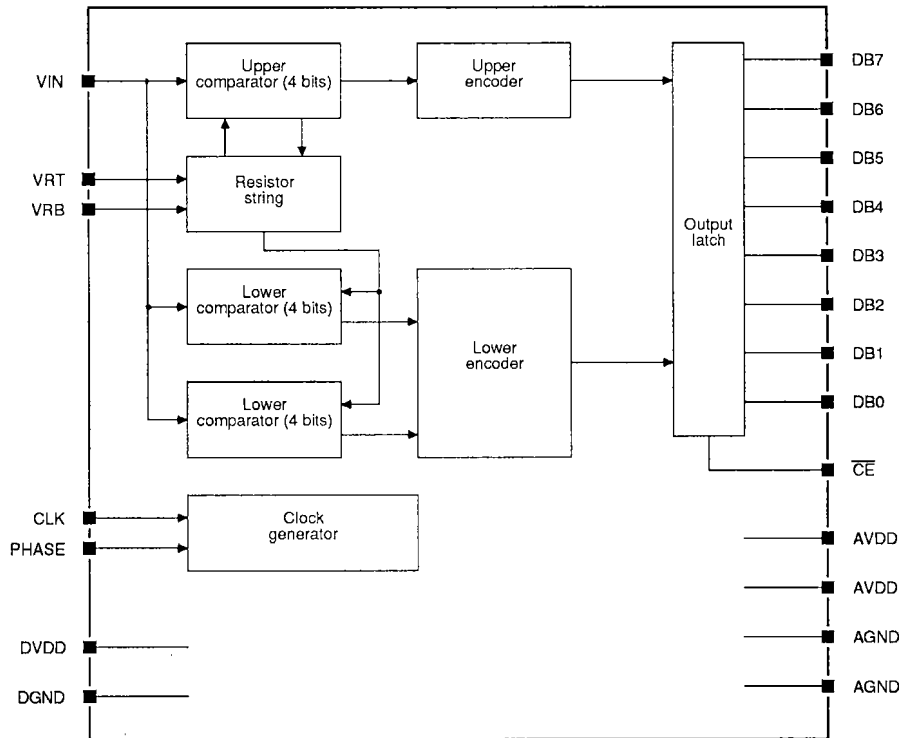
**22-pin DIP**



**22-pin SOP**



**BLOCK DIAGRAM**



**PIN DESCRIPTION**

Number	Name	Description
1	AVDD	Analog supply
2	VRT	Reference voltage (top end)
3	VIN	Analog input
4	AVDD	Analog supply
5	PHASE	Clock polarity switch control
6	$\overline{CE}$	Output tristate control
7	NC	No connection
8	NC	No connection
9	AGND	Analog ground
10	VRB	Reference voltage (bottom end)
11	AGND	Analog ground
12	DGND	Digital ground
13	DB0	Converter data output bit 0 (LSB)
14	DB1	Converter data output bit 1
15	DB2	Converter data output bit 2
16	DB3	Converter data output bit 3
17	DB4	Converter data output bit 4
18	DB5	Converter data output bit 5

## SM6102P/S

Number	Name	Description
19	DB6	Converter data output bit 6
20	DB7	Converter data output bit 7 (MSB)
21	CLK	Clock input
22	DVDD	Digital supply

## SPECIFICATIONS

### Absolute Maximum Ratings

$V_{GND} = 0 \text{ V}$

Parameter	Symbol	Rating	Unit
Supply voltage range	$V_{DD}$	-0.3 to 7.0	V
Input voltage range	$V_{IN}$	-0.3 to $V_{DD} + 0.3$	V
Output voltage range	$V_{OUT}$	-0.3 to $V_{DD} + 0.3$	V
Storage temperature range	$T_{stg}$	-40 to 125	deg. C
Power dissipation	$P_D$	350	mW
Soldering temperature	$T_{sld}$	260	deg. C
Soldering time	$t_{sld}$	10	s

### Recommended Operating Conditions

$V_{GND} = 0 \text{ V}$

Parameter	Symbol	Rating			Unit
		min	typ	max	
Supply voltage	$V_{DD}$	4.75	5.0	5.25	V
Reference voltage (top end)	$V_{RT}$	$V_{RB} + 2.0$	-	$V_{DD} + 0.1$	V
Reference voltage (bottom end)	$V_{RB}$	-0.1	-	$V_{RT} - 2.0$	V
Analog full scale	$V_{RT} - V_{RB}$	2.0	-	-	V
Operating temperature	$T_{opr}$	-20	-	70	deg. C

### DC Electrical Characteristics

$V_{DD} = 5 \text{ V} \pm 5\%$ ,  $f_{CLK} = 8 \text{ MHz}$ ,  $T_a = -20 \text{ to } 70 \text{ deg. C}$  unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
HIGH-level digital input voltage	$V_{IH}$		3.5	-	-	V
LOW-level digital input voltage	$V_{IL}$		-	-	1.0	V
HIGH-level digital input current	$I_{IH}$	$V_{IN} = V_{DD}$	-	-	2	$\mu\text{A}$
LOW-level digital input current	$I_{IL}$	$V_{IN} = 0 \text{ V}$	-2	-	-	$\mu\text{A}$
HIGH-level digital output voltage	$V_{OH}$	$I_{OH} = -0.4 \text{ mA}$	2.7	-	-	V
LOW-level digital output voltage	$V_{OL}$	$I_{OL} = 1.6 \text{ mA}$	-	-	0.4	V
HIGH-level tristate output leakage current	$I_{OHL}$	$V_O = V_{DD}$	-	-	3	$\mu\text{A}$

## SM6102P/S

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
LOW-level tristate output leakage current	$I_{OLL}$	$V_O = 0\text{ V}$	-3	-	-	$\mu\text{A}$
Analog input resistance	$R_{VIN}$	$V_{IN} = \text{DC}$	1	-	-	$\text{M}\Omega$
Analog input capacitance	$C_{VIN}$		-	30	-	$\text{pF}$
Reference resistance	$R_{REF}$	$V_{RT}$ to $V_{RB}$	260	400	600	$\Omega$
Current consumption	$I_{DD}$		-	20	30	$\text{mA}$

### AC Electrical Characteristics

$V_{DD} = 5\text{ V} \pm 5\%$ ,  $T_a = -20$  to  $70$  deg. C unless otherwise noted

Parameter	Symbol	Rating			Unit
		min	typ	max	
CLK HIGH-level pulsewidth	$t_{PWH}$	60	-	5000	ns
CLK LOW-level pulsewidth	$t_{PWL}$	60	-	5000	ns
Aperture time	$t_A$	-	10	-	ns
Digital output delay time	$t_D$	-	25	40	ns
Conversion speed	FS	-	-	8	MSPS

### Converter Characteristics

$V_{DD} = 5\text{ V} \pm 5\%$ ,  $T_a = -20$  to  $70$  deg. C unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Resolution	RES		-	-	8	Bits
Non-linearity error	NL	$V_{RT} - V_{RB} = 2\text{ V}$ , $V_{IN} = \text{DC}$	-	-	$\pm 1.5$	LSB
		$V_{RT} - V_{RB} = 5\text{ V}$ , $V_{IN} = \text{DC}$	-	-	$\pm 1.0$	
Differential non-linearity error	DNL	$V_{RT} - V_{RB} = 2\text{ V}$ , $V_{IN} = \text{DC}$	-	-	$\pm 1.0$	LSB
		$V_{RT} - V_{RB} = 5\text{ V}$ , $V_{IN} = \text{DC}$	-	-	$\pm 0.75$	

## FUNCTIONAL DESCRIPTION

### Converter Operation

The SM6102P/S uses a 2-step flash conversion method where one step sets the upper four bits and the next sets the lower four bits. The lower comparator comprises two circuits, A and B, which operate alternately at a rate set by the input clock frequency.

#### When PHASE = LOW

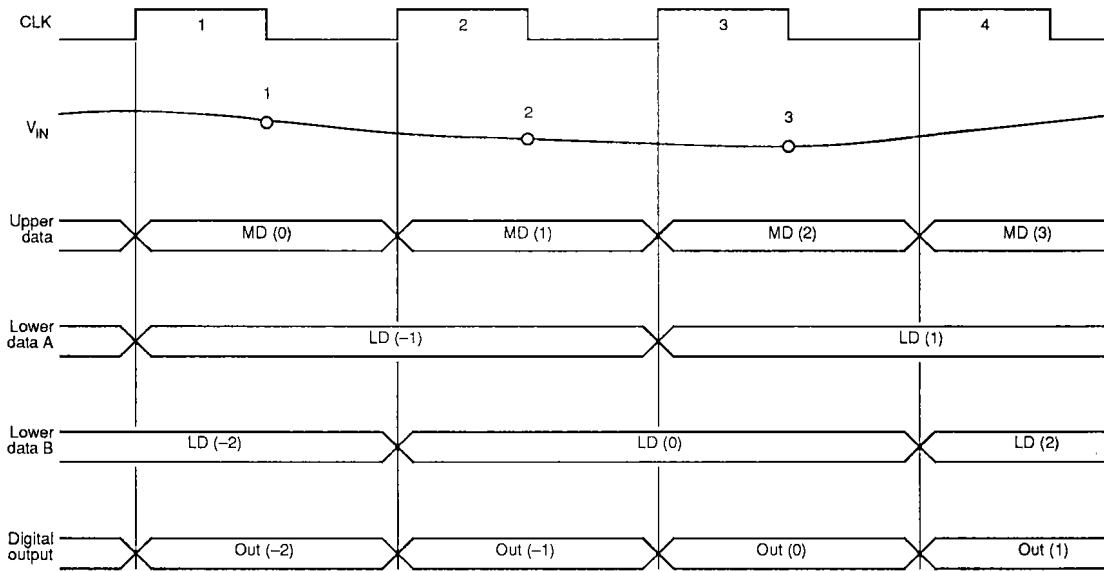
When CLK is HIGH, the upper and lower comparator (block A, for example) threshold voltages are balanced automatically. The analog input is then sampled on the first falling edge of CLK. On the second rising edge of CLK, the upper four bits are

set and the upper comparator sets the threshold voltage for the lower comparator. The lower four bits are set on the third rising edge of CLK. On the fourth rising edge of CLK, the upper and lower bits are re-combined and converted. The conversion, therefore, takes 2.5 clock cycles from the input sampling to the converter data output.

Lower comparator B operates identically to comparator A except that it is shifted by one clock cycle.

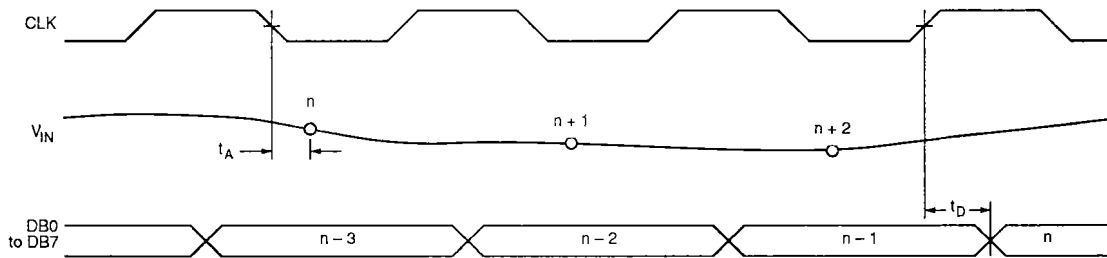
**When PHASE = HIGH**

The converter operates similarly as when PHASE is LOW, except that the CLK signal has opposite polarity.

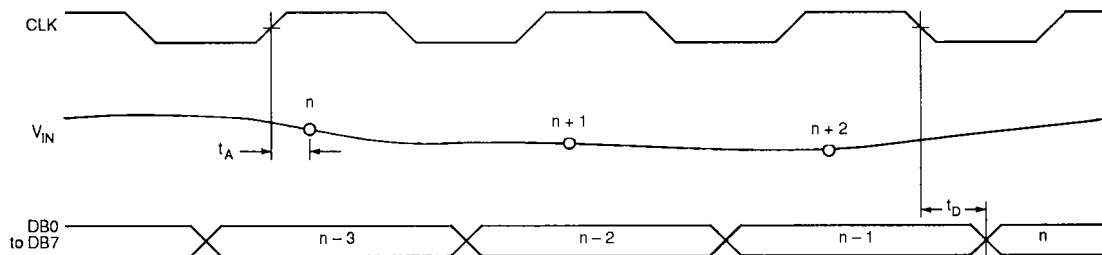


**Converter Timing**

**PHASE = LOW**



**PHASE = HIGH**



## Output Tristate Control

CE	DB0 to DB7
LOW	Enable
HIGH	High impedance

## Output Codes

Analog input voltage (V)	Output code								Decimal steps
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0.00	0	0	0	0	0	0	0	0	0
0.01	0	0	0	0	0	0	0	1	1
0.02	0	0	0	0	0	0	1	0	2
0.03	0	0	0	0	0	0	1	1	3
0.04	0	0	0	0	0	1	0	0	4
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
2.51	1	1	1	1	1	0	1	1	251
2.52	1	1	1	1	1	1	0	0	252
2.53	1	1	1	1	1	1	0	1	253
2.54	1	1	1	1	1	1	1	0	254
2.55	1	1	1	1	1	1	1	1	255

## Notes

1. The analog input voltage shown is the center voltage for each step.
2.  $V_{RT}$  and  $V_{RB}$  are adjusted such that the zero transition is 0.005 V and full-scale is 2.545 V.

## DEVICE HANDLING PRECAUTIONS

1. Parallel electrolytic and ceramic filter capacitors should be connected to the supply and reference voltage pins.
2. The system ground should be connected to a single, common Earth.
3. As far as practicable, the analog input should be kept free of digital noise. For example, analog input wire on the printed circuit board should be screened by AGND.
4. The SM6102 uses CMOS chopper comparators where the analog input is alternately connected and disconnected from the input circuits. The analog inputs should, therefore, have a low impedance. Also, input buffering is recommended.

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