

## OVERVIEW

The SM6105 and SM6106 are multi-channel, 8-bit A/D converters fabricated in Molybdenum-gate CMOS. They feature fast conversion times for four or eight channels, respectively, using a half-flash conversion method. They do not require an external sample-and-hold circuit, and can operate with or without an external microprocessor.

The SM6105 is available in 24-pin plastic skinny DIPs and 24-pin SOPs, and the SM6106, in 28-pin plastic DIPs and 28-pin SOPs.

## FEATURES

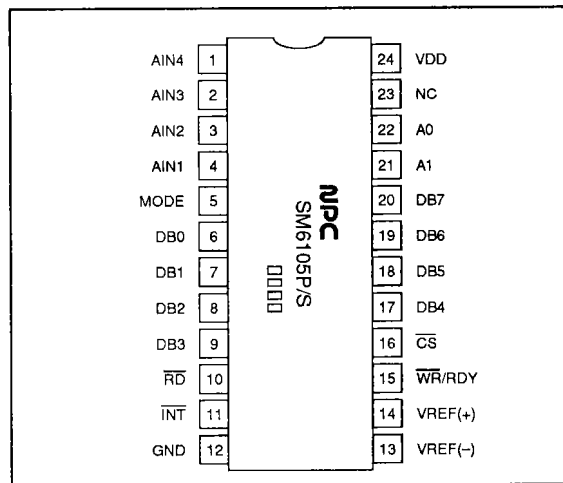
- 8-bit resolution
- Four (SM6105) or eight (SM6106) multiplexed input channels
- 1.3  $\mu\text{s}$  (max) conversion time in RD mode and 0.7  $\mu\text{s}$  (max) in WR-RD mode
- External sample-and-hold circuit not required for input signals with less than 200 mV/s slew rate
- 7 mA (typ) current consumption (excluding VREF current)
- $\pm 0.7$  LSB (max) non-linearity
- $\pm 0.7$  LSB (max) differential non-linearity
- No external clock required
- Direct microprocessor interface
- TTL- and CMOS-compatible input/outputs
- Single 5 V supply
- 24-pin plastic skinny DIP and 24-pin SOP (SM6105)
- 28-pin plastic DIP and 28-pin SOP (SM6106)
- Molybdenum-gate CMOS process

## APPLICATIONS

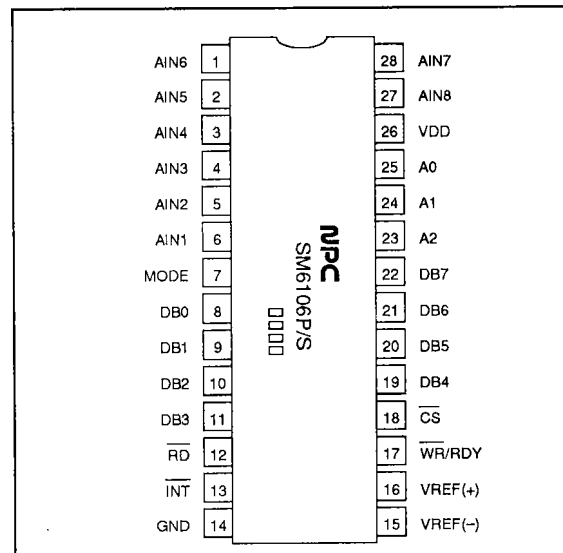
- Data acquisition systems
- Measuring instruments
- Process control

## PINOUT

### SM6105



### SM6106

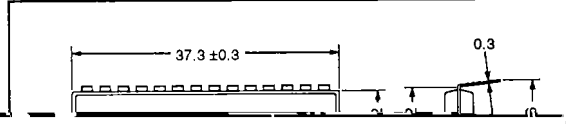
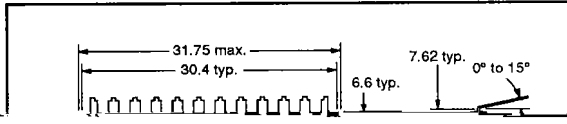


**PACKAGE DIMENSIONS**

Unit: mm

**24-pin plastic skinny DIP (SM6105)**

**28-pin plastic DIP (SM6106)**



## PIN DESCRIPTION

| Number |        | Name                | Description   |
|--------|--------|---------------------|---|
| SM6105 | SM6106 |                     |   |
| –      | 1      | AIN6                | Analog input channel 6  |
| –      | 2      | AIN5                | Analog input channel 5  |
| 1      | 3      | AIN4                | Analog input channel 4  |
| 2      | 4      | AIN3                | Analog input channel 3  |
| 3      | 5      | AIN2                | Analog input channel 2  |
| 4      | 6      | AIN1                | Analog input channel 1  |
| 5      | 7      | MODE                | Mode select input with internal pull-down resistance. RD mode when LOW or open, and WR-RD mode when HIGH  |
| 6      | 8      | DB0                 | Tristate data output bit 0 (LSB)  |
| 7      | 9      | DB1                 | Tristate data output bit 1  |
| 8      | 10     | DB2                 | Tristate data output bit 2  |
| 9      | 11     | DB3                 | Tristate data output bit 3  |
| 10     | 12     | $\overline{RD}$     | WR-RD mode: The results of the last conversion are output on DB0 to DB7 when $\overline{CS}$ and $\overline{INT}$ are LOW and $\overline{RD}$ is pulled LOW. If $\overline{RD}$ is pulled LOW before the internal conversion time has elapsed (approx. 400 ns), the conversion results are latched and output. For stand-alone operation, $\overline{RD}$ should be held LOW.<br>RD mode: Conversion begins when $\overline{CS}$ is LOW and $\overline{RD}$ is pulled LOW. Mode A or B is selected depending on whether $\overline{RD}$ is held LOW until conversion is completed or $\overline{RD}$ is returned HIGH before conversion is completed. |
| 11     | 13     | $\overline{INT}$    | $\overline{INT}$ goes LOW when conversion is completed and the data is latched. $\overline{INT}$ returns HIGH on the rising edge of $\overline{RD}$ or $\overline{CS}$ .  |
| 12     | 14     | GND                 | Ground  |
| 13     | 15     | VREF–               | Reference voltage input (low end)   |
| 14     | 16     | VREF+               | Reference voltage input (high end)  |
| 15     | 17     | $\overline{WR}/RDY$ | WR-RD mode ( $\overline{WR}$ input): Conversion is started on the falling edge of $\overline{WR}$ . If $\overline{RD}$ is HIGH, the conversion is completed approx. 400 ns after the rising edge of $\overline{WR}$ . $\overline{INT}$ then goes LOW and the data is latched.<br>RD mode (RDY output): This is an N-channel open-drain output. RDY goes LOW on the falling edge of $\overline{CS}$ or $\overline{RD}$ . It enters a high-impedance state when conversion is completed (mode A) or on the falling edge of $\overline{CS}$ or $\overline{RD}$ (mode B).   |
| 16     | 18     | $\overline{CS}$     | Chip select input. $\overline{RD}$ and $\overline{WR}$ propagate through the internal circuits only when $\overline{CS}$ is LOW.  |
| 17     | 19     | DB4                 | Tristate data output bit 4  |
| 18     | 20     | DB5                 | Tristate data output bit 5  |
| 19     | 21     | DB6                 | Tristate data output bit 6  |
| 20     | 22     | DB7                 | Tristate data output bit 7 (MSB)  |
| –      | 23     | A2                  | Analog channel select inputs with internal pull-down resistances  |
| 21     | 24     | A1                  |   |
| 22     | 25     | A0                  |   |
| 23     | –      | NC                  | No connection   |
| 24     | 26     | VDD                 | Supply voltage  |

**SM6105/SM6106**

| Number |        | Name | Description            |
|--------|--------|------|------------------------|
| SM6105 | SM6106 |      |                        |
| -      | 27     | AIN8 | Analog input channel 8 |
| -      | 28     | AIN7 | Analog input channel 7 |

**SPECIFICATIONS**

**Absolute Maximum Ratings**

$V_{SS} = 0 \text{ V}$

| Parameter                   | Symbol    | Rating                 | Unit   |
|-----------------------------|-----------|------------------------|--------|
| Supply voltage range        | $V_{DD}$  | -0.3 to 7.0            | V      |
| Input voltage range         | $V_{IN}$  | -0.3 to $V_{DD} + 0.3$ | V      |
| Output voltage range        | $V_{OUT}$ | -0.3 to $V_{DD} + 0.3$ | V      |
| Power dissipation           | $P_D$     | 250                    | mW     |
| Operating temperature range | $T_{opr}$ | -20 to 80              | deg. C |
| Storage temperature range   | $T_{stg}$ | -40 to 125             | deg. C |
| Soldering temperature       | $T_{sld}$ | 260                    | deg. C |
| Soldering time              | $t_{sld}$ | 10                     | s      |

**Recommended Operating Conditions**

| Parameter             | Symbol    | Rating |     |      | Unit   |
|-----------------------|-----------|--------|-----|------|--------|
|                       |           | min    | typ | max  |        |
| Supply voltage        | $V_{DD}$  | 4.75   | 5.0 | 5.25 | V      |
| Operating temperature | $T_{opr}$ | -20    | -   | 70   | deg. C |

**DC Electrical Characteristics**

$V_{DD} = 5 \text{ V} \pm 5\%$ ,  $T_a = -20 \text{ to } 70 \text{ deg. C}$ , unless otherwise noted

| Parameter   | Symbol      | Condition   | Rating |           |                | Unit          |
|---|-------------|---|--------|-----------|----------------|---------------|
|   |             |   | min    | typ       | max            |               |
| $V_{REF+}$ to $V_{REF-}$ reference resistance   | $R_{REF}$   |   | 0.5    | 0.85      | 1.3            | k $\Omega$    |
| Analog input voltage  | $V_{IN}$    |   | -0.1   |           | $V_{DD} + 0.1$ | V             |
| Analog input leakage current  | $I_{LEAK1}$ | $V_{IN} = 0 \text{ V to } V_{DD}$ ,<br>$V_{\overline{CS}} = V_{\overline{WR}} = 0 \text{ V}$ ,<br>$V_{MODE} = V_{DD}$ | -      | $\pm 0.1$ | $\pm 3$        | $\mu\text{A}$ |
| $\overline{CS}$ , $\overline{WR}$ , $\overline{RD}$ and A0 to A2 HIGH-level input voltage | $V_{IH1}$   |   | 2.4    | -         | -              | V             |
| MODE HIGH-level input voltage   | $V_{IH2}$   |   | 3.5    | -         | -              | V             |
| $\overline{CS}$ , $\overline{WR}$ , $\overline{RD}$ and A0 to A2 LOW-level input voltage  | $V_{IL1}$   |   | -      | -         | 0.8            | V             |
| MODE LOW-level input voltage  | $V_{IL2}$   |   | -      | -         | 1.5            | V             |

SM6105/SM6106

| Parameter   | Symbol      | Condition   | Rating |     |     | Unit    |
|---|-------------|---|--------|-----|-----|---------|
|   |             |   | min    | typ | max |         |
| $\overline{CS}$ and $\overline{RD}$ HIGH-level input current                                    | $I_{IH1}$   | $V_{IH} = V_{DD}$   | –      | –   | 1   | $\mu A$ |
| WR HIGH-level input current   | $I_{IH2}$   | $V_{IH} = V_{DD}$   | –      | –   | 3   | $\mu A$ |
| MODE and A0 to A2 HIGH-level input current  | $I_{IH3}$   | $V_{IH} = V_{DD}$   | –      | 60  | –   | $\mu A$ |
| $\overline{CS}$ , $\overline{WR}$ , $\overline{RD}$ , MODE and A0 to A2 LOW-level input current | $I_{IL}$    | $V_{IL} = 0 V$  | –1     | –   | –   | $\mu A$ |
| DB0 to DB7 and $\overline{INT}$ HIGH-level output voltage                                       | $V_{OH}$    | $I_{source} = 360 \mu A$  | 4      | –   | –   | V       |
| DB0 to DB7, $\overline{INT}$ and RDY LOW-level output voltage                                   | $V_{OL}$    | $I_{sink} = 1.6 mA$   | –      | –   | 0.4 | V       |
| DB0 to DB7 high-impedance leakage current   | $I_{LEAK2}$ | $V_{OUT} = V_{DD}$  | –      | –   | 3   | $\mu A$ |
|   |             | $V_{OUT} = 0 V$   | –3     | –   | –   |         |
| Current consumption   | $I_{DD}$    | Not operating,<br>$V_{\overline{CS}} = V_{\overline{RD}} = V_{MODE} = 0 V$  | –      | 5   | –   | mA      |
|   |             | Operating $t_{WR} = 250 ns$ ,<br>$t_{RD} = 300 ns$ ,<br>$RD_{PW} = 150 ns$ ,<br>$t_P = 100 ns$ ,<br>$V_{MODE} = V_{DD}$ | –      | 7   | –   |         |
| AIN1 to AIN8 analog input pin capacitance   | $C_{VIN}$   |   | –      | 30  | –   | pF      |
| Logic output pin capacitance  | $C_{OUT}$   |   | –      | 5   | –   | pF      |
| Logic input pin capacitance   | $C_{IN}$    |   | –      | 5   | –   | pF      |

AC Electrical Characteristics

$V_{DD} = 5 V \pm 5\%$ ,  $t_r = t_f = 20 ns$ ,  $T_a = -20$  to  $70$  deg. C

| Parameter                                      | Symbol                       | Condition                                   | Rating |                |                | Unit       |
|--|------------------------------|---|--------|----------------|----------------|------------|
|  |                              |   | min    | typ            | max            |            |
| RD mode conversion time                        | $t_{CRD}$                    |   | –      | 0.8            | 1.3            | $\mu s$    |
| WR-RD mode B conversion time                   | $t_{WR} + t_{RD} + t_{ACC1}$ | $t_{WR} = 250 ns$ ,<br>$t_{RD} = 300 ns$    | –      | –              | 0.7            | $\mu s$    |
| Input signal slew rate                         | SR                           |   | –      | –              | 0.2            | V/ $\mu s$ |
| A0 to A2 setup time                            | $t_{AS}$                     |   | 0      | –              | –              | ns         |
| A0 to A2 hold time                             | $t_{AH}$                     |   | 35     | –              | –              | ns         |
| $\overline{CS}$ to RDY delay time              | $t_{RDY}$                    | RD mode                                     | –      | 30             | 60             | ns         |
| $\overline{RD}$ to $\overline{INT}$ delay time | $t_{INTH}$                   |   | –      | 50             | 100            | ns         |
| Data access time                               | $t_{ACC}$                    | RD mode A. See note 2.                      | –      | $t_{CRD} + 20$ | $t_{CRD} + 40$ | ns         |
| Data hold time                                 | $t_{DH}$                     | See note 3.                                 | –      | 50             | 100            | ns         |
| $\overline{RD}$ pulsewidth                     | $\overline{RD}_{PW1}$        | RD mode B                                   | 70     | –              | 300            | ns         |
| Data access time                               | $t_{ACC2}$                   | RD mode B, WR-RD modes A and B. See note 2. | –      | 50             | 100            | ns         |

SM6105/SM6106

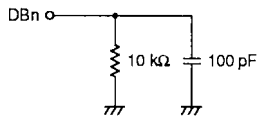
| Parameter                                     | Symbol                | Condition                    | Rating |               |                | Unit    |
|---|-----------------------|------------------------------|--------|---------------|----------------|---------|
|   |                       |                              | min    | typ           | max            |         |
| $\overline{WR}$ pulsewidth                    | $t_{WR}$              | WR-RD mode                   | 0.25   | –             | 50             | $\mu s$ |
| $\overline{WR}$ to $\overline{RD}$ setup time | $t_{RD}$              | WR-RD modes A and B          | 300    | –             | –              | ns      |
| $\overline{WR}$ to $\overline{RD}$ setup time | $t_{INTL}$            | WR-RD mode A                 | –      | –             | $t_i$          | ns      |
|   |                       | WR-RD mode B                 | –      | $t_{RD} + 50$ | $t_{RD} + 100$ |         |
| Data access time                              | $t_{ACC1}$            | WR-RD mode B.<br>See note 2. | –      | 80            | 150            | ns      |
| $\overline{RD}$ pulsewidth                    | $\overline{RD}_{PW2}$ | WR-RD modes A and B          | 150    | –             | –              | ns      |
| Internal comparison time                      | $t_i$                 | WR-RD mode                   | –      | 400           | 650            | ns      |
| $\overline{INT}$ to data delay time           | $t_{ID}$              | WR-RD mode C.<br>See note 2. | –      | 20            | 40             | ns      |
| Succeeding conversion wait time               | $t_p$                 |                              | 100    | –             | –              | ns      |

Notes

1. All timing is measured at a signal control level of 1.6 V.
2. Measured using the data access test circuits at output levels of 1.6 V.
3. Measured using the data hold test circuits at output levels of 1.6 V.

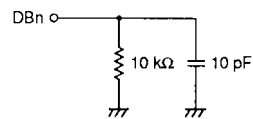
Data access test circuits

$V_{OH}$  from high impedance

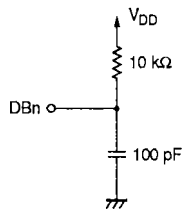


Data hold test circuits

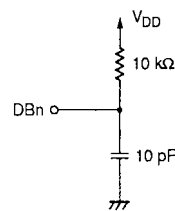
High impedance from  $V_{OH}$



$V_{OL}$  from high impedance



High impedance from  $V_{OL}$



Converter Characteristics

$V_{DD} = 5 V \pm 5\%$ ,  $V_{REF+} = 5 \pm 0.5 V$ ,  $V_{REF-} = 0 V$ ,  $T_a = -20$  to  $70$  deg. C

| Parameter                  | Rating |     |           | Unit |
|----------------------------|--------|-----|-----------|------|
|                            | min    | typ | max       |      |
| Resolution                 | 8      | –   | –         | bit  |
| Non-linearity              | –      | –   | $\pm 0.7$ | LSB  |
| Differential non-linearity | –      | –   | $\pm 0.7$ | LSB  |
| Offset error               | –      | –   | $\pm 0.7$ | LSB  |
| Gain error                 | –      | –   | $\pm 0.7$ | LSB  |

## FUNCTIONAL DESCRIPTION

The SM6105 and SM6106 comprise two parallel A/D converters, one each for the upper and lower four bits of the 8-bit output.

When both  $\overline{RD}$  and  $\overline{CS}$  go LOW (RD mode) or both  $\overline{WR}$  and  $\overline{CS}$  go LOW (WR-RD mode), analog data on the selected input channel is latched and conversion begins. The fifteen comparators in the upper converter (upper four bits) set the threshold levels for the fifteen comparators in the lower converter (lower four bits). The data is then latched and buffered for output.

The SM6105 and SM6106 have two basic modes of operation, set by the level on MODE. If MODE is LOW or open, RD mode is selected, and if MODE is HIGH, WR-RD mode is selected. These two basic modes also have sub-modes of operation, according to the timing of  $\overline{CS}$ ,  $\overline{RD}$  and  $\overline{WR}$ .

### RD Mode (MODE = LOW or open)

#### Mode A

This mode is provided for microprocessors that support wait cycles. When  $\overline{CS}$  is LOW, the CPU can strobe  $\overline{RD}$  LOW. The data on the selected input channel is latched on the falling edge of  $\overline{CS}$ , then RDY goes LOW and conversion begins.  $\overline{INT}$  goes LOW to signal the CPU that the conversion has completed approximately 800 ns later, and the data is output.

### Input Channel Selection

| A2 | A1 | A0 | Channel |
|----|----|----|---------|
| 0  | 0  | 0  | AIN1    |
| 0  | 0  | 1  | AIN2    |
| 0  | 1  | 0  | AIN3    |
| 0  | 1  | 1  | AIN4    |
| 1  | 0  | 0  | AIN5    |
| 1  | 0  | 1  | AIN6    |
| 1  | 1  | 0  | AIN7    |
| 1  | 1  | 1  | AIN8    |

The thick line indicates the data that applies to the SM6105.

If RDY is connected to a pull-up resistor, RDY goes HIGH on the falling edge of  $\overline{INT}$ , thus acting as the bus wait signal for the CPU.  $\overline{INT}$  returns HIGH and the outputs go high impedance on the rising edge of  $\overline{RD}$  or  $\overline{CS}$ .

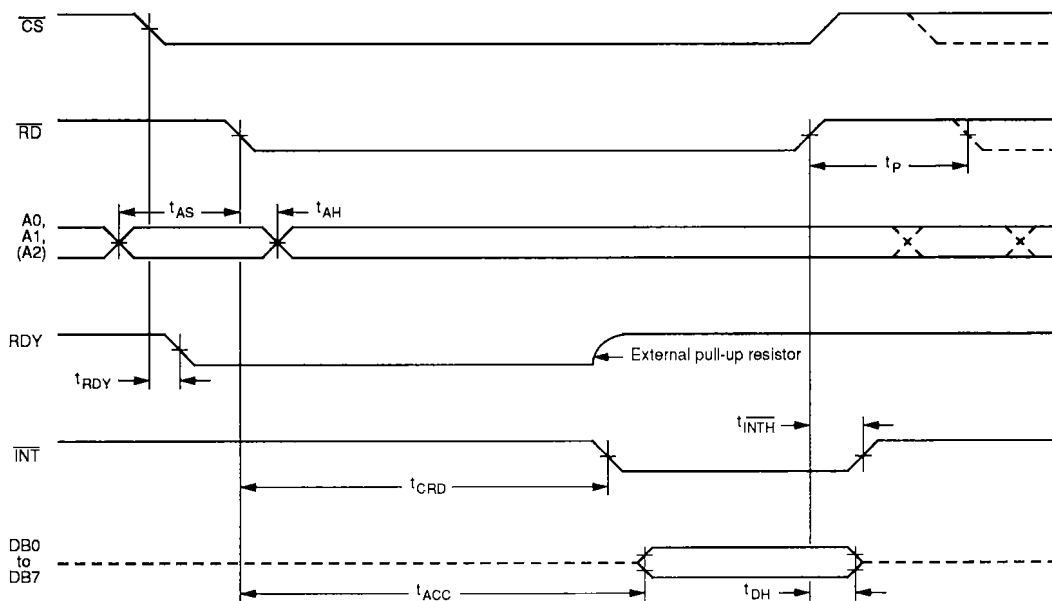


Figure 1. RD mode A

**Mode B**

This mode is provided for microprocessors that do not support wait cycles. When  $\overline{CS}$  is LOW, the CPU can strobe  $\overline{RD}$  LOW. The data on the selected input channel is latched on the falling edge of  $\overline{CS}$ , then RDY goes LOW and conversion begins.  $\overline{INT}$

goes HIGH on the rising edge of  $\overline{RD}$  or  $\overline{CS}$ , and then LOW again when conversion completes. The output data is read by strobing  $\overline{RD}$  LOW again; this also starts the succeeding conversion cycle.

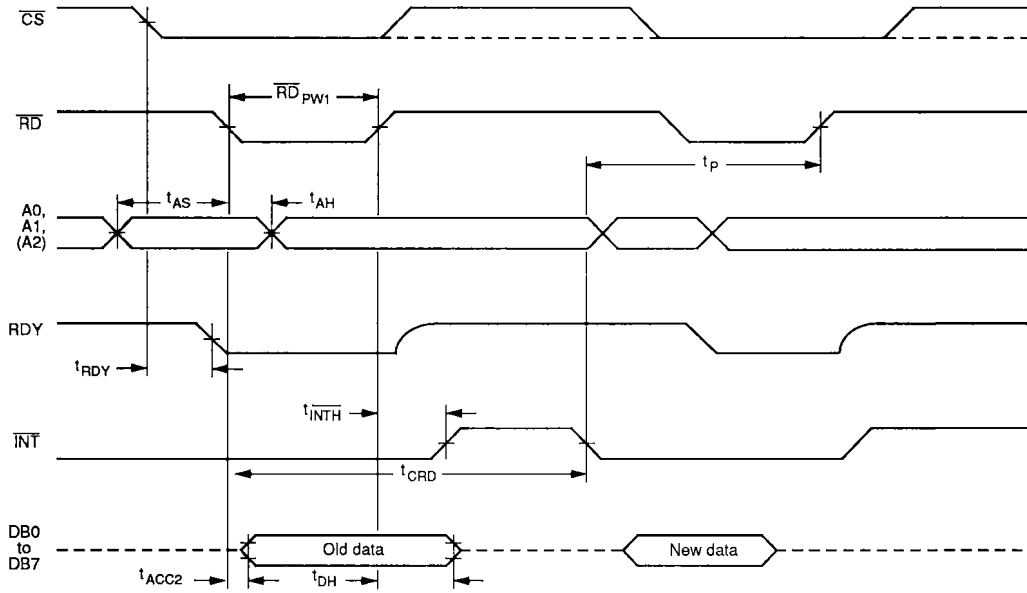


Figure 2. RD mode B



**WR-RD Mode (MODE = HIGH)**

**Mode A**

When  $\overline{CS}$  is LOW, either  $\overline{RD}$  or  $\overline{WR}$  can be pulled LOW. The data on the selected input channel is latched on the falling edge of  $\overline{WR}$ , and conversion begins. If  $\overline{RD}$  is held HIGH,  $\overline{INT}$  goes LOW approximately 400 ns after the rising edge of  $\overline{WR}$ ,

to inform the CPU that conversion is complete, and the output data is latched. When  $\overline{RD}$  goes LOW, the output data is output on DB0 to DB7 to be read by the CPU. In this mode, the CPU is effectively performing interrupt processing.

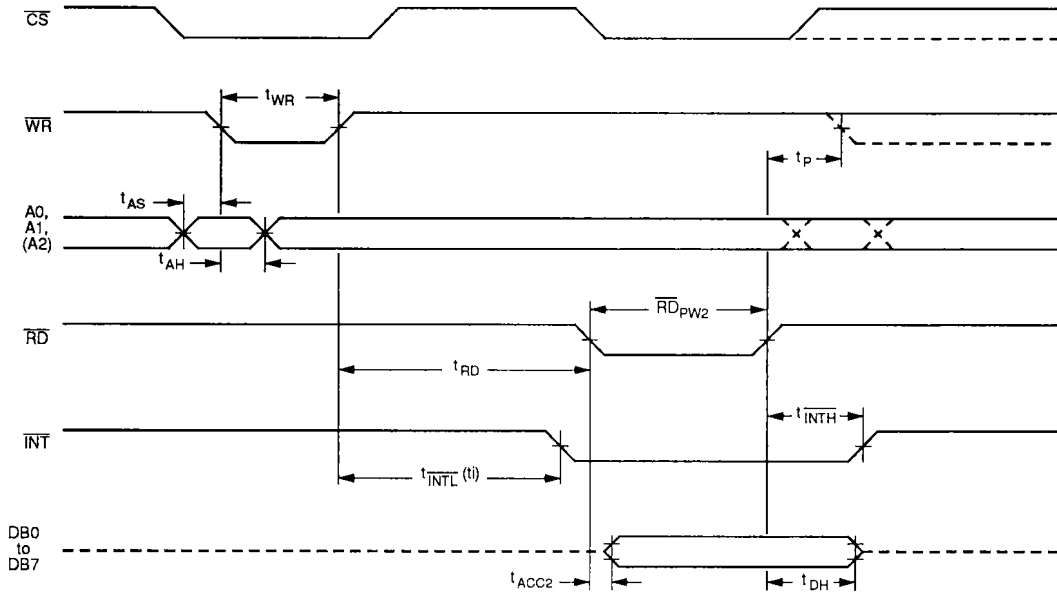


Figure 3. WR-RD mode A ( $t_{RD} > t_i$ )

**Mode B**

In mode A,  $\overline{RD}$  is not pulled LOW until after  $\overline{INT}$  goes LOW, indicating conversion completion. In mode B, however,  $\overline{RD}$  is pulled LOW earlier to shorten the conversion cycle. Provided that the WR-RD setup time ( $t_{RD}$ ) is satisfied, approximately

300 ns,  $\overline{RD}$  can be pulled LOW to complete the conversion without error.  $\overline{INT}$  then goes LOW and the output data is latched and output on DB0 to DB7. In this mode, the CPU is effectively polling the A/D converter.

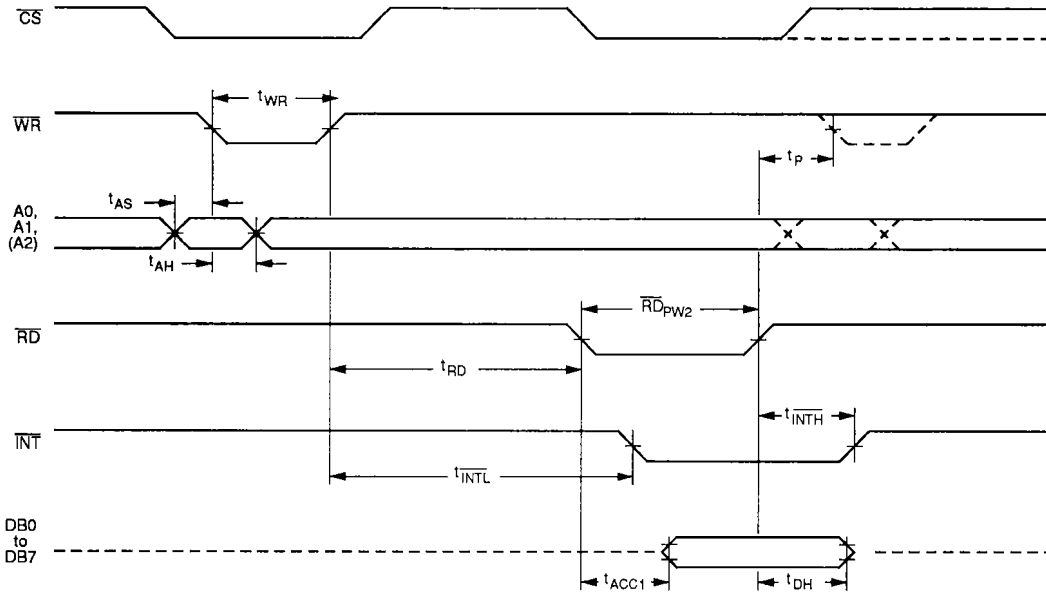


Figure 4. WR-RD mode B ( $t_{RD} < t_i$ )

**Mode C**

In mode C,  $\overline{CS}$  and  $\overline{RD}$  are both tied LOW to allow stand-alone operation (without an external microprocessor). The data on the selected input channel is latched on the falling edge of  $\overline{WR}$ , and conversion begins.  $\overline{INT}$  then goes HIGH on the

rising edge of  $\overline{WR}$ , and the DB0 to DB7 outputs go high impedance.  $\overline{INT}$  then goes LOW again approximately 400 ns after the rising edge of  $\overline{WR}$ , and the output data is output on DB0 to DB7.

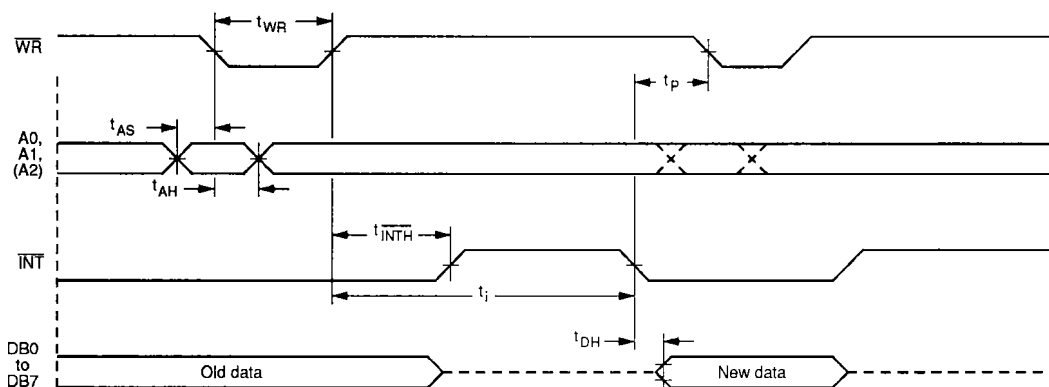
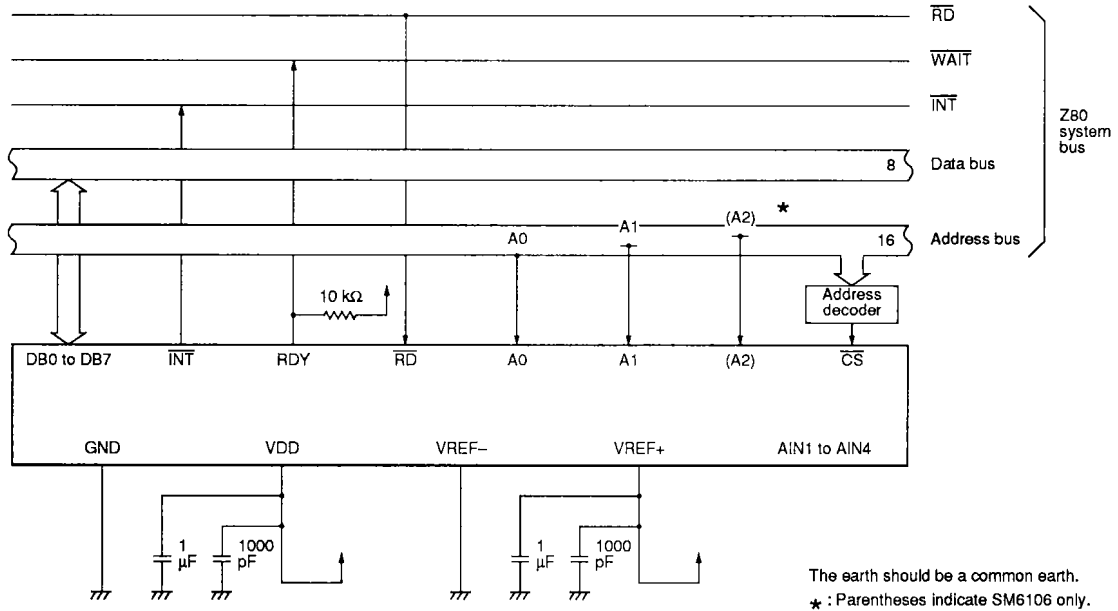


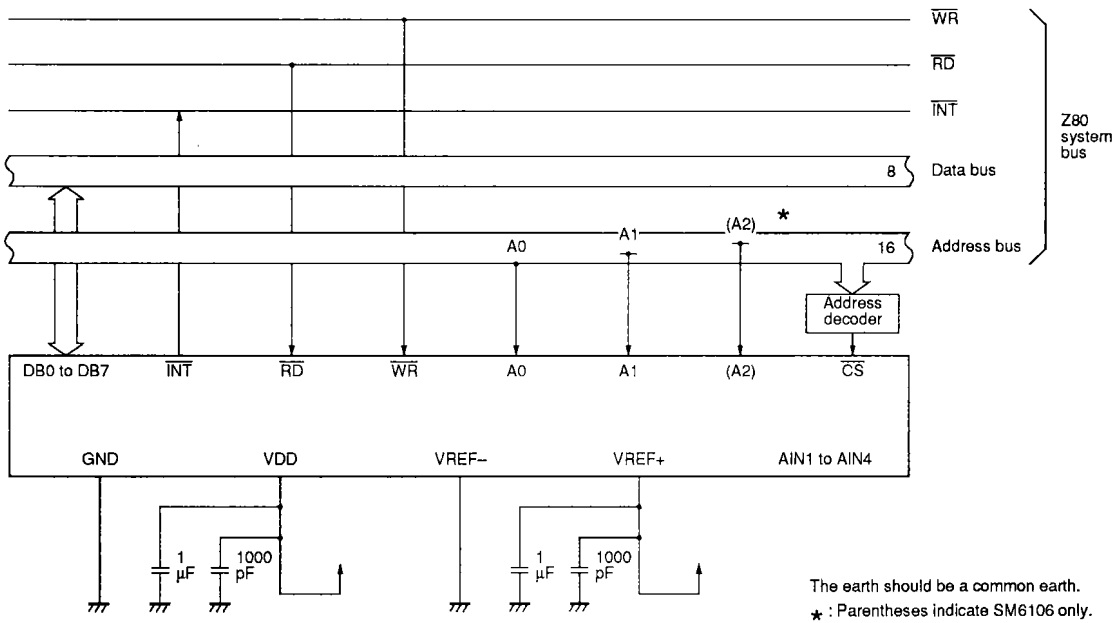
Figure 5. WR-RD mode C ( $\overline{CS} = \overline{RD} = \text{LOW}$ )

Standard Configuration

RD mode



WR-RD mode



## DESIGN NOTE

The SM6105 and SM6106 use CMOS chopper comparators where the analog input is alternately connected and disconnected from the input circuits.

The analog inputs should, therefore, have a low impedance. Also, input buffering is recommended.

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