

100307 Low Power Quint Exclusive OR/NOR Gate

General Description

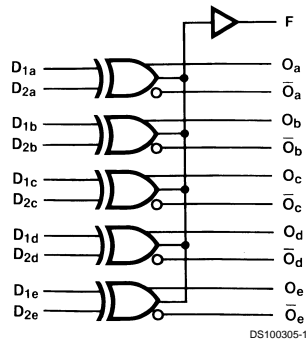
The 100307 is monolithic quint exclusive-OR/NOR gate. The Function output is the wire-OR of all five exclusive-OR outputs. All inputs have 50 kΩ pull-down resistors.

Features

- Low Power Operation

- 2000V ESD protection
- Pin/function compatible with 100107
- Voltage compensated operating range = -4.2V to -5.7V
- Available to industrial grade temperature range
- Available to Standard Microcircuit Drawing (SMD) 5962-9459001

Logic Symbol



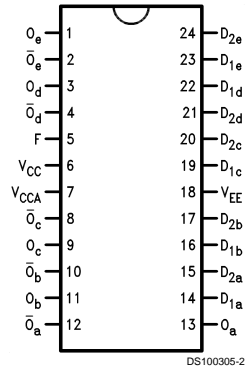
Logic Equation

$$F = (D_{1a} \oplus D_{2a}) + (D_{1b} \oplus D_{2b}) + (D_{1c} \oplus D_{2c}) + (D_{1d} \oplus D_{2d}) + (D_{1e} \oplus D_{2e})$$

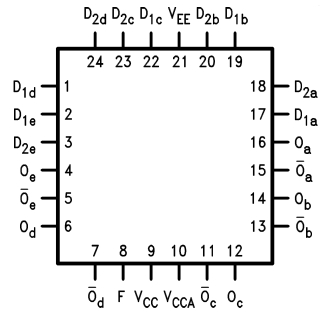
Pin Names	Description
$D_{na}-D_{ne}$	Data Inputs
F	Function Output
O_a-O_e	Data Outputs
$\bar{O}_a-\bar{O}_e$	Complementary Data Outputs

Connection Diagrams

24-Pin DIP



24-Pin Quad Cerpak



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Above which the useful life may be impaired. (Note 1)

Storage Temperature (T _{STG})	-65°C to +150°C
Maximum Junction Temperature (T _J)	
Ceramic	+175°C
Plastic	+150°C
V _{EE} Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	V _{EE} to +0.5V
Output Current (DC Output HIGH)	-50 mA

ESD (Note 2)

≥2000V

Recommended Operating Conditions

Case Temperature (T _C)	
Military	-55°C to +125°C
Supply Voltage (V _{EE})	-5.7V to -4.2V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Military Version DC Electrical Characteristics

V_{EE} = -4.2V to -5.7V, V_{CC} = V_{CCA} = GND, T_C = -55°C to +125°C

Symbol	Parameter	Min	Max	Units	T _C	Conditions	Notes	
V _{OH}	Output HIGH Voltage	-1025	-870	mV	0°C to +125°C	V _{IN} = V _{IH} (Max) or V _{IL} (Min)	Loading with 50Ω to -2.0V	1, 2, 3
		-1085	-870	mV	-55°C			
V _{OL}	Output LOW Voltage	-1830	-1620	mV	0°C to +125°C	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to -2.0V	1, 2, 3
		-1830	-1555	mV	-55°C			
V _{OHC}	Output HIGH Voltage	-1035		mV	0°C to +125°C	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to -2.0V	1, 2, 3
		-1085		mV	-55°C			
V _{OLC}	Output LOW Voltage		-1610	mV	0°C to +125°C	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to -2.0V	1, 2, 3
			-1555	mV	-55°C			
V _{IH}	Input HIGH Voltage	-1165	-870	mV	-55°C to +125°C	Guaranteed HIGH Signal for All Inputs	1, 2, 3, 4	
V _{IL}	Input LOW Voltage	-1830	-1475	mV	-55°C to +125°C	Guaranteed LOW Signal for All Inputs	1, 2, 3, 4	
I _{IL}	Input LOW Current	0.50		μA	-55°C to +125°C	V _{EE} = -4.2V V _{IN} = V _{IL} (Min)	1, 2, 3	
I _{IH}	Input High Current D _{2a} -D _{2e} D _{1a} -D _{1e}		250	μA	0°C to +125°C	V _{EE} = -5.7V V _{IN} = V _{IH} (Max)	1, 2, 3	
			350	μA	-55°C			
	D _{2a} -D _{2e} D _{1a} -D _{1e}		350	μA	-55°C	V _{EE} = -5.7V V _{IN} = V _{IH} (Max)	1, 2, 3	
			500	μA	-55°C			
I _{EE}	Power Supply Current	-75	-25	mA	-55°C to +125°C	Inputs Open	1, 2, 3	

Note 3: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 4: Screen tested 100% on each device at -55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 5: Sample tested (Method 5005, Table I) on each manufactured lot at -55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 6: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay $D_{2a}-D_{2e}$ to O, \bar{O}	0.30	2.10	0.40	1.90	0.40	2.40	ns	Figures 1, 2	1, 2, 3
t_{PLH} t_{PHL}	Propagation Delay $D_{1a}-D_{1e}$ to O, \bar{O}	0.30	1.90	0.40	1.80	0.40	2.20	ns		
t_{PLH} t_{PHL}	Propagation Delay Data to F	0.80	2.90	0.90	2.80	0.90	3.40	ns		
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.70	0.30	1.60	0.20	1.70	ns		4

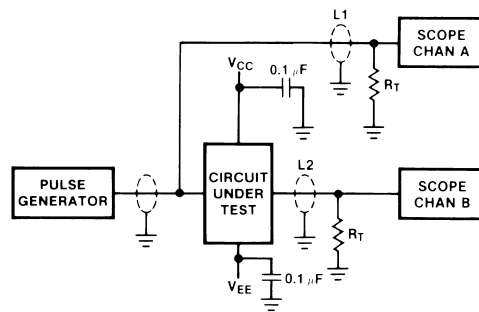
Note 7: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 8: Screen tested 100% on each device at $+25^\circ C$ temperature only, Subgroup A9.

Note 9: Sample tested (Method 5005, Table I) on each mfg. lot at $+25^\circ C$, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.

Note 10: Not tested at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ temperature (design characterization data).

Test Circuitry



DS100305-5

Notes:

$V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$

L1 and L2 = equal length 50Ω impedance lines

$R_T = 50\Omega$ terminator internal to scope

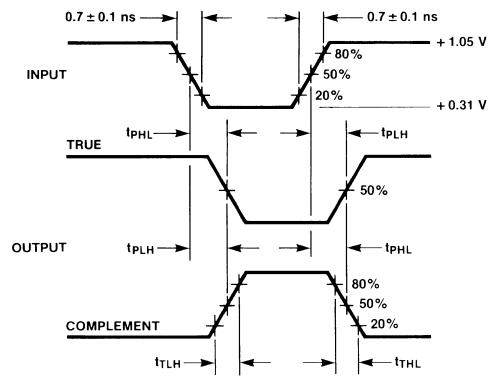
Decoupling $0.1\ \mu F$ from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance $\leq 3\ pF$

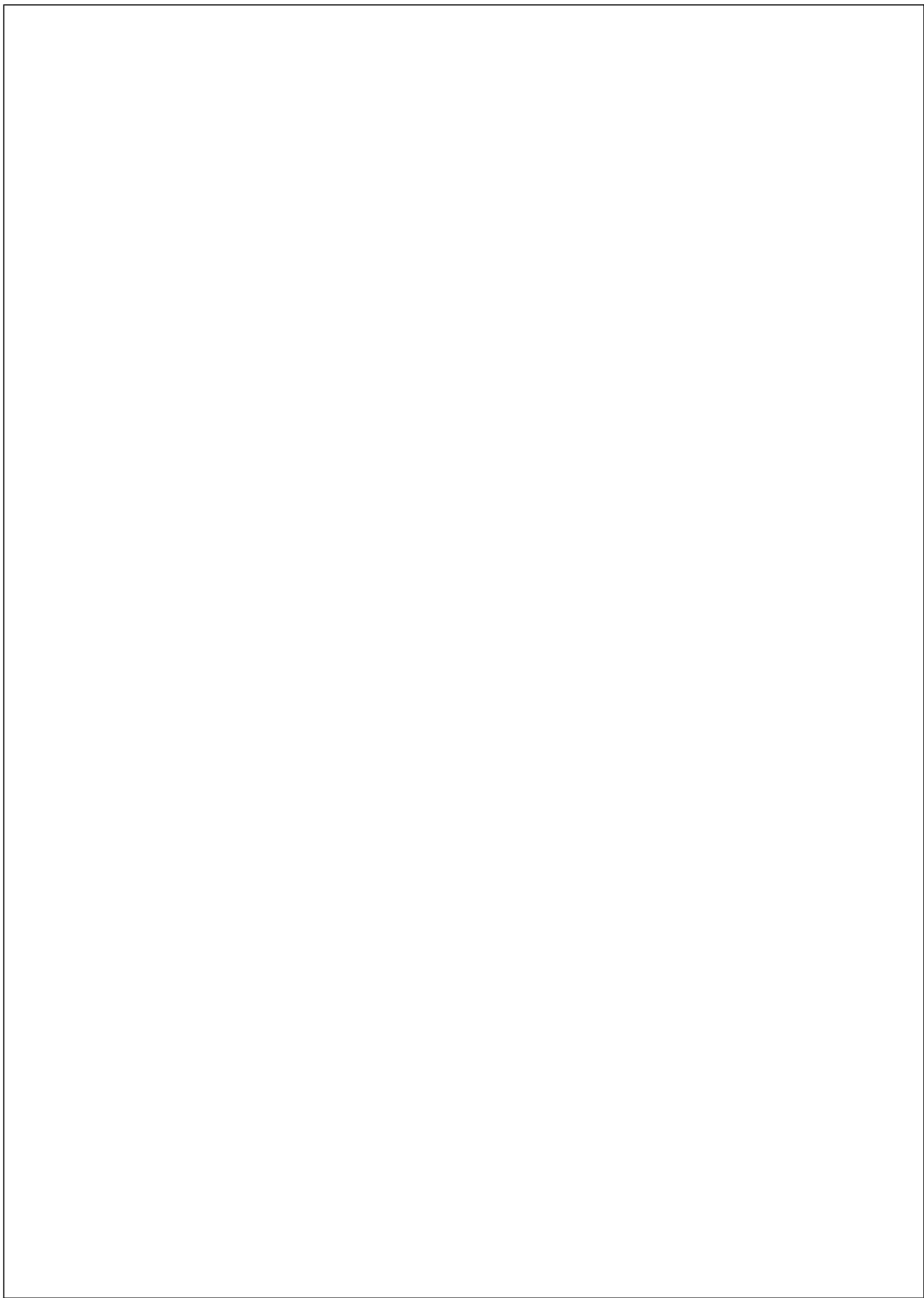
FIGURE 1. AC Test Circuit

Switching Waveforms

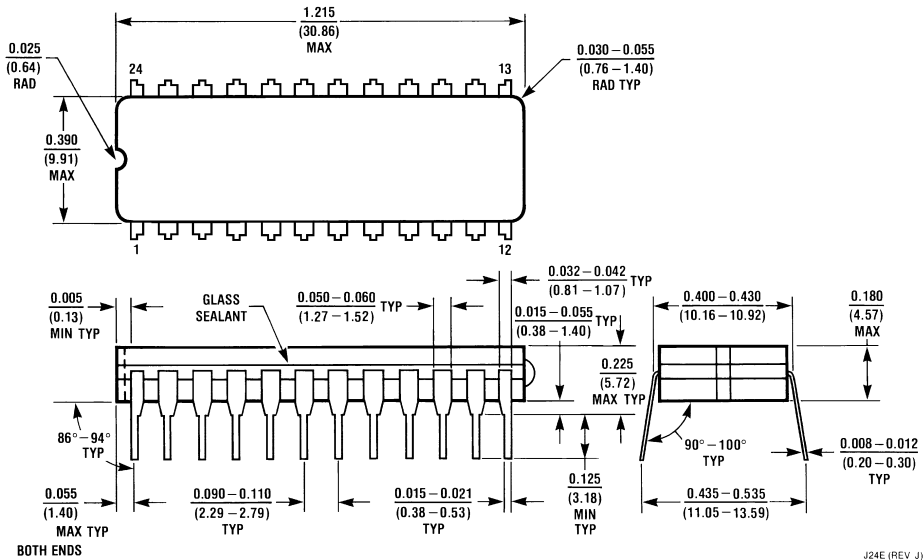


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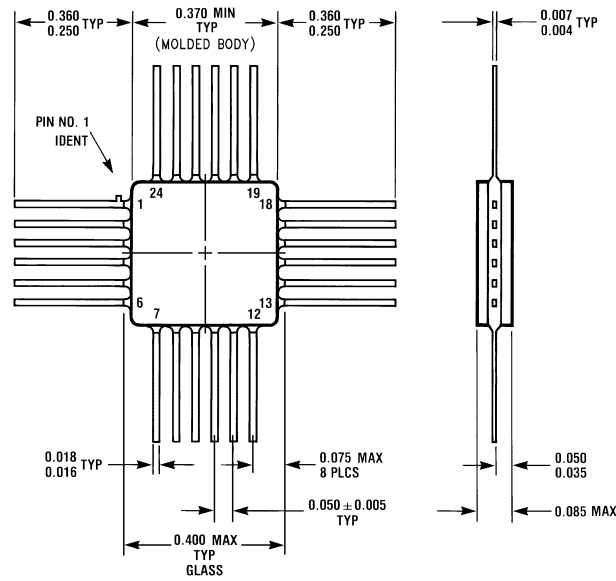
FIGURE 2. Propagation Delay and Transition Times



Physical Dimensions inches (millimeters) unless otherwise noted



24-Pin Ceramic Dual-In-Line Package (D)
NS Package Number J24E



24-Pin Quad Cerpak (F)
NS Package Number W24B

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