

# 100321 Low Power 9-Bit Inverter

## General Description

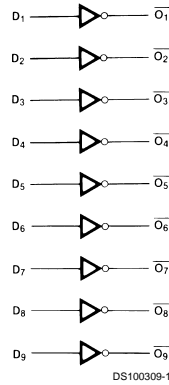
The 100321 is a monolithic 9-bit inverter. The device contains nine inverting buffer gates with single input and output. All inputs have 50 kΩ pull-down resistors.

- 2000V ESD protection
- Pin/function compatible with 100121
- Voltage compensated operating range = -4.2V to -5.7V
- Available to MIL-STD-883

## Features

- 30% power reduction of the 100121

## Logic Symbol

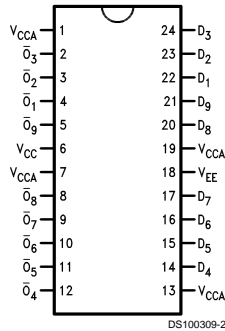


DS100309-1

Pin Names	Description
D <sub>1</sub> -D <sub>9</sub>	Data Inputs
$\bar{O}_1$ - $\bar{O}_9$	Data Outputs

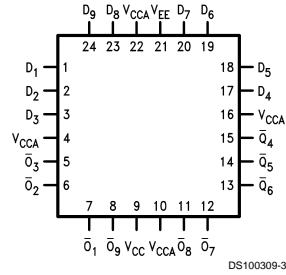
## Connection Diagrams

24-Pin DIP



DS100309-2

24-Pin Quad Cerpak



DS100309-3

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Above which the useful life may be impaired	
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Maximum Junction Temperature ( $T_J$ )	
Ceramic	+175°C
Plastic	+150°C
$V_{EE}$ Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	$V_{EE}$ to +0.5V
Output Current (DC Output HIGH)	-50 mA

ESD (Note 2)

≥2000V

## Recommended Operating Conditions

Case Temperature ( $T_C$ )	
Military	-55°C to +125°C
Supply Voltage ( $V_{EE}$ )	-5.7V to -4.2V
<b>Note 1:</b> Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.	
<b>Note 2:</b> ESD testing conforms to MIL-STD-883, Method 3015.	

## Military Version

### DC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = -55^\circ C$  to  $+125^\circ C$

Symbol	Parameter	Min	Max	Units	$T_C$	Conditions	Notes	
$V_{OH}$	Output HIGH Voltage	-1025	-870	mV	0°C to +125°C	$V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$	Loading with 50Ω to -2.0V	(Notes 3, 4, 5)
		-1085	-870	mV	-55°C			
$V_{OL}$	Output LOW Voltage	-1830	-1620	mV	0°C to +125°C	$V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$	Loading with 50Ω to -2.0V	(Notes 3, 4, 5)
		-1830	-1555	mV	-55°C			
$V_{OHC}$	Output HIGH Voltage	-1035		mV	0°C to +125°C	$V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$	Loading with 50Ω to -2.0V	(Notes 3, 4, 5)
		-1085		mV	-55°C			
$V_{OLC}$	Output LOW Voltage		-1610	mV	0°C to +125°C	$V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$	Loading with 50Ω to -2.0V	(Notes 3, 4, 5)
			-1555	mV	-55°C			
$V_{IH}$	Input HIGH Voltage	-1165	-870	mV	-55°C to +125°C	Guaranteed HIGH Signal for All Inputs	(Notes 3, 4, 5, 6)	
$V_{IL}$	Input LOW Voltage	-1830	-1475	mV	-55°C to +125°C	Guaranteed LOW Signal for All Inputs	(Notes 3, 4, 5, 6)	
$I_{IL}$	Input LOW Current	0.50		μA	-55°C to +125°C	$V_{EE} = -4.2V$ $V_{IN} = V_{IL} (Min)$	(Notes 3, 4, 5)	
$I_{IH}$	Input HIGH Current		240	μA	0°C to +125°C	$V_{EE} = -5.7V$ $V_{IN} = V_{IH} (Max)$	(Notes 3, 4, 5)	
			340	μA	-55°C			
$I_{EE}$	Power Supply Current	-70	-25	mA	-55°C to +125°C	Inputs Open	(Notes 3, 4, 5)	

**Note 3:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

**Note 4:** Screen tested 100% on each device at -55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

**Note 5:** Sample tested (Method 5005, Table I) on each manufactured lot at -55°C, +25°C and +125°C, Subgroups A1, 2, 3, 7, and 8.

**Note 6:** Guaranteed by applying specified input condition and testing  $V_{OH}/V_{OL}$ .

## AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
$t_{PLH}$	Propagation Delay	0.30	1.80	0.40	1.60	0.40	1.80	ns	Figures 1, 2	(Notes 7, 8, 9, 11)
$t_{PHL}$	Data to Output									
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.30	1.20	0.30	1.20	0.30	1.20	ns		(Note 10)

**Note 7:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals  $-55^\circ C$ ), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

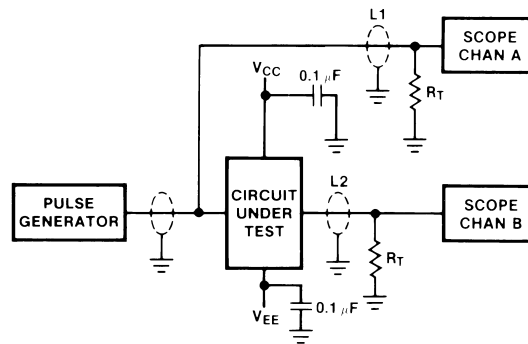
**Note 8:** Screen tested 100% on each device at  $+25^\circ C$  temperature only, Subgroup A9.

**Note 9:** Sample tested (Method 5005, Table I) on each mfg. lot at  $+25^\circ C$ , Subgroup A9, and at  $+125^\circ C$  and  $-55^\circ C$  temperatures, Subgroups A10 and A11.

**Note 10:** Not tested at  $+25^\circ C$ ,  $+125^\circ C$ , and  $-55^\circ C$  temperature (design characterization data).

**Note 11:** The propagation delay specified is for single output switching. Delays may vary up to 200 ps with multiple outputs switching.

## Test Circuitry



DS100309-5

### Notes:

$V_{CC}, V_{CCA} = +2V$ ,  $V_{EE} = -2.5V$

L1 and L2 = equal length 50Ω impedance lines

$R_T = 50\Omega$  terminator internal to scope

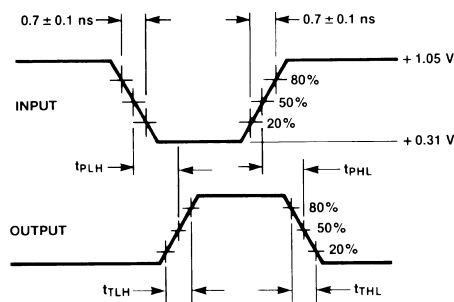
Decoupling 0.1  $\mu F$  from GND to  $V_{CC}$  and  $V_{EE}$

All unused outputs are loaded with 50Ω to GND

$C_L$  = Fixture and stray capacitance  $\leq 3$  pF

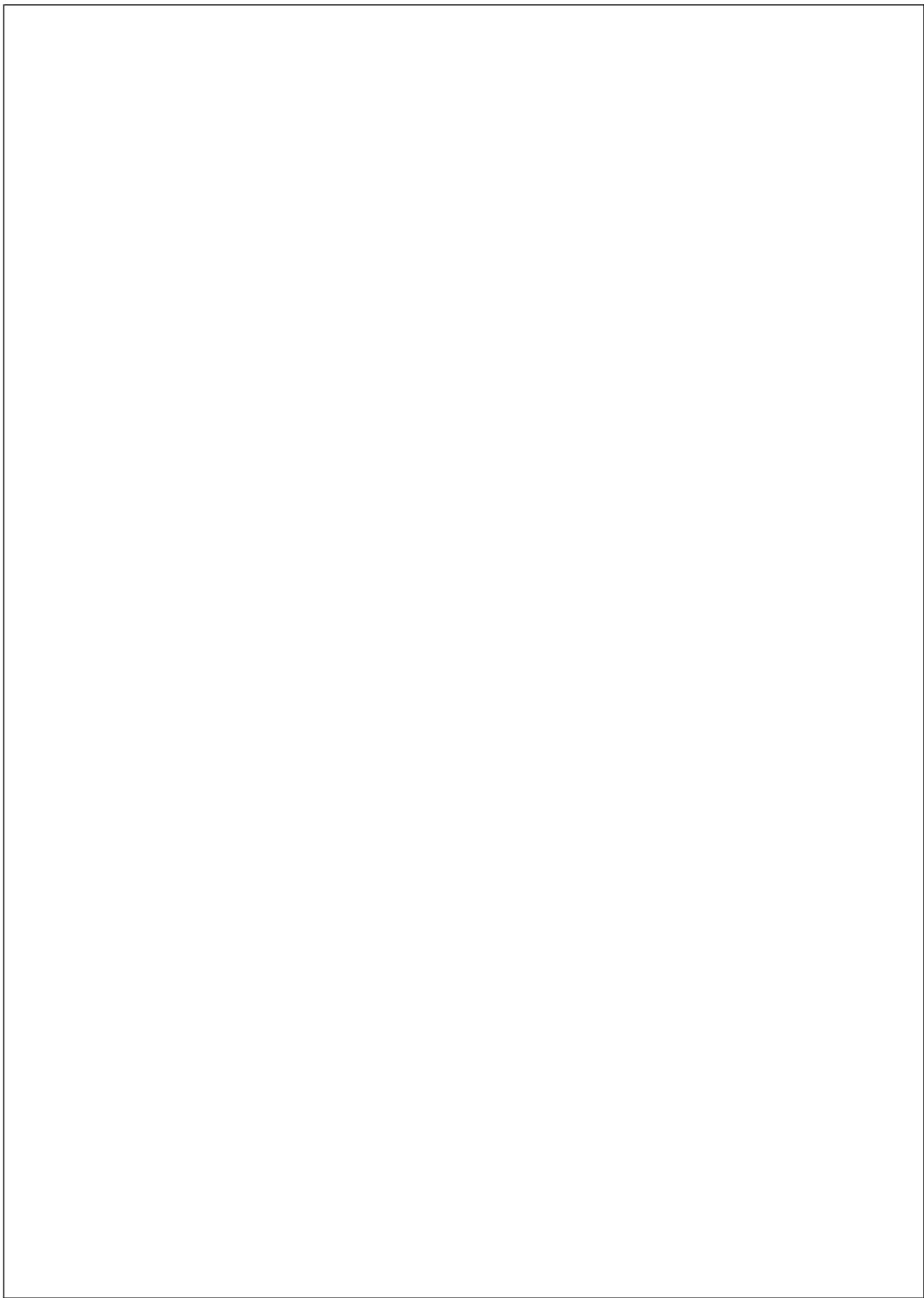
FIGURE 1. AC Test Circuit

## Switching Waveforms

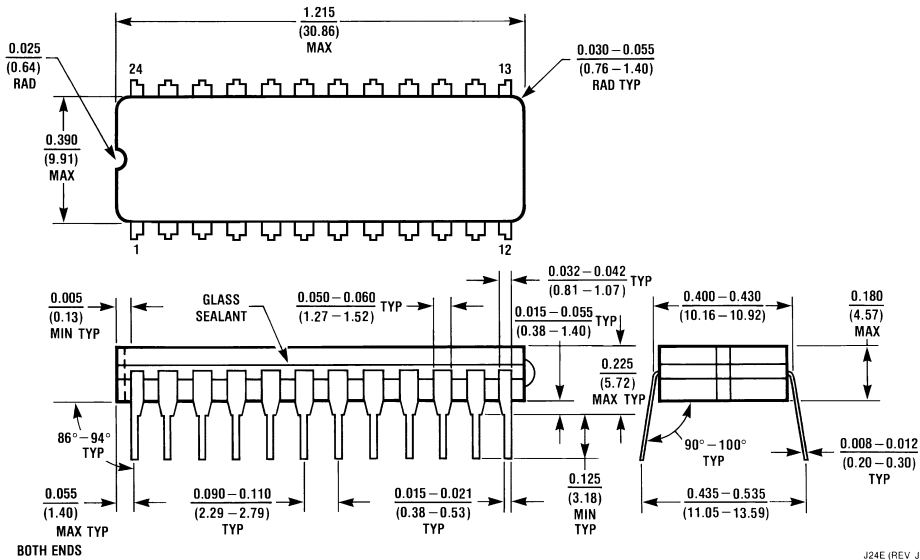


DS100309-6

FIGURE 2. Propagation Delay and Transition Times

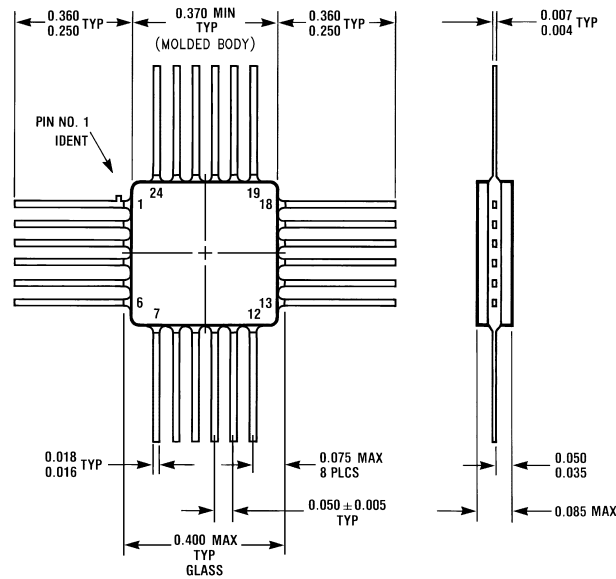


**Physical Dimensions** inches (millimeters) unless otherwise noted



J24E (REV. J)

**24-Lead Ceramic Dual-In-Line Package (D)**  
NS Package Number J24E



W24B (REV. D)

**24-Lead Quad Cerpak (F)**  
NS Package Number W24B

**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



**National Semiconductor Corporation**  
Americas  
Tel: 1-800-272-9959  
Fax: 1-800-737-7018  
Email: support@nsc.com

[www.national.com](http://www.national.com)

**National Semiconductor Europe**  
Fax: +49 (0) 1 80-530 85 86  
Email: europe.support@nsc.com  
Deutsch Tel: +49 (0) 1 80-530 85 85  
English Tel: +49 (0) 1 80-532 78 32  
Français Tel: +49 (0) 1 80-532 93 58  
Italiano Tel: +49 (0) 1 80-534 16 80

**National Semiconductor Asia Pacific Customer Response Group**  
Tel: 65-2544466  
Fax: 65-2504466  
Email: sea.support@nsc.com

**National Semiconductor Japan Ltd.**  
Tel: 81-3-5620-6175  
Fax: 81-3-5620-6179