National Semiconductor

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100324
Low Power Hex TTL-to-ECL Translator

General Description

The 100324 is a hex translator, designed to convert TTL logic levels to 100K ECL logic levels. The inputs are compatible with standard or Schottky TTL. A common Enable (E), when LOW, holds all inverting outputs HIGH and holds all true outputs LOW. The differential outputs allow each circuit to be used as an inverting/non-inverting translator, or as a differential line driver. The output levels are voltage compensated over the full −4.2V to −5.7V range.

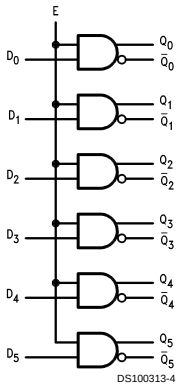
When the circuit is used in the differential mode, the 100324, due to its high common mode rejection, overcomes voltage gradients between the TTL and ECL ground systems. The V_{EE} and V_{TTL} power may be applied in either order.

The 100324 is pin and function compatible with the 100124 with similar AC performance, but features power dissipation roughly half of the 100124 to ease system cooling requirements.

Features

- Pin/function compatible with 100124
- Meets 100124 AC specifications
- 50% power reduction of the 100124
- Differential outputs
- 2000V ESD protection
- −4.2V to −5.7V operating range
- Standard Microcircuit Drawing (SMD) 5962-9153001

Logic Diagram



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Pin Names	Description
D_0–D_5	Data Inputs
E	Enable Input
Q_0–Q_5	Data Outputs
$\overline{Q}_0$–$\overline{Q}_5$	Complementary Data Outputs

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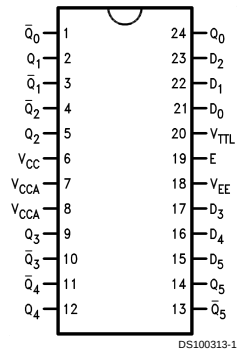
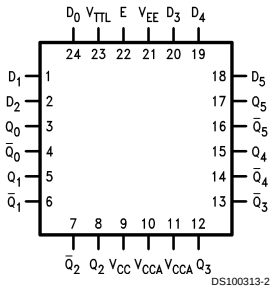
Connection Diagrams

24-Pin DIP



DS100313-1

24-Pin Quad Cerpak



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Above which the useful life may be impaired.

Storage Temperature (T_{STG})	−65˚C to +150˚C
Maximum Junction Temperature (T_J)	
Ceramic	+175˚C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
V_{TTL} Pin Potential to Ground Pin	−0.5V to +6.0V
Input Voltage (DC)	−0.5V to +6.0V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Military	−55˚C to +125˚C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Military Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55˚C to +125˚C, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0˚C to +125˚C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	(Notes 3, 4, 5)
		−1085	−870	mV	−55˚C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0˚C to +125˚C			
		−1830	−1555	mV	−55˚C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0˚C to +125˚C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	(Notes 3, 4, 5)
		−1085		mV	−55˚C			
V_{OLC}	Output LOW Voltage		−1610	mV	0˚C to +125˚C			
			−1555	mV	−55˚C			
V_{IH}	Input HIGH Voltage	2.0	5.0	V	−55˚C to +125˚C	Over V_{TTL}, V_{EE}, T_C Range		(Notes 3, 4, 5, 6)
V_{IL}	Input LOW Voltage	0.0	0.8	V	−55˚C to +125˚C	Over V_{TTL}, V_{EE}, T_C Range		(Notes 3, 4, 5, 6)
I_{IH}	Input HIGH Current		20	µA	−55˚C to +125˚C	V_{IN} = +2.7V		(Notes 3, 4, 5)
	Breakdown Test		100	µA	−55˚C to +125˚C	V_{IN} = +7.0V		
I_{IL}	Input LOW Current							
	Data	−0.9		mA	−55˚C to +125˚C	V_{IN} = +0.4V		(Notes 3, 4, 5)
	Enable	−5.4						
V_{FCD}	Input Clamp Diode Voltage		−1.2	V	−55˚C to +125˚C	I_{IN} = −18 mA		(Notes 3, 4, 5)
I_{EE}	V_{EE} Power Supply Current	−70	−22	mA	−55˚C to +125˚C	All Inputs V_{IN} = +4.0V		(Notes 3, 4, 5)
I_{TTL}	V_{TTL} Power Supply Current		38	mA	−55˚C to +125˚C	All Inputs V_{IN} = GND		(Notes 3, 4, 5)

Note 3: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55˚C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 4: Screen tested 100% on each device at −55˚C, +25˚C, and +125˚C, Subgroups 1, 2, 3, 7, and 8.

Note 5: Sample tested (Method 5005, Table I) on each manufactured lot at −55˚C, +25˚C, and +125˚C, Subgroups A1, 2, 3, 7, and 8.

Note 6: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = −55˚C		T_C = +25˚C		T_C = +125˚C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH}	Propagation Delay	0.50	3.00	0.50	2.90	0.30	3.30	ns		(Notes 7, 8, 9)
t_{PHL}	Data and Enable to Output								*Figures 1, 2*	
t_{TLH}	Transition Time	0.35	1.80	0.45	1.80	0.45	1.80	ns		(Note 10)
t_{THL}	20% to 80%, 80% to 20%									

Note 7: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55˚C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 8: Screen tested 100% on each device at +25˚C temperature only, Subgroup A9.

Note 9: Sample tested (Method 5005, Table I) on each manufactured lot at +25˚C, Subgroup A9, and at +125˚C and −55˚C temperatures, Subgroups A10 and A11.

Note 10: Not tested at +25˚C, +125˚C, and −55˚C temperature (design characterization data).

Switching Waveform

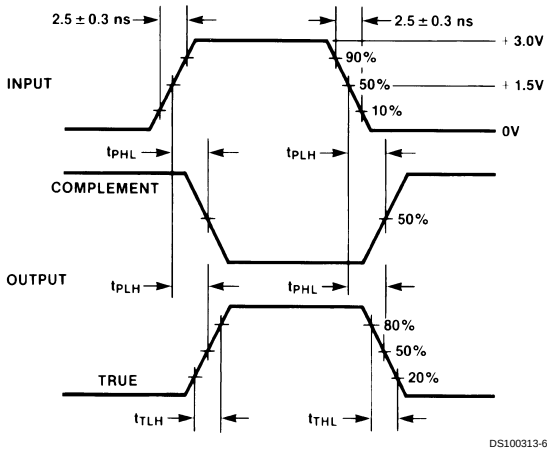
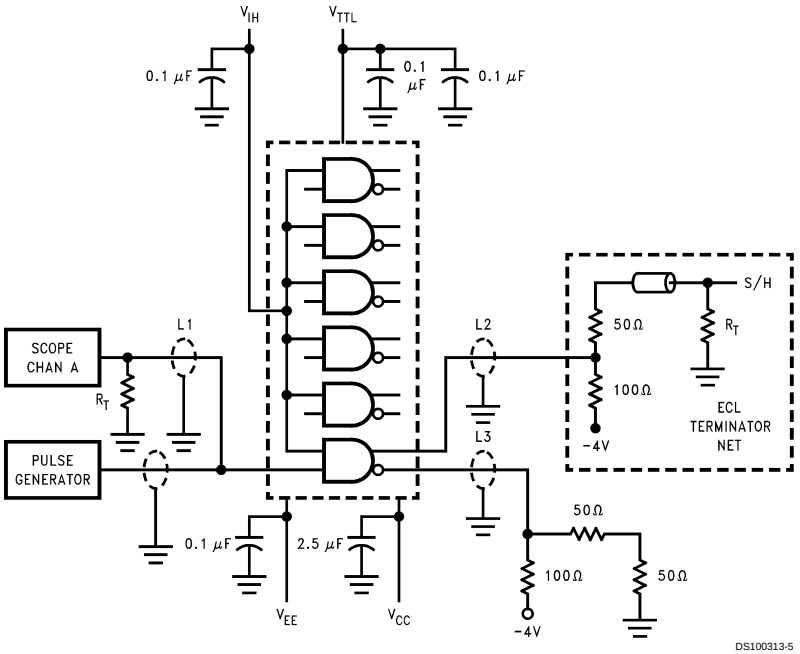


FIGURE 1. Propagation Delay and Transition Times

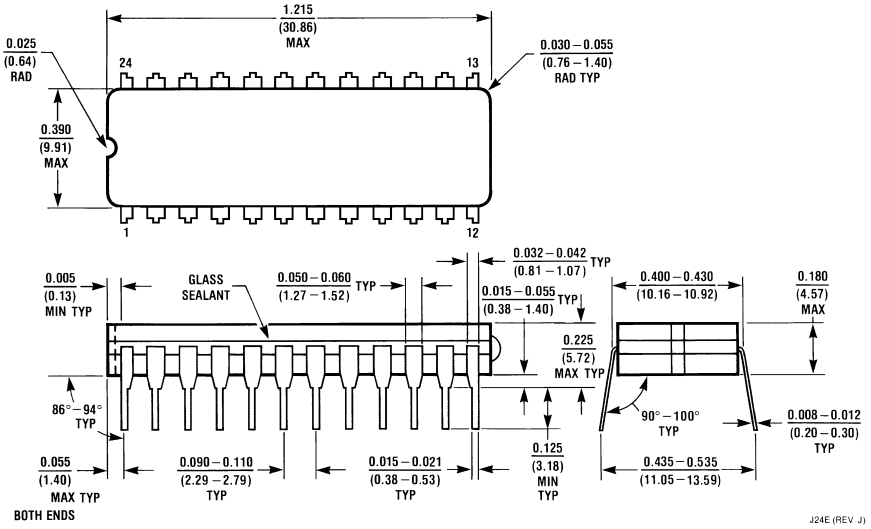
Test Circuit



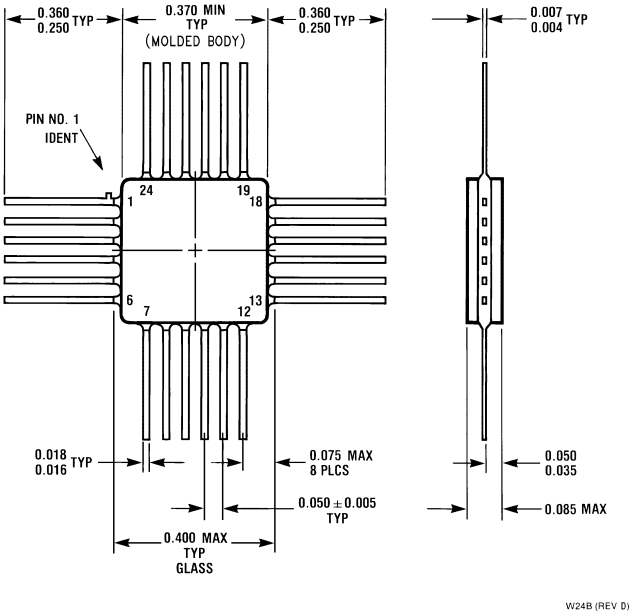
Note:
V_{CC}, V_{CCA} = 0V, V_{EE} = −4.5V, V_{TTL} = +5.0V, V_{IH} = +3.0V
L1, L2 and L3 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 µF from GND to V_{CC}, V_{EE} and V_{TTL}
All unused outputs are loaded with 50Ω to −2V or with equivalent ECL terminator network
C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 2. AC Test Circuit

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)
NS Package Number J24E



24 Lead Quad Cerpak (F)
NS Package Number W24B

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National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
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