National Semiconductor

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100329
Low Power Octal ECL/TTL Bidirectional Translator with Register

General Description

The 100329 is an octal registered bidirectional translator designed to convert TTL logic levels to 100K ECL logic levels and vice versa. The direction of the translation is determined by the DIR input. A LOW on the output enable input (OE) holds the ECL outputs in a cut-off state and the TTL outputs at a high impedance level. The outputs change synchronously with the rising edge of the clock input (CP) even though only one output is enabled at the time.

The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is −2.0V, presenting a high impedance to the data bus. This high impedance reduces the termination power and prevents loss of low state noise margin when several loads share the bus.

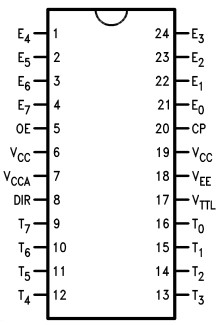
The 100329 is designed with FAST® TTL output buffers, featuring optimal DC drive and capable of quickly charging and discharging highly capacitive loads. All inputs have 50 kΩ pull-down resistors.

Features

- Bidirectional translation
- ECL high impedance outputs
- Registered outputs
- FAST TTL outputs
- TRI-STATE® outputs
- Voltage compensated operating range = −4.2V to −5.7V
- Standard Microcircuit Drawing (SMD) 5962-9206601

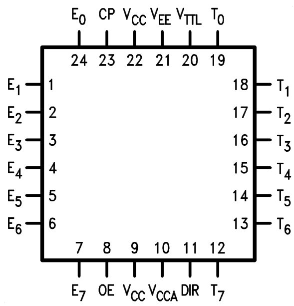
Connection Diagrams

24-Pin DIP



DS100306-2

24-Pin Quad Cerpack



DS100306-4

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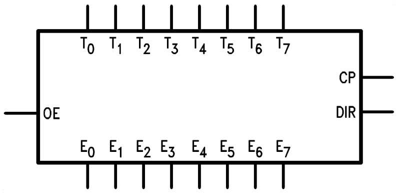
FAST® is a registered trademark of Fairchild Semiconductor.

Logic Symbol



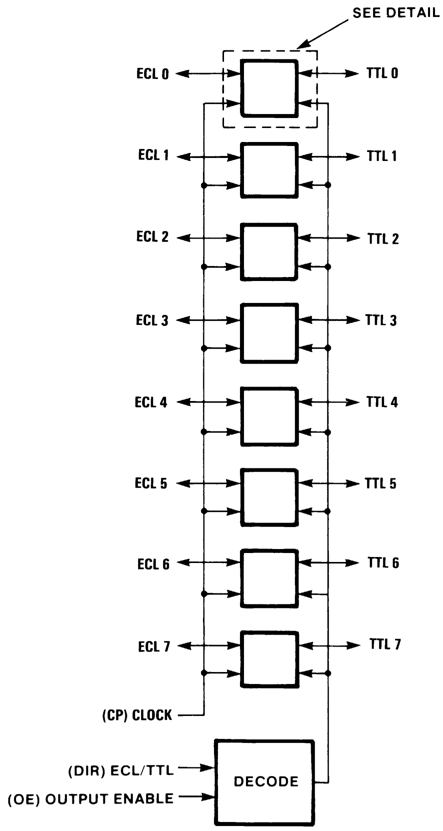
DS100306-1

Pin Descriptions

Pin Names	Description
E_0–E_7	ECL Data I/O
T_0–T_7	TTL Data I/O
OE	Output Enable Input
CP	Clock Pulse Input
	(Active Rising Edge)
DIR	Direction Control Input

All pins function at 100K ECL levels except for T_0–T_7.

Functional Diagram



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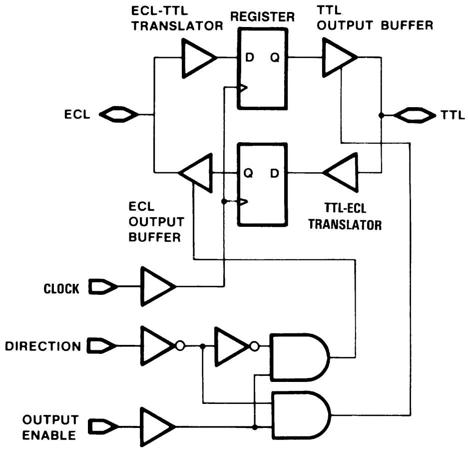
Note: DIR and OE use ECL logic levels

Detail



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OE	DIR	CP	ECL Port	TTL Port	Notes
L	L	X	Input	Z	1, 3
L	H	X	LOW (Cut-Off)	Input	2, 3
H	L	⌐	L	L	1
H	L	⌐	H	H	1
H	L	L	X	NC	1, 3
H	H	⌐	L	L	2
H	H	⌐	H	H	2
H	H	L	NC	X	2, 3

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
⌐ = LOW-to-HIGH Clock Transition
NC = No Change

Note 1: ECL input to TTL output mode.

Note 2: TTL input to ECL output mode.

Note 3: Retains data present before CP.

Absolute Maximum Ratings (Note 4)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_j)	
Ceramic	+175°C
V_{EE} Pin Potential to	
Ground Pin	−7.0V to +0.5V
V_{TTL} Pin Potential to	
Ground Pin	−0.5V to +6.0V
ECL Input Voltage (DC)	V_{EE} to +0.5V
ECL Output Current	
(DC Output HIGH)	−50 mA
TTL Input Voltage (Note 6)	−0.5V to +6.0V
TTL Input Current (Note 6)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State	
TRI-STATE Output	−0.5V to +5.5V
Current Applied to TTL	
Output in LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD (Note 5)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Military	−55°C to +125°C
ECL Supply Voltage (V_{EE})	−5.7V to −4.2V
TTL Supply Voltage (V_{TTL})	+4.5V to +5.5V

Note 4: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 5: ESD testing conforms to MIL-STD-883, Method 3015.

Note 6: Either voltage limit or current limit is sufficient to protect inputs.

Military Version TTL-to-ECL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	(Notes 7, 8, 9)
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
	Cutoff Voltage		−1950	mV	0°C to +125°C	OE or DIR Low		
			−1850	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω0 to −2.0V	(Notes 7, 8, 9)
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	2.0		V	−55°C to +125°C	Over V_{TTL}, V_{EE}, T_C Range		(Notes 7, 8, 9, 10)
V_{IL}	Input LOW Voltage		0.8	V	−55°C to +125°C	Over V_{TTL}, V_{EE}, T_C Range		(Notes 7, 8, 9, 10)
I_{IH}	Input HIGH Current		70	µA	−55°C to 125°C	V_{IN} = +2.7V		(Notes 7, 8, 9)
	Breakdown Test		1.0	mA	−55°C to +125°C	V_{IN} = +5.5V		
I_{IL}	Input LOW Current	−1.0		mA	−55°C to +125°C	V_{IN} = +0.5V		(Notes 7, 8, 9)
V_{FCD}	Input Clamp Diode Voltage	−1.2		V	−55°C to +125° C	I_{IN} = −18 mA		(Notes 7, 8, 9)
I_{EE}	V_{EE} Supply Current	−206	−70	mA	−55°C to +125°C	OE and DIR High Inputs Open V_{EE} = −4.2V to −5.7V		(Notes 7, 8, 9)

Military Version
ECL-to-TTL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55˚C to +125˚C, C_L = 50 pF, V_{TTL} = +4.5V to + 5.5V

Symbol	Parameter	Min	Max	Units	T_C	Conditions	Notes
V_{OH}	Output HIGH Voltage	2.5 2.4		mV	0˚C to +125˚C −55˚C	I_{OH} = −1 mA, V_{TTL} = 4.50V	(Notes 7, 8, 9)
V_{OL}	Output LOW Voltage		0.5	mV	−55˚C +125˚C	I_{OL} = 24 mA, V_{TTL} = 4.50V	
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55˚C +125˚C	Guaranteed HIGH Signal for All Inputs	(Notes 7, 8, 9, 10)
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55˚C to +125˚C	Guaranteed LOW Signal for All Inputs	(Notes 7, 8, 9, 10)
I_{IH}	Input HIGH Current		350 500	µA	0˚C to +125˚C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)	(Notes 7, 8, 9)
I_{IL}	Input LOW Current	0.50		µA	−55˚C to +125˚C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)	(Notes 7, 8, 9)
I_{OZHT}	TRI-STATE Current Output High		70	µA	−55˚C to +125˚C	V_{OUT} = +2.7V	(Notes 7, 8, 9)
I_{OZLT}	TRI-STATE Current Output Low	−1.0		mA	−55˚C to +125˚C	V_{OUT} = +0.5V	(Notes 7, 8, 9)
I_{OS}	Output Short-Circuit CURRENT	−60	−150	mA	−55˚C to +125˚C	V_{OUT} = 0.0V, V_{TTL} = +5.5V	(Notes 7, 8, 9)
I_{TTL}	V_{TTL} Supply Current		70 47 70	mA mA mA	−55˚C to +125˚C	TTL Outputs Low TTL Output High TTL Output in TRI-STATE	(Notes 7, 8, 9)

Note 7: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55˚C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 8: Screen tested 100% on each device at −55˚C, +25˚C, and +125˚C, Subgroups, 1, 2 3, 7, and 8.

Note 9: Sample tested (Method 5005, Table I) on each manufactured lot at −55˚C, +25˚C, and +125˚C, Subgroups A1, 2, 3, 7, and 8.

Note 10: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version
TTL-to-ECL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55˚C		T_C = 25˚C		T_C = +125˚C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	CP to E_n	1.3	3.8	1.6	3.7	1.9	4.3	ns ns	*Figures 1, 2*	(Notes 11, 12, 13)
t_{PZH}	OE to E_n (Cutoff to HIGH)	1.0	4.3	1.5	4.4	1.7	9.0	ns	*Figures 1, 2*	(Notes 11, 12, 13)
t_{PHZ}	OE to E_n (HIGH to Cutoff)	1.5	5.0	1.6	4.5	1.6	5.0	ns	*Figures 1, 2*	
t_{PHZ}	DIR to E_n (HIGH to Cutoff)	1.6	4.7	1.6	4.3	1.7	4.7	ns	*Figures 1, 2*	
t_{set}	T_n to CP	2.5		2.0		2.5		ns	*Figures 1, 2*	(Note 14)
t_{hold}	T_n to CP	2.5		2.0		2.5		ns	*Figures 1, 2*	
t_{pw}(H)	Pulse Width CP	2.5		2.0		2.5		ns	*Figures 1, 2*	(Note 14)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.4	2.3	0.5	2.1	0.4	2.4	ns	*Figures 1, 2*	(Note 14)
f_{MAX}	CP	250		250		250		MHz		

Military Version
ECL-to-TTL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND, C_L = 50 pF

Symbol	Parameter	T_C = −55˚C		T_C = 25˚C		T_C = +125˚C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	CP to T_n	3.1	8.0	3.1	7.3	3.3	8.0	ns	*Figures 1, 2*	(Notes 11, 12, 13)
t_{PZH}	OE to T_n	3.4	9.1	3.7	9.0	4.0	10.1	ns	*Figures 3, 4*	(Notes 11, 12, 13)
t_{PZL}	(Enable Time)	3.7	9.5	4.0	9.3	4.3	10.4			
t_{PHZ}	OE to T_n	3.2	10.0	3.3	9.0	3.5	9.3	ns	*Figures 3, 5*	
t_{PLZ}	(Disable Time)	3.0	9.8	3.4	8.8	4.1	10.4			
t_{PHZ}	DIR to T_n	2.6	9.5	2.8	8.8	3.0	9.0	ns	*Figures 3, 6*	
t_{PLZ}	(Disable Time)	2.7	8.7	3.1	8.0	4.0	9.6			
t_{set}	E_n to CP	2.5		2.0		2.5		ns	*Figures 3, 4*	(Note 14)
t_{hold}	E_n to CP	3.0		2.5		3.0		ns	*Figures 3, 4*	
t_{pw}(H)	Pulse Width CP	2.5		2.5		5.0		ns	*Figures 3, 4*	(Note 14)
f_{MAX}	CP	200		200		100		MHz		

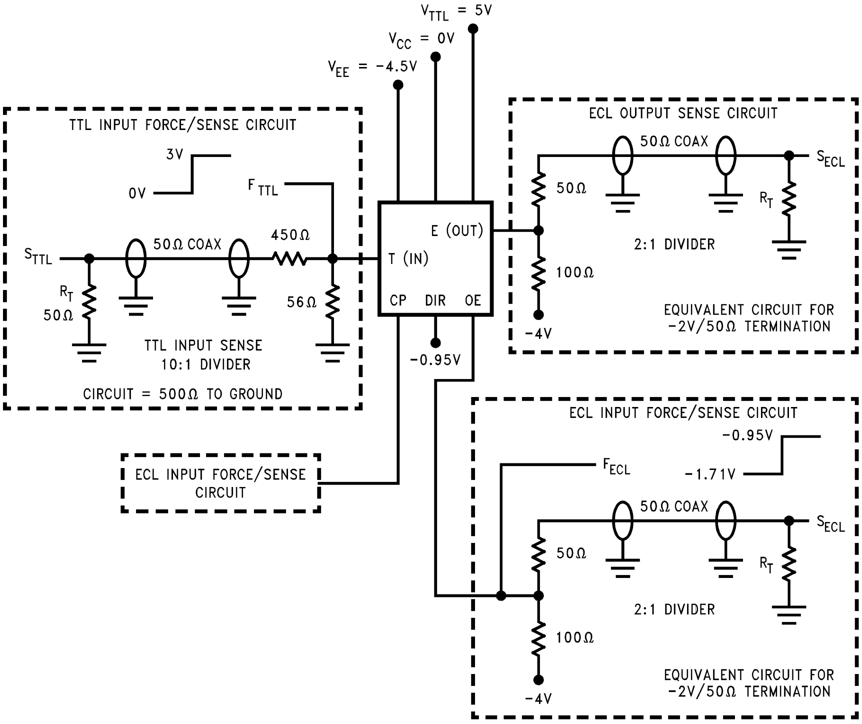
Note 11: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55˚C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 12: Screen tested 100% on each device at +25˚C, temperature only, Subgroup A9.

Note 13: Sample tested (Method 5005, Table I) on each mfg. lot at +25˚C, Subgroup A9, and at +125˚C and −55˚C temperatures, Subgroups A10 and A11.

Note 14: Not tested at +25˚C, +125˚C and −55˚C temperature (design characterization data).

Test Circuitry (TTL-to-ECL)



Note 15: R_T = 50Ω termination resistive load. When an input or output is being monitored by a scope, R_T is supplied by the scope's 50Ω input resistance. When an input or output is not being monitored, an external 50Ω resistance must be applied to serve as R_T.

Note 16: TTL and ECL force signals are brought to the DUT via 50Ω coax lines.

Note 17: V_{TTL} is decoupled to ground with 0.1 µF, V_{EE} is decoupled to ground with 0.01 µF and V_{CC} is connected to ground.

FIGURE 1. TTL-to-ECL AC Test Circuit

Switching Waveforms (TTL-to-ECL)

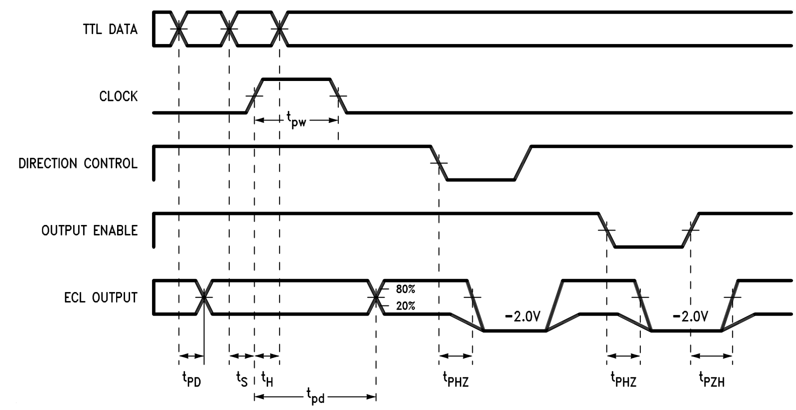
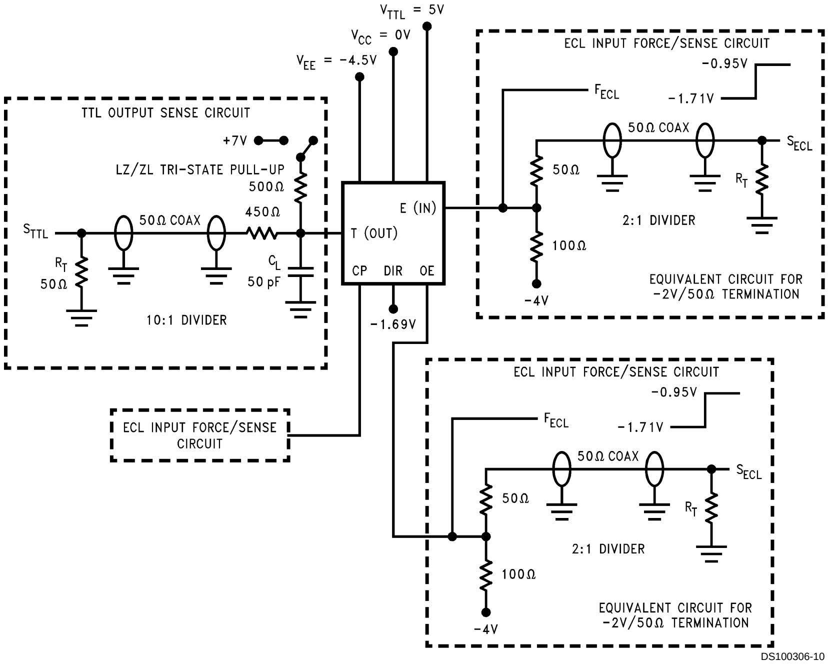


FIGURE 2. TTL to ECL Transition — Propagation Delay and Transition Times

Test Circuitry (ECL-to-TTL)



Note 18: R_T = 50Ω termination resistive load. When an input or output is being monitored by a scope, $R_T$is supplied by the scope's 50Ω input resistance. When an input or output is not being monitored, an external 50Ω resistance must be applied to serve as R_T.

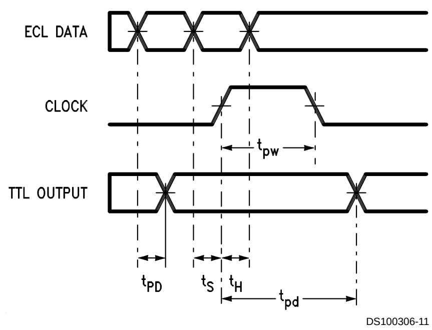
Note 19: The TTL TRI-STATE pull-up switch is connected to +7V only for ZL and LZ tests.

Note 20: TTL and ECL force signals are brought to the DUT via 50Ω coax lines.

Note 21: V_{TTL} is decoupled to ground with 0.1 µF, V_{EE} is decoupled to ground with 0.01 µF and V_{CC} is connected to ground.

FIGURE 3. ECL-to-TTL AC Test Circuit

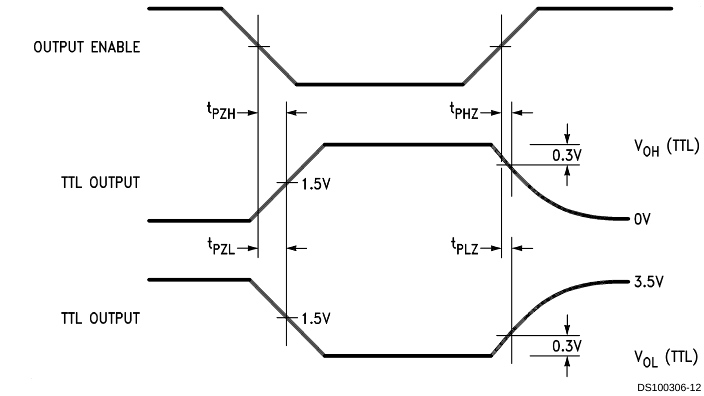
Switching Waveforms (ECL-to-TTL)



Note: DIR is LOW, OE is HIGH

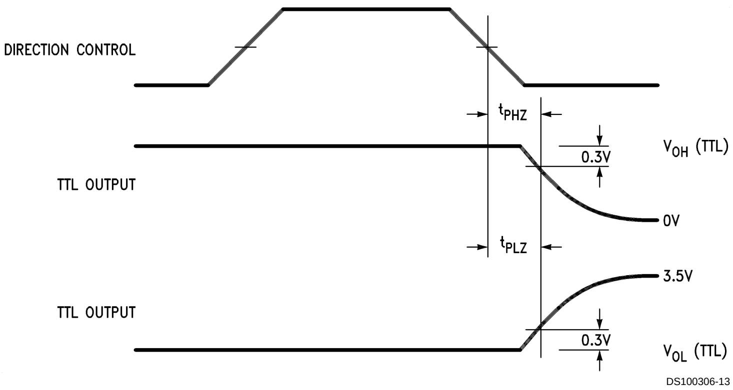
FIGURE 4. ECL-to-TTL Transition — Propagation Delay and Transition Times

Switching Waveforms (ECL-to-TTL) (Continued)



Note: DIR is LOW

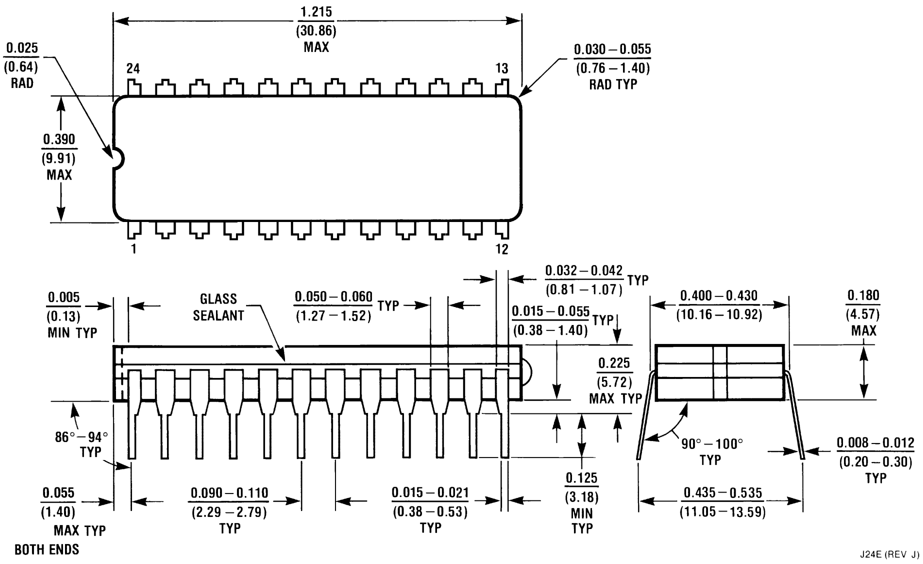
FIGURE 5. ECL-to-TTL Transition, OE to TTL Output, Enable and Disable Times



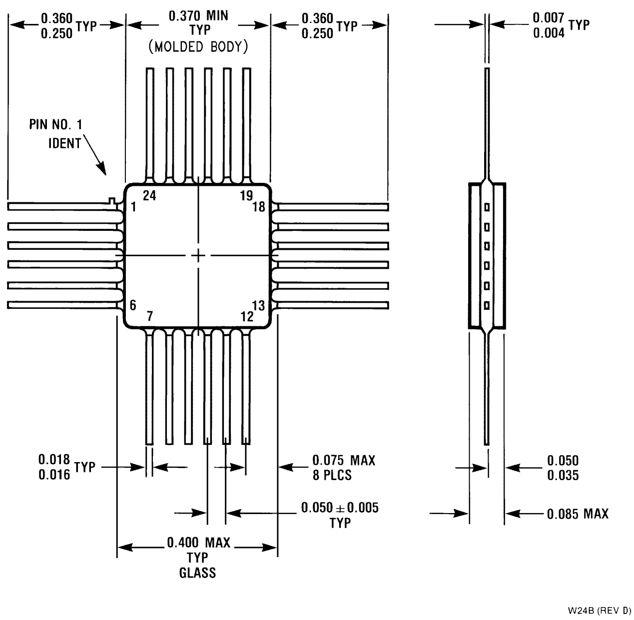
Note: OE is HIGH

FIGURE 6. ECL-to-TTL Transition, DIR to TTL Output, Disable Time

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)
Package Number J24E



24-Lead Quad Cerpak (F)
Package Number W24B

Notes

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