

## 100344 Low Power 8-Bit Latch with Cut-Off Drivers

### General Description

The 100344 contains eight D-type latches, individual inputs ( $D_n$ ), outputs ( $Q_n$ ), a common enable pin ( $\bar{E}$ ), latch enable ( $\bar{LE}$ ), and output enable pin ( $\bar{OEN}$ ). A Q output follows its D input when both  $\bar{E}$  and  $\bar{LE}$  are LOW. When either  $\bar{E}$  or  $\bar{LE}$  (or both) are HIGH, a latch stores the last valid data present on its D input prior to  $\bar{E}$  or  $\bar{LE}$  going HIGH.

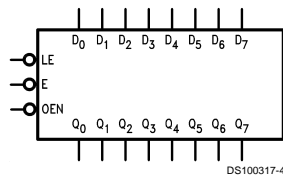
A HIGH on  $\bar{OEN}$  holds the outputs in a cut-off state. The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is  $-2.0V$ , presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

The 100344 outputs are designed to drive a doubly terminated  $50\Omega$  transmission line ( $25\Omega$  load impedance). All inputs have  $50\text{ k}\Omega$  pull-down resistors.

### Features

- Cut-off drivers
- Drives  $25\Omega$  load
- Low power operation
- 2000V ESD protection
- Voltage compensated operating range =  $-4.2V$  to  $-5.7V$
- Available to MIL-STD-883

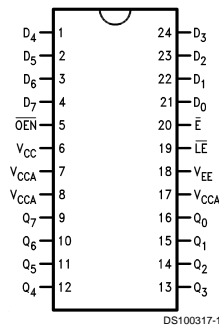
### Logic Symbol



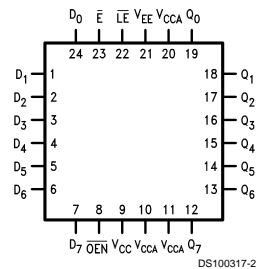
Pin Names	Description
$D_0$ - $D_7$	Data Inputs
$\bar{E}$	Enable Input
$\bar{LE}$	Latch Enable Input
$\bar{OEN}$	Output Enable Input
$Q_0$ - $Q_7$	Data Outputs

### Connection Diagrams

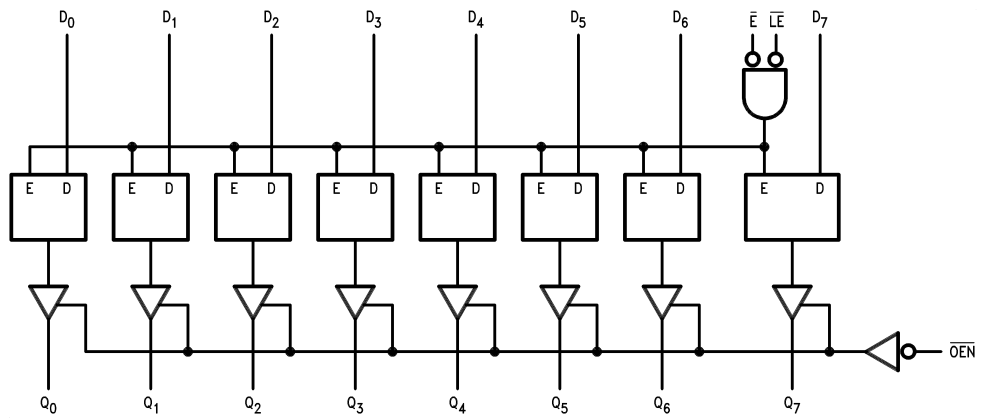
24-Pin DIP



24-Pin Quad Cerpak



## Logic Diagram



DS100317-5

## Truth Table

Inputs				Outputs
D <sub>n</sub>	$\bar{E}$	$\bar{LE}$	$\bar{OEN}$	Q <sub>n</sub>
L	L	L	L	L
H	L	L	L	H
X	H	X	L	Latched (Note 1)
X	X	H	L	Latched (Note 1)
X	X	X	H	Cutoff

H = HIGH Voltage level  
 L = LOW Voltage level  
 Cutoff = lower-than-LOW state  
 X = Don't Care

**Note 1:** Retains data present before either  $\bar{LE}$  or  $\bar{E}$  go HIGH.

## Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Above which the useful life may be impaired

Storage Temperature (T <sub>STG</sub> )	-65°C to +150°C
Maximum Junction Temperature (T <sub>J</sub> )	
Ceramic	+175°C
V <sub>EE</sub> Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	V <sub>EE</sub> to +0.5V
Output Current (DC Output HIGH)	-100 mA

ESD (Note 3)

≥2000V

## Recommended Operating Conditions

Case Temperature (T<sub>C</sub>)

Military

-55°C to +125°C

Supply Voltage (V<sub>EE</sub>)

-5.7V to -4.2V

**Note 2:** Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 3:** ESD testing conforms to MIL-STD-883, Method 3015.

## Military Version

### DC Electrical Characteristics

V<sub>EE</sub> = -4.2V to -5.7V, V<sub>CC</sub> = V<sub>CCA</sub> = GND, T<sub>C</sub> = -55°C to +125°C

Symbol	Parameter	Min	Max	Units	T <sub>C</sub>	Conditions	Notes	
V <sub>OH</sub>	Output HIGH Voltage	-1025	-870	mV	0°C to +125°C	V <sub>IN</sub> = V <sub>IH</sub> (Max) or V <sub>IL</sub> (Min)	Loading with 25Ω to -2.0V	(Notes 4, 5, 6)
		-1085	-870	mV	-55°C			
V <sub>OL</sub>	Output LOW Voltage	-1830	-1620	mV	0°C to +125°C	V <sub>IN</sub> = V <sub>IH</sub> (Min) or V <sub>IL</sub> (Max)	Loading with 25Ω to -2.0V	(Notes 4, 5, 6)
		-1830	-1555	mV	-55°C			
V <sub>OHC</sub>	Output HIGH Voltage	-1035		mV	0°C to +125°C	V <sub>IN</sub> = V <sub>IH</sub> (Min) or V <sub>IL</sub> (Max)	Loading with 25Ω to -2.0V	(Notes 4, 5, 6)
		-1085		mV	-55°C			
V <sub>OLC</sub>	Output LOW Voltage		-1610	mV	0°C to +125°C	V <sub>IN</sub> = V <sub>IH</sub> (Min) or V <sub>IL</sub> (Max)	Loading with 25Ω to -2.0V	(Notes 4, 5, 6)
			-1555	mV	-55°C			
V <sub>OLZ</sub>	Cutoff LOW Voltage		-1950	mV	0°C to +125°C	V <sub>IN</sub> = V <sub>IH</sub> (Min) or V <sub>IL</sub> (Max)	$\overline{\text{OEN}} = \text{HIGH}$	(Notes 4, 5, 6)
			-1850	mV	-55°C			
V <sub>IH</sub>	Input HIGH Voltage	-1165	-870	mV	-55°C to +125°C	Guaranteed HIGH Signal for All Inputs	(Notes 4, 5, 6, 7)	
V <sub>IL</sub>	Input LOW Voltage	-1830	-1475	mV	-55°C to +125°C	Guaranteed LOW Signal for All Inputs	(Notes 4, 5, 6, 7)	
I <sub>IL</sub>	Input LOW Current	0.50		μA	-55°C to +125°C	V <sub>EE</sub> = -4.2V V <sub>IN</sub> = V <sub>IL</sub> (Min)	(Notes 4, 5, 6, 7)	
I <sub>IH</sub>	Input HIGH Current		240	μA	0°C to +125°C	V <sub>EE</sub> = -5.7V V <sub>IN</sub> = V <sub>IH</sub> (Max)	(Notes 4, 5, 6)	
			340	μA	-55°C			
I <sub>EE</sub>	Power Supply Current	-195	-73	mA	-55°C to +125°C	Inputs Open V <sub>EE</sub> = -4.2V to -4.8V V <sub>EE</sub> = -4.2V to -5.7V	(Notes 4, 5, 6)	
		-205	-73					

**Note 4:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

**Note 5:** Screen tested 100% on each device at -55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

**Note 6:** Sample tested (Method 5005, Table I) on each manufactured lot at -55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

**Note 7:** Guaranteed by applying specified input condition and testing V<sub>OH</sub>/V<sub>OL</sub>.

## AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
$t_{PLH}$ $t_{PHL}$	Propagation Delay $D_n$ to Output	0.50	2.60	0.70	2.60	0.70	3.10	ns	Figures 1, 2	(Notes 8, 9, 10, 12)
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\overline{LE}$ , $\overline{E}$ to Output	0.80	3.30	1.00	3.30	1.10	3.80	ns	Figures 1, 4	(Notes 8, 9, 10, 12)
$t_{PZH}$ $t_{PHZ}$	Propagation Delay $\overline{OEN}$ to Output	1.00	4.60	1.10	4.20	1.20	4.40	ns	Figures 1, 2	(Notes 8, 9, 10, 12)
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.40	2.50	0.40	2.40	0.40	2.70	ns	Figures 1, 3	(Note 11)
$t_s$	Setup Time $D_0-D_7$	1.50		1.50		1.70		ns	Figures 1, 3	(Note 11)
$t_h$	Hold Time $D_0-D_7$	0.60		0.60		0.60		ns	Figures 1, 3	(Note 11)
$t_{pw(H)}$	Pulse Width HIGH $\overline{LE}$ , $\overline{E}$	2.40		2.40		2.40		ns	Figures 1, 3	(Note 11)

**Note 8:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals  $-55^\circ C$ ), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

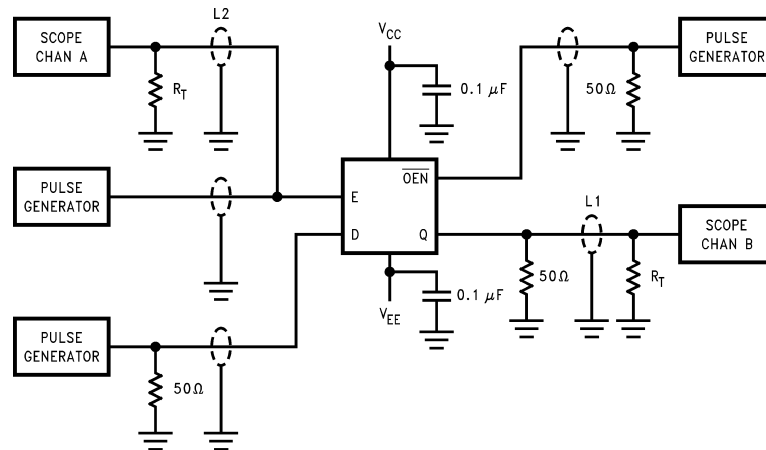
**Note 9:** Screen tested 100% on each device at  $+25^\circ C$  temperature only, Subgroup A9.

**Note 10:** Sample tested (Method 5005, Table I) on each manufactured lot at  $+25^\circ C$ , Subgroup A9, and at  $+125^\circ C$  and  $-55^\circ C$  temperatures, Subgroups A10 and A11.

**Note 11:** Not tested at  $+25^\circ C$ ,  $+125^\circ C$ , and  $-55^\circ C$  temperature (design characterization data).

**Note 12:** The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

## Test Circuitry



DS100317-6

### Notes:

$V_{CC}, V_{CCA} = +2V$ ,  $V_{EE} = -2.5V$

L1 and L2 = equal length  $50\Omega$  impedance lines

$R_T = 50\Omega$  terminator internal to scope

Decoupling  $0.1 \mu F$  from GND to  $V_{CC}$  and  $V_{EE}$

All unused outputs are loaded with  $25\Omega$  to GND

$C_L$  = Fixture and stray capacitance  $\leq 3$  pF

FIGURE 1. AC Test Circuit

## Switching Waveforms

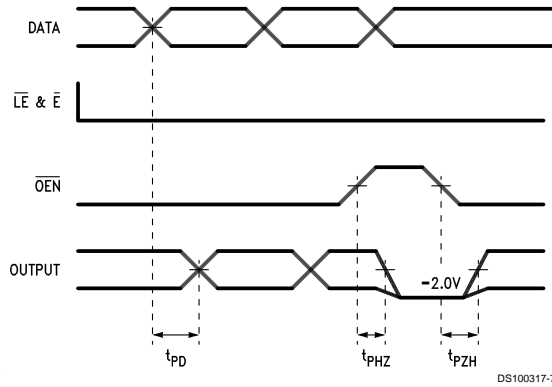


FIGURE 2. Propagation Delay and Cutoff Times

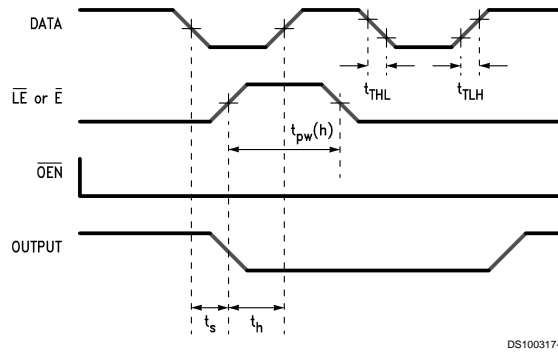


FIGURE 3. Setup, Hold and Pulse Width Times

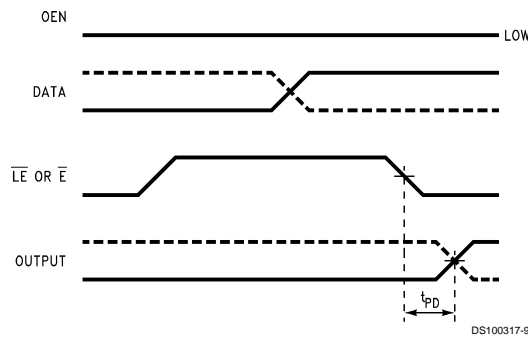
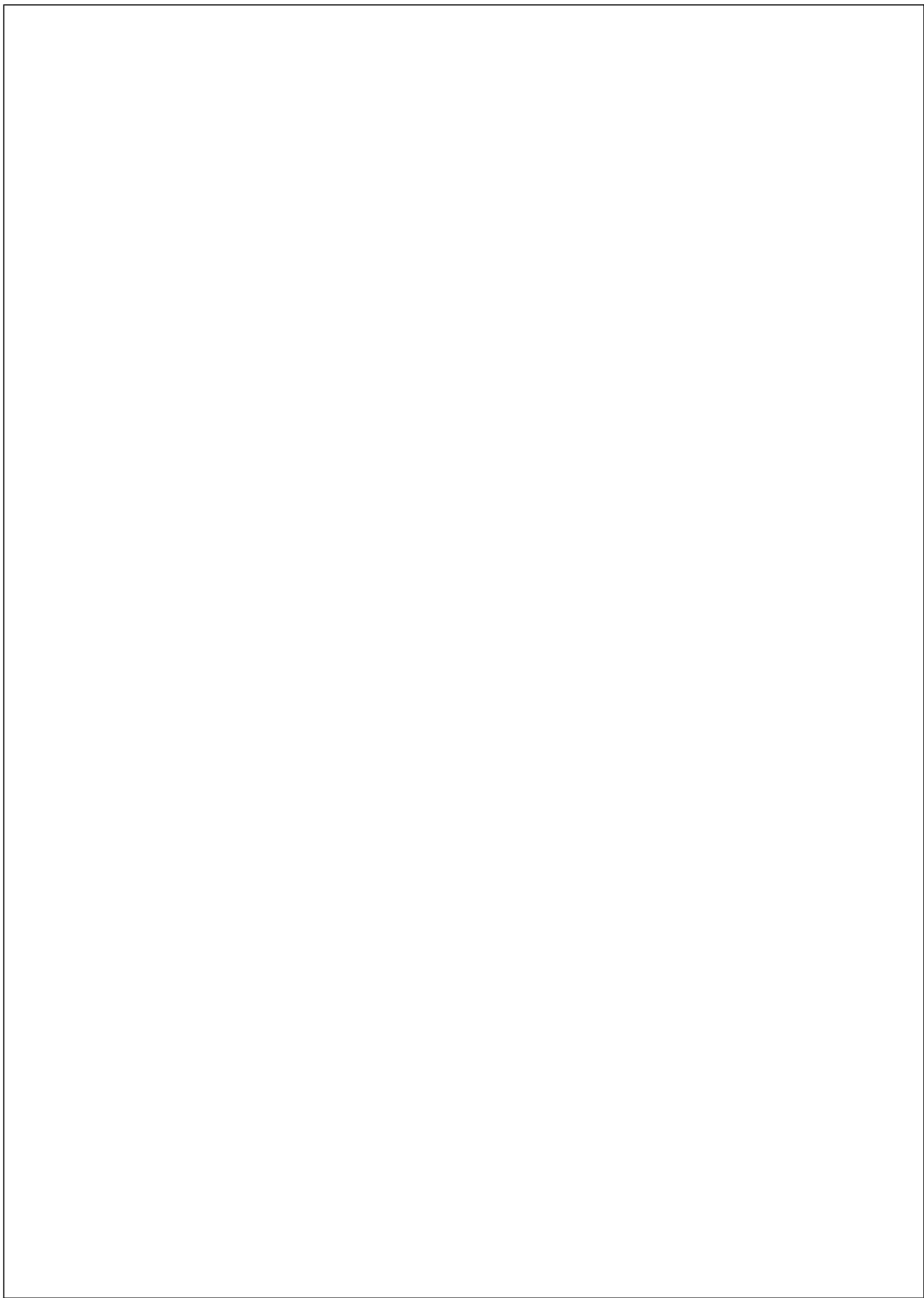
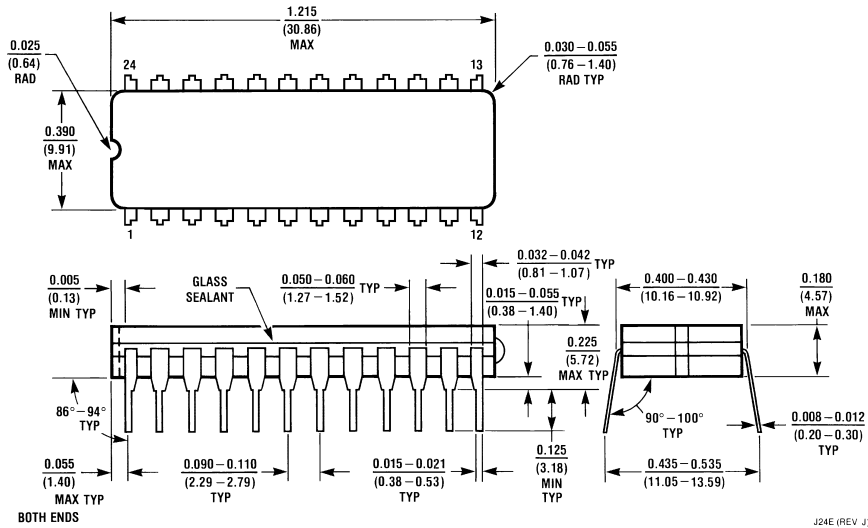


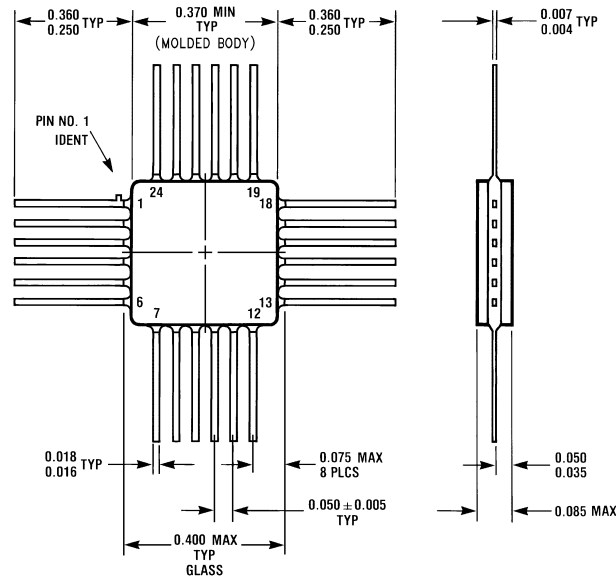
FIGURE 4. Propagation Delay  $\overline{LE}$ ,  $\overline{E}$  to Q



**Physical Dimensions** inches (millimeters) unless otherwise noted



**24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)**  
NS Package Number J24E



**24-Lead Quad Cerpak (F)**  
NS Package Number W24B

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**National Semiconductor Corporation**  
Americas  
Tel: 1-800-272-9959  
Fax: 1-800-737-7018  
Email: support@nsc.com

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**National Semiconductor Europe**  
Fax: +49 (0) 1 80-530 85 86  
Email: europe.support@nsc.com  
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