

## 54ABT240

### Octal Buffer/Line Driver with TRI-STATE® Outputs

#### General Description

The 'ABT240 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Standard Microcircuit Drawing (SMD) — 5962-9318801

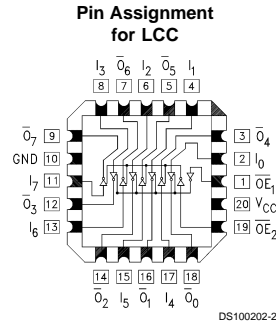
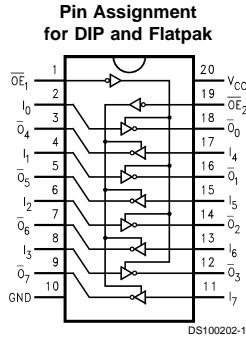
#### Features

- Output sink capability of 48 mA, source capability of 24 mA

#### Ordering Code

Military	Package Number	Package Description
54ABT240J-QML	J20A	20-Lead Ceramic Dual-In-Line
54ABT240W-QML	W20A	20-Lead Cerpack
54ABT240E-QML	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

#### Connection Diagrams



Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	TRI-STATE Output Enable Inputs
$I_0-I_7$	Inputs
$\overline{O}_0-\overline{O}_7$	Outputs

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

## Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	$I_n$	
L	L	H
L	H	L
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	$I_n$	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	
Ceramic	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	-0.5V to 5.5V
in the HIGH State	-0.5V to V <sub>CC</sub>

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
DC Latchup Source Current (Across Comm Operating Range)	-150 mA
Over Voltage Latchup (I/O)	10V

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

Symbol	Parameter	ABT240			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54ABT	2.5		V	Min	I <sub>OH</sub> = -3 mA
		54ABT	2.0		V	Min	I <sub>OH</sub> = -24 mA
V <sub>OL</sub>	Output LOW Voltage	54ABT		0.55	V	Min	I <sub>OL</sub> = 48 mA
I <sub>IH</sub>	Input HIGH Current		5		μA	Max	V <sub>IN</sub> = 2.7V (Note 4)
				5			V <sub>IN</sub> = V <sub>CC</sub>
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>IL</sub>	Input LOW Current			-5	μA	Max	V <sub>IN</sub> = 0.5V (Note 4)
				-5			V <sub>IN</sub> = 0.0V
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OZH</sub>	Output Leakage Current			50	μA	0 - 5.5V	V <sub>OUT</sub> = 2.7V; $\overline{OE}_n$ = 2.0V
I <sub>OZL</sub>	Output Leakage Current			-50	μA	0 - 5.5V	V <sub>OUT</sub> = 0.5V; $\overline{OE}_n$ = 2.0V
I <sub>OS</sub>	Output Short-Circuit Current	-100		-275	mA	Max	V <sub>OUT</sub> = 0.0V
I <sub>CEX</sub>	Output High Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>ZZ</sub>	Bus Drainage Test			100	μA	0.0	V <sub>OUT</sub> = 5.5V; All Others GND
I <sub>CCH</sub>	Power Supply Current			50	μA	Max	All Outputs HIGH
I <sub>CCL</sub>	Power Supply Current			30	mA	Max	All Outputs LOW
I <sub>CCZ</sub>	Power Supply Current			50	μA	Max	$\overline{OE}_n$ = V <sub>CC</sub> ; All Others at V <sub>CC</sub> or Ground
I <sub>CC1</sub>	Additional I <sub>CC</sub> /Input	Outputs Enabled		1.5	mA	Max	V <sub>I</sub> = V <sub>CC</sub> - 2.1V
		Outputs TRI-STATE		1.5	mA		Enable Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V
		Outputs TRI-STATE		50	μA		Data Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V All Others at V <sub>CC</sub> or Ground
I <sub>CCD</sub>	Dynamic I <sub>CC</sub> (Note 4)	No Load		0.1	mA/ MHz	Max	Outputs Open $\overline{OE}_n$ = GND, (Note 3) One Bit Toggling, 50% Duty Cycle

**Note 3:** For 8 bits toggling, I<sub>CCD</sub> < 0.8 mA/MHz.

**Note 4:** Guaranteed, but not tested.

## AC Electrical Characteristics

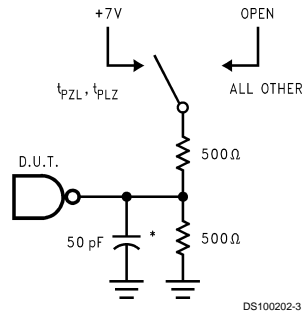
Symbol	Parameter	54ABT		Units	Fig. No.
		T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> = 4.5V-5.5V C <sub>L</sub> = 50 pF			
		Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Data to Outputs	0.8 1.0	5.5 5.5	ns	Figure 5
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time	0.8 0.8	7.5 7.7	ns	Figure 4
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time	1.0 1.0	7.5 7.2	ns	Figure 4

## Capacitance

Symbol	Parameter	Typ	Units	Conditions T <sub>A</sub> = 25°C
C <sub>IN</sub>	Input Capacitance	5.0	pF	V <sub>CC</sub> = 0V
C <sub>OUT</sub> (Note 5)	Output Capacitance	9.0	pF	V <sub>CC</sub> = 5.0V

Note 5: C<sub>OUT</sub> is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

## AC Loading



\*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

Amplitude	Rep. Rate	t <sub>w</sub>	t <sub>r</sub>	t <sub>f</sub>
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

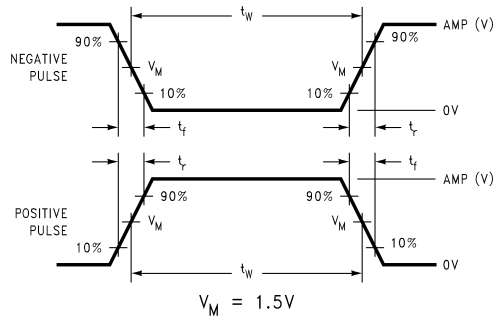
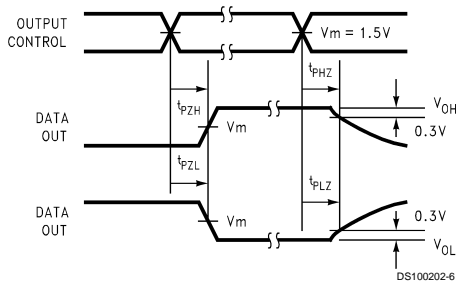
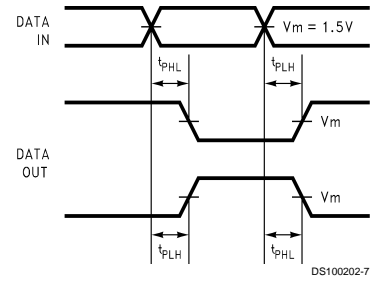


FIGURE 2. Test Input Signal Levels

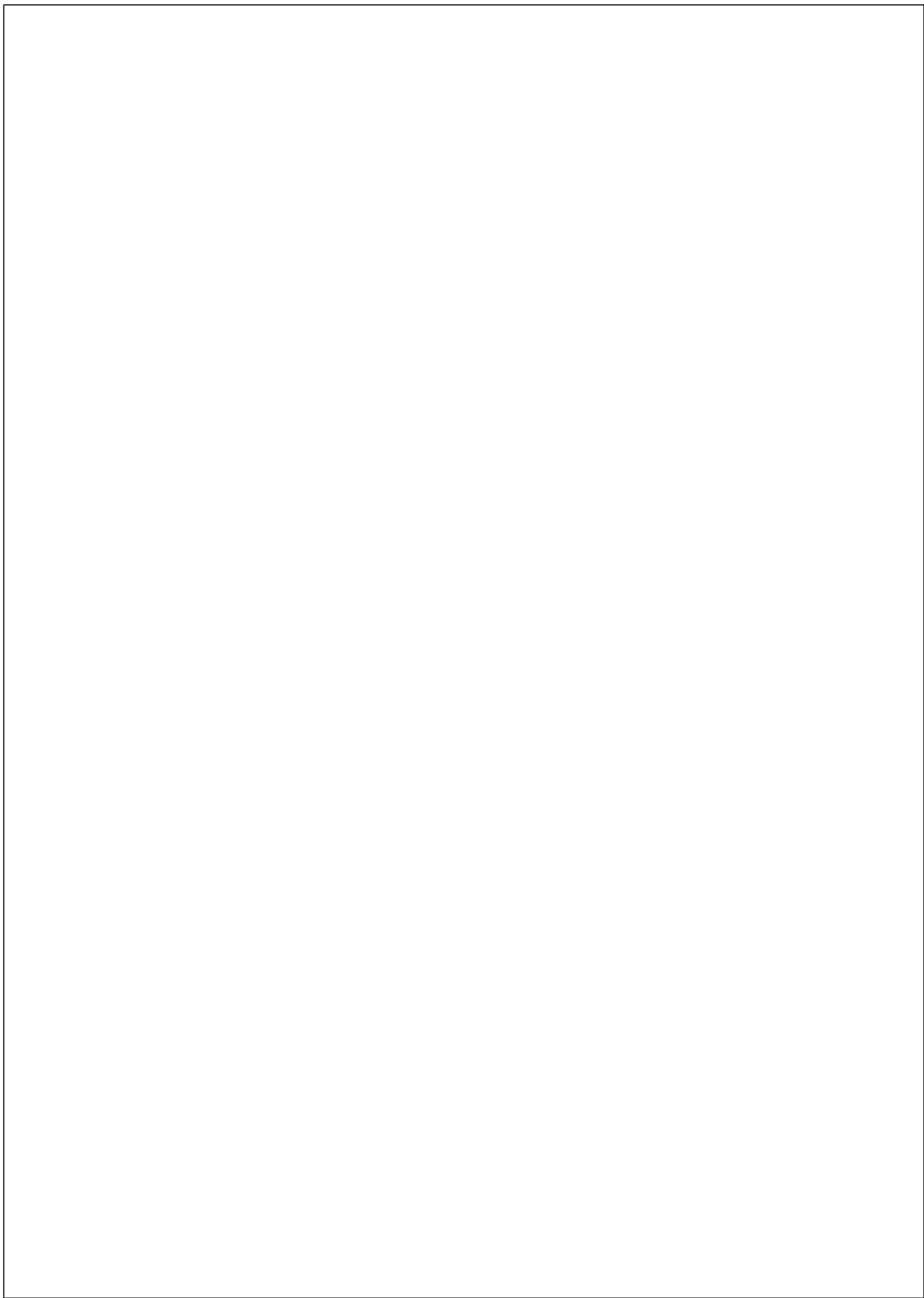
## AC Waveforms



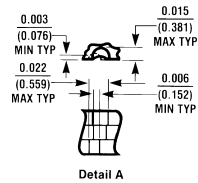
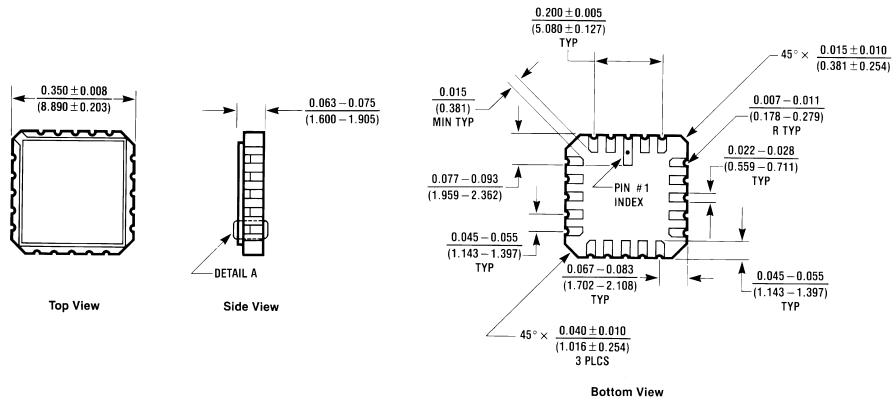
**FIGURE 4. TRI-STATE Output HIGH and LOW Enable and Disable Times**



**FIGURE 5. Propagation Delay Waveforms for Inverting and Non-Inverting Functions**

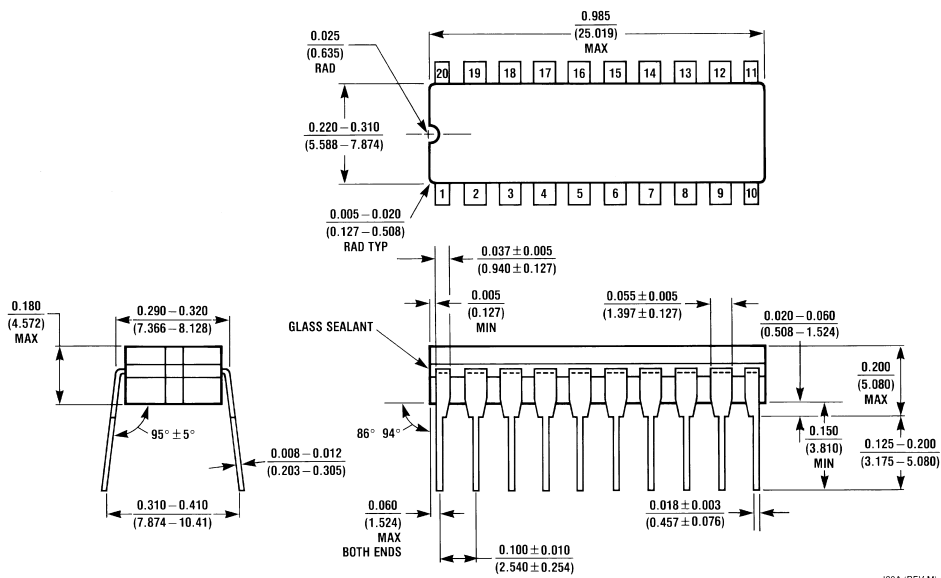


**Physical Dimensions** inches (millimeters) unless otherwise noted



E20A (REV D)

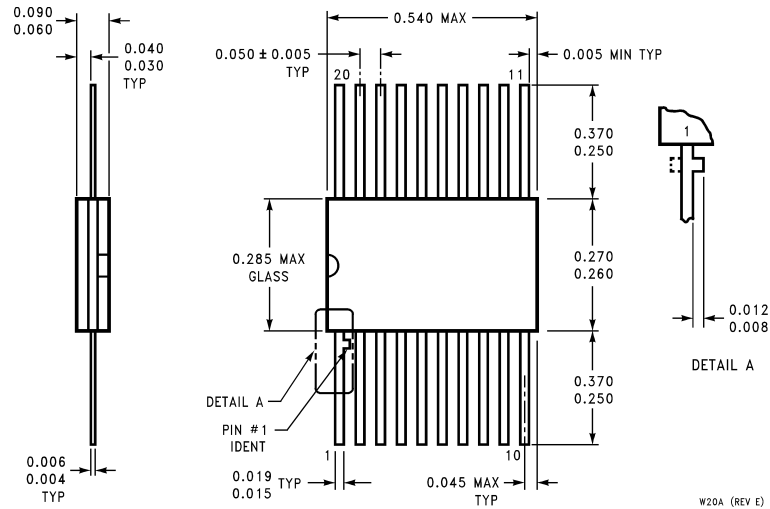
**20-Terminal Ceramic Chip Carrier (L)**  
**NS Package Number E20A**



J20A (REV M)

**20-Lead Ceramic Dual-In-Line Package (D)**  
**NS Package Number J20A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



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