National Semiconductor

August 1998

54ABT652 Octal Transceivers and Registers with TRI-STATE® Outputs

General Description

The 'ABT652 consists of bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to HIGH logic level. Output Enable pins (OEAB, $\overline{OEBA}$) are provided to control the transceiver function.

Features

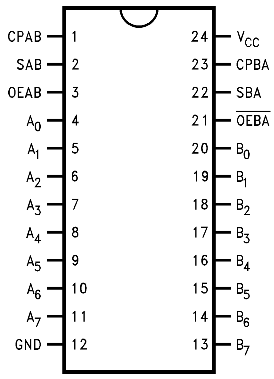
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- A and B output sink capability of 48 mA, source capability of 24 mA
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Standard Microcircuit Drawing (SMD) 5962-9324201

Ordering Code:

Commercial	Package Number	Package Description
54ABT652J-QML	J24A	24-Lead Ceramic Dual-in-line
54ABT652W-QML	W24C	24-Lead Cerpack
54ABT652E-QML	E28A	28-Lead Ceramic Leadless Chip Carrier, Type C

Connection Diagram

Pin Assignment for DIP and Flatpack



DS100220-1

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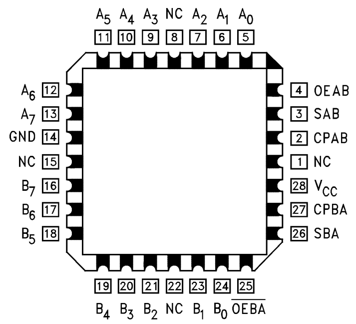
Connection Diagram (Continued)

Pin Assignment for LCC



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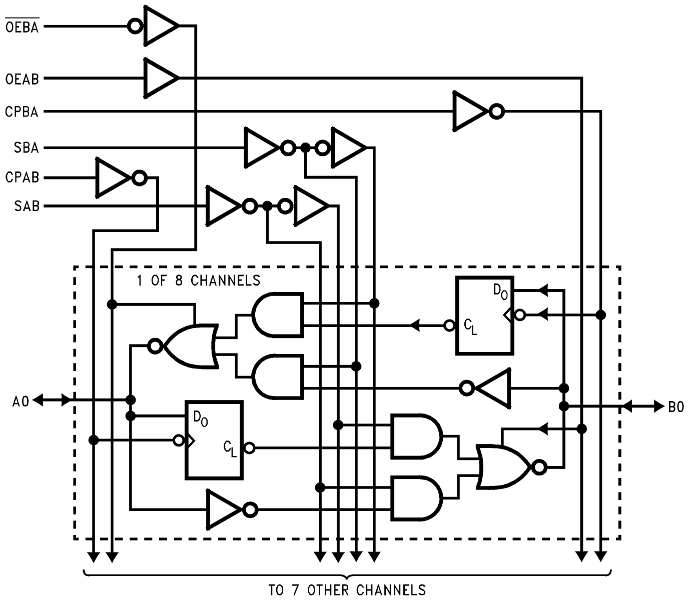
Pin Descriptions

Pin Names	Description
A_0–A_7	Data Register A Inputs/TRI-STATE Outputs
B_0–B_7	Data Register B Inputs/TRI-STATE Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Select Inputs
OEAB, $\overline{\text{OEBA}}$	Output Enable Inputs

Logic Diagram



DS100220-3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both.

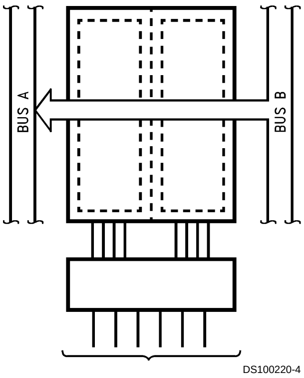
The select (SAB, SBA) controls can multiplex stored and real-time.

The examples in *Figure 1* demonstrate the four fundamental bus-management functions that can be performed with the 'ABT652C.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appropriate Clock Inputs (CPAB, CPBA) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

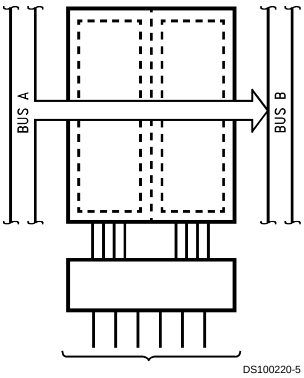
Functional Description (Continued)

Note A: Real-Time Transfer Bus B to Bus A



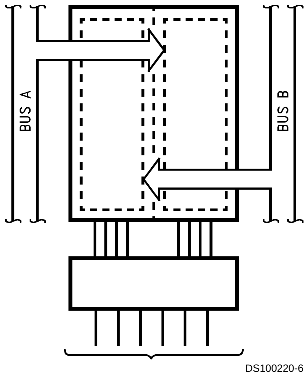
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

Note B: Real-Time Transfer Bus A to Bus B



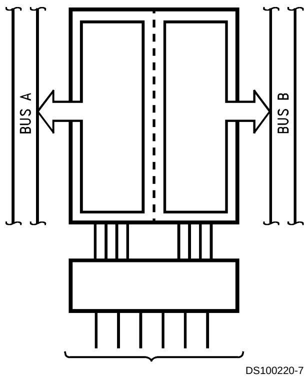
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

Note C: Storage



OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
X	H	N	X	X	X
L	X	X	N	X	X
L	H	N	N	X	X

Note D: Transfer Storage Data to A or B



OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	H

FIGURE 1.

Functional Description (Continued)

Inputs						Inputs/Outputs (Note 1)		Operating Mode
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	A_0 thru A_7	B_0 thru B_7	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	N	N	X	X			Store A and B Data
X	H	N	H or L	X	X	Input	Not Specified	Store A, Hold B
H	H	N	N	X	X	Input	Output	Store A in Both Registers
L	X	H or L	N	X	X	Not Specified	Input	Hold A, Store B
L	L	N	N	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
N = LOW to HIGH Clock Transition

Note 1: The data output functions may be enabled or disabled by various signals at OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs.

Absolute Maximum Ratings (Note 2)

Storage Temperature	−65˚C to +150˚C
Ambient Temperature under Bias	−55˚C to +125˚C
Junction Temperature under Bias	
Ceramic	−55˚C to +175˚C
V_{CC} Pin Potential to	
Ground Pin	−0.5V to +7.0V
Input Voltage (Note 3)	−0.5V to +7.0V
Input Current (Note 3)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disable or	
or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55˚C to +125˚C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		ABT652 Min	ABT652 Typ	ABT652 Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage	54ABT 54ABT	2.5 2.0			V	Min	I_{OH} = −3 mA, (A_n, B_n) I_{OH} = −24 mA, (A_n, B_n)
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA, (A_n, B_n)
I_{IH}	Input HIGH Current				2	µA	Max	V_{IN} = 2.7V (Non-I/O Pins) (Note 4) V_{IN} = V_{CC} (Non-I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test				7	µA	Max	V_{IN} = 7.0V (Non-I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)				100	µA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current				−2	µA	Max	V_{IN} = 0.5V (Non-I/O Pins) (Note 4) V_{IN} = 0.0V (Non-I/O Pins)
I_{IH} + I_{OZH}	Output Leakage Current				50	µA	0V–5.5V	V_{OUT} = 2.7V (A_n, B_n); $\overline{OEBA}$ = 2.0V and OEAB = GND = 2.0V
I_{IL} + I_{OZL}	Output Leakage Current				−50	µA	0V–5.5V	V_{OUT} = 0.5V (A_n, B_n); $\overline{OEBA}$ = 2.0V and OEAB = GND = 2.0V
I_{OS}	Output Short-Circuit Current		−50		−180	mA	Max	V_{OUT} = 0V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{CCH}	Power Supply Current				250	µA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				250	µA	Max	Outputs TRI-STATE; All others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input				2.5	mA	Max	V_I = V_{CC} − 2.1V All others at V_{CC} or GND

Note 4: Guaranteed but not tested.

Note 5: For 8 outputs toggling, I_{CCD} < 1.4 mA/MHz.

Note 6: Guaranteed, but not tested.

DC Electrical Characteristics

Symbol	Parameter	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	1.2	V	5.0	T_A = 25°C (Note 7)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	-1.8	V	5.0	T_A = 25°C (Note 7)

Note 7: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

AC Electrical Characteristics

Symbol	Parameter	54ABT T_A = −55°C to +125°C V_{CC} = 4.5V–5.5V C_L = 50 pF		Units	Fig. No.
		Min	Max		
f_{max}	Max Clock Frequency	125		MHz	
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	1.4 1.2	7.8 8.4	ns	*Figure 5*
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	1.5 1.5	6.7 6.7	ns	*Figure 5*
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A_n to B_n	1.2 1.2	6.9 7.7	ns	*Figure 5*
t_{PZH} t_{PZL}	Enable Time $\overline{OEBA}$ or OEAB to A_n or B_n	1.3 2.0	5.6 7.8	ns	*Figure 7*
t_{PHZ} t_{PLZ}	Disable Time $\overline{OEBA}$ or OEAB to A_n or B_n	1.5 1.5	8.2 7.3	ns	*Figure 7*

AC Operating Requirements

Symbol	Parameter	54ABT T_A = −55°C to +125°C V_{CC} = 4.5V–5.5V C_L = 50 pF		Units	Fig. No.
		Min	Max		
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW Bus to Clock	3.5		ns	*Figure 8*
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW Bus to Clock	1.5		ns	*Figure 8*
$t_W(H)$ $t_W(L)$	Pulse Width, HIGH or LOW	4.0		ns	*Figure 6*

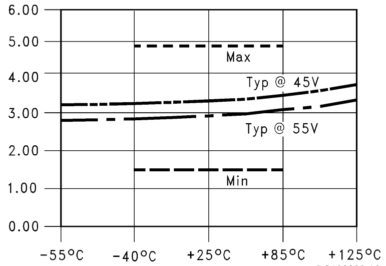
Capacitance

Symbol	Parameter	Max	Units	Conditions (T_A = 25°C)
C_{IN}	Input Capacitance	14.0	pF	V_{CC} = 0V (non I/O pins)
$C_{I/O}$ (Note 8)	I/O Capacitance	19.5	pF	V_{CC} = 5.0V (A_n, B_n)

Note 8: $C_{I/O}$ is measured at frequency, f = 1 MHz, per MIL-STD-883D, Method 3012.

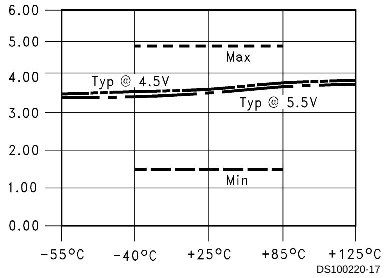
Capacitance (Continued)

t_{PLH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
Clock to Bus



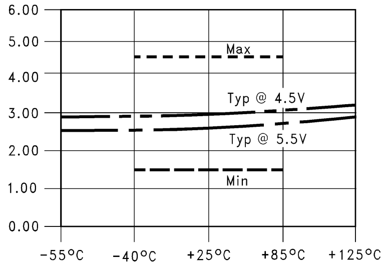
DS100220-16

t_{PHL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
Clock to Bus



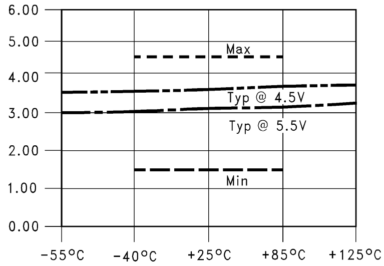
DS100220-17

t_{PLH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
Bus to Bus



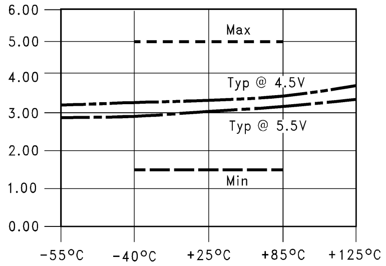
DS100220-18

t_{PHL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
Bus to Bus



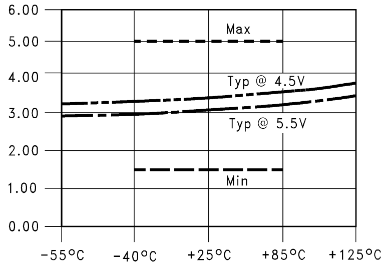
DS100220-19

t_{PLH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
SBA or SAB to A_n or B_n



DS100220-20

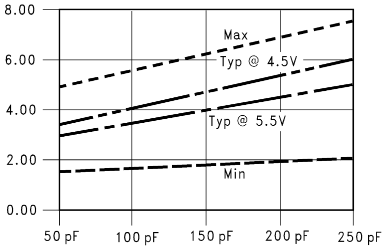
t_{PHL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
SBA or SAB to A_n or B_n



DS100220-21

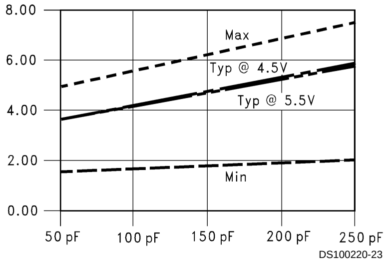
Capacitance (Continued)

t_{PLH} vs Load Capacitance
1 Output Switching, T_A = 25˚C
Clock to Bus



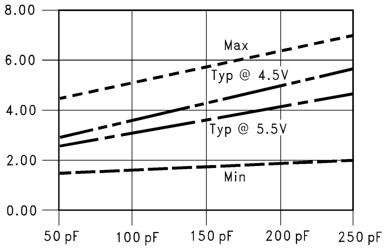
DS100220-22

t_{PHL} vs Load Capacitance
1 Output Switching, T_A = 25˚C
Clock to Bus



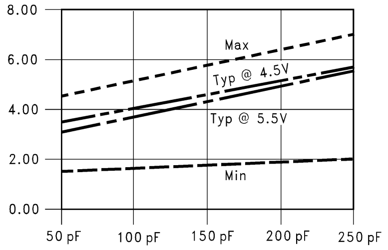
DS100220-23

t_{PLH} vs Load Capacitance
1 Output Switching, T_A = 25˚C
Bus to Bus



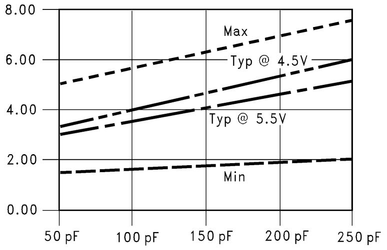
DS100220-24

t_{PHL} vs Load Capacitance
1 Output Switching, T_A = 25˚C
Bus to Bus



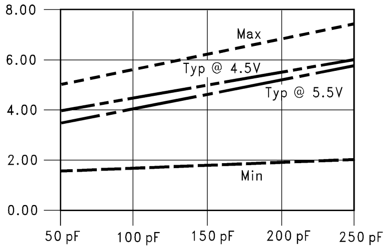
DS100220-25

t_{PLH} vs Load Capacitance
1 Output Switching, T_A = 25˚C
SBA or SAB to A_n or B_n



DS100220-26

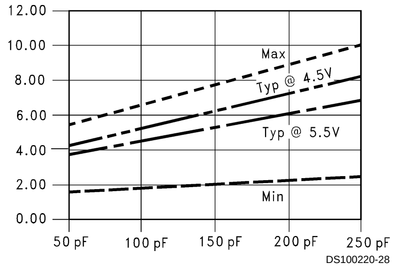
t_{PHL} vs Load Capacitance
1 Output Switching, T_A = 25˚C
SBA or SAB to A_n or B_n



DS100220-27

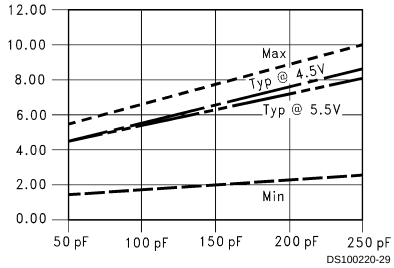
Capacitance (Continued)

t_{PLH} vs Load Capacitance
8 Outputs Switching, T_A = 25˚C
Clock to Bus



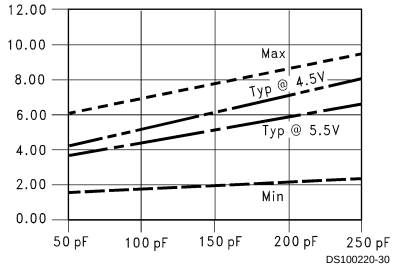
DS100220-28

t_{PHL} vs Load Capacitance
8 Outputs Switching, T_A = 25˚C
Clock to Bus



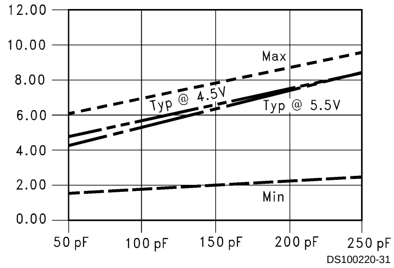
DS100220-29

t_{PLH} vs Load Capacitance
8 Outputs Switching, T_A = 25˚C
Bus to Bus



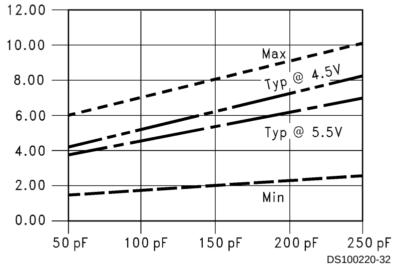
DS100220-30

t_{PHL} vs Load Capacitance
8 Outputs Switching, T_A = 25˚C
Bus to Bus



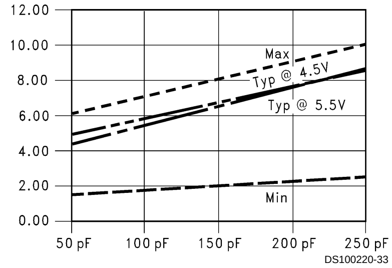
DS100220-31

t_{PLH} vs Load Capacitance
8 Outputs Switching, T_A = 25˚C
SBA or SAB to A_n or B_n



DS100220-32

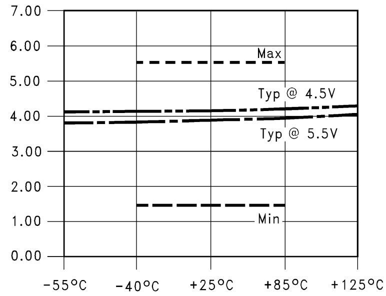
t_{PHL} vs Load Capacitance
8 Outputs Switching, T_A = 25˚C
SBA or SAB to A_n or B_n



DS100220-33

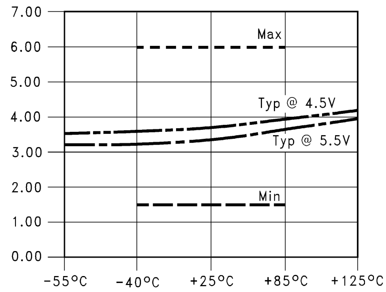
Capacitance (Continued)

t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



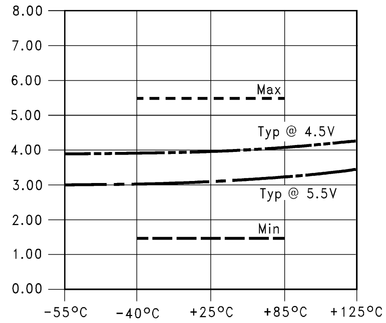
DS100220-34

t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



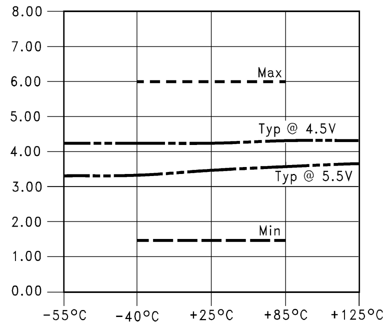
DS100220-35

t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



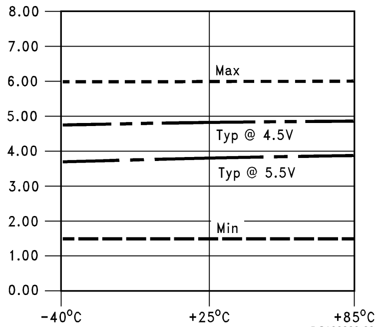
DS100220-36

t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



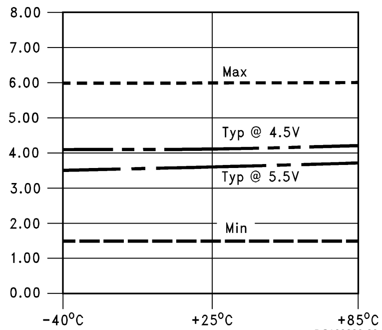
DS100220-37

t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



DS100220-38

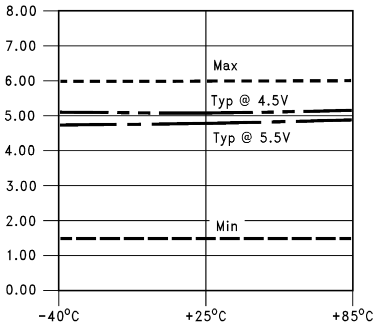
t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



DS100220-39

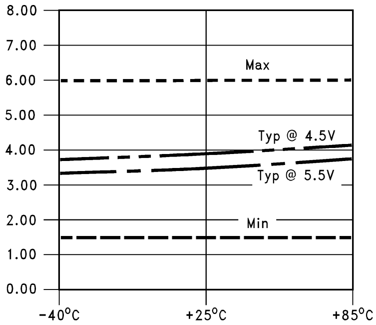
Capacitance (Continued)

t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



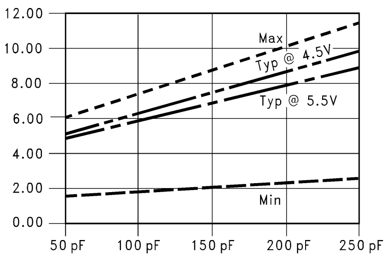
DS100220-40

t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



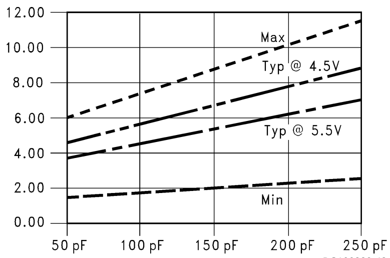
DS100220-41

t_{PZL} vs Load Capacitance
8 Outputs Switching
T_A = 25°C



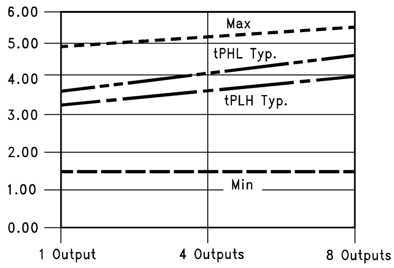
DS100220-42

t_{PZH} vs Load Capacitance
8 Outputs Switching
T_A = 25°C



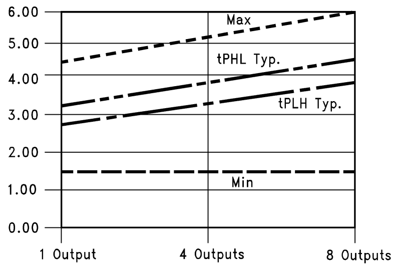
DS100220-43

t_{PLH} and t_{PHL} vs Number Output Switching
V_{CC} = 5V, T_A = 25°C, C_L = 50 pF
Clock to Bus



DS100220-44

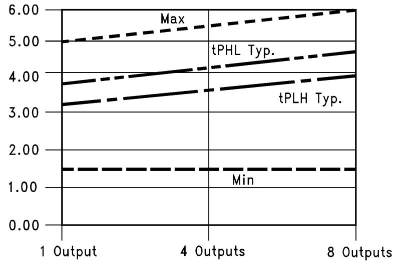
t_{PLH} and t_{PHL} vs Number Output Switching
V_{CC} = 5V, T_A = 25°C, C_L = 50 pF
Bus to Bus



DS100220-45

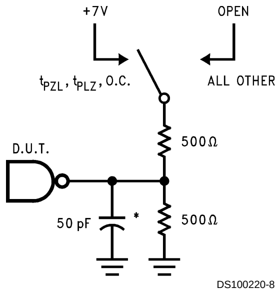
Capacitance (Continued)

t_{PLH} and t_{PHL} vs Number Output Switching
V_{CC} = 5V, T_A = 25˚C, C_L = 50 pF
SBA or SAB to A_n or B_n



DS100220-46

AC Loading



*Includes jig and probe capacitance

FIGURE 2. Standard AC Test Load

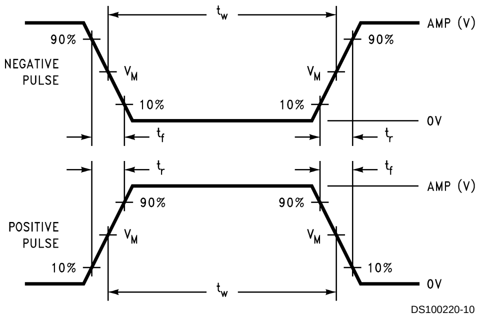


FIGURE 3. Test Input Signal Levels

Input Pulse Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 4. Test Input Signal Requirements

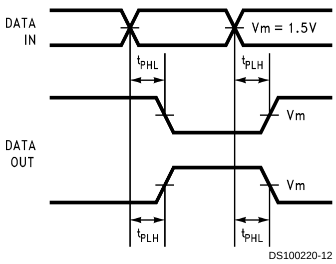


FIGURE 5. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

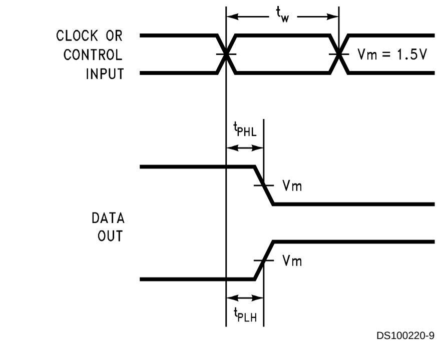


FIGURE 6. Propagation Delay, Pulse Width Waveforms

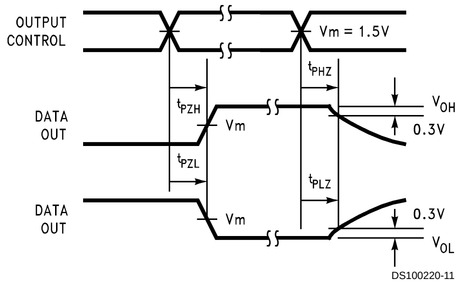


FIGURE 7. TRI-STATE Output HIGH and LOW Enable and Disable Times

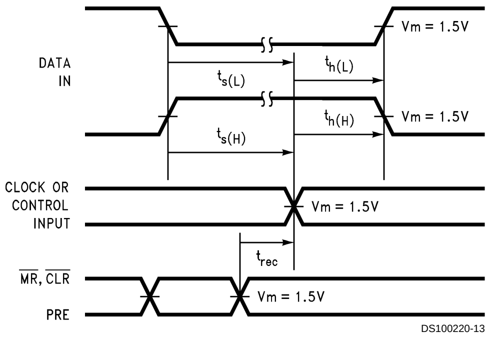
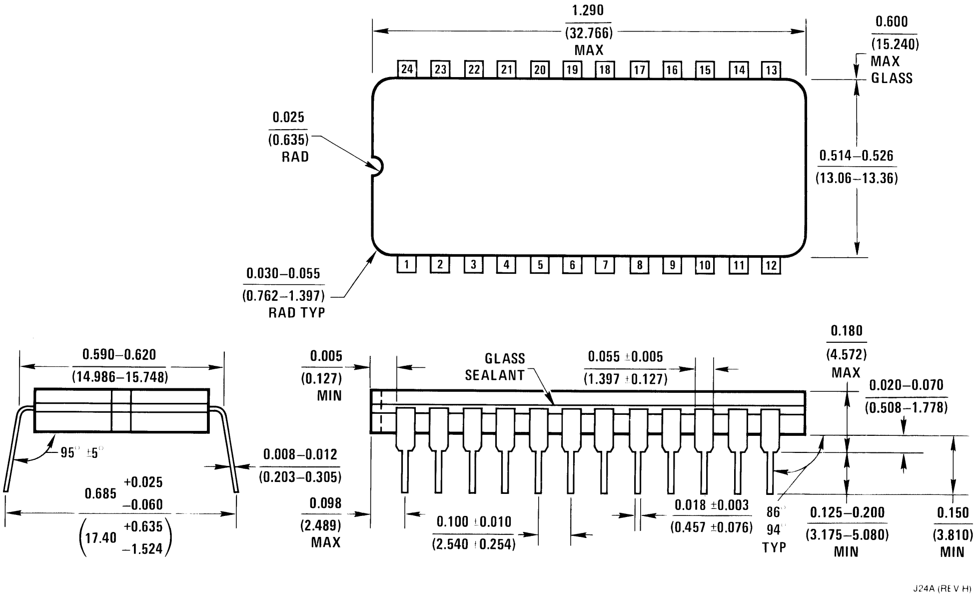
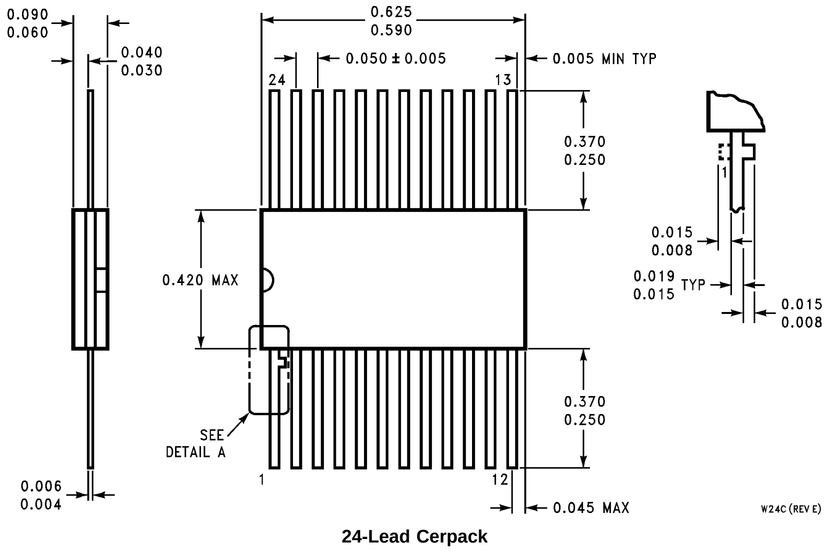


FIGURE 8. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

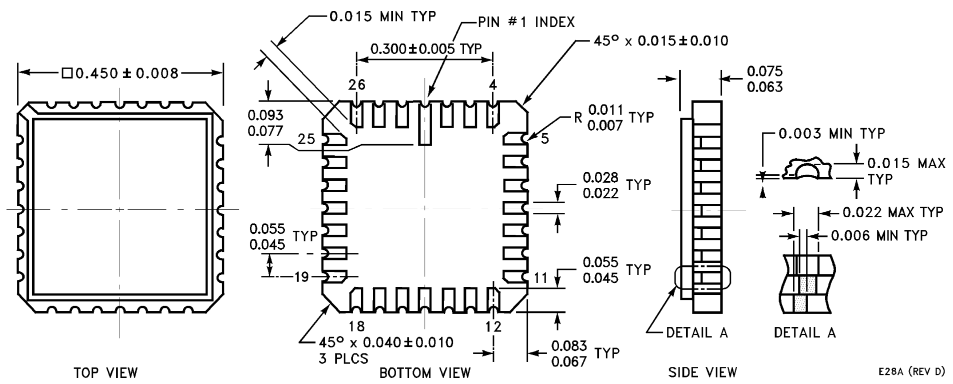


24-Lead Ceramic Dual-in-line
NS Package Number J24A



24-Lead Cerpack
NS Package Number W24C

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Ceramic Leadless Chip Carrier, Type C
NS Package Number E28A

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