

54AC273 Octal D Flip-Flop

General Description

The '273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (MR) input load and reset (clear) all flip-flops simultaneously.

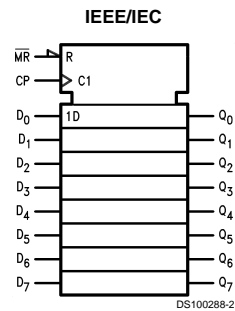
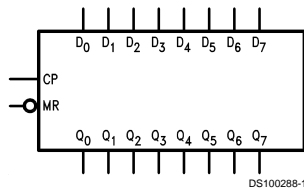
The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the MR input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Features

- Ideal buffer for microprocessor or memory
- Eight edge-triggered D flip-flops
- Buffered common clock
- Buffered, asynchronous master reset
- See '377 for clock enable version
- See '373 for transparent latch version
- See '374 for TRI-STATE® version
- Outputs source/sink 24 mA
- 'ACT has TTL-compatible inputs
- Standard Military Drawing (SMD)
— 'AC273: 5962-87756

Logic Symbols

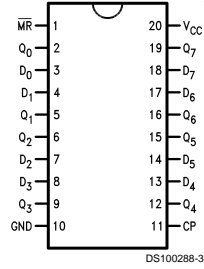


Pin Names	Description
D ₀ -D ₇	Data Inputs
MR	Master Reset
CP	Clock Pulse Input
Q ₀ -Q ₇	Data Outputs

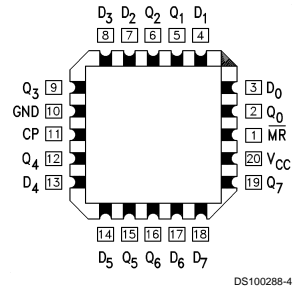
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Connection Diagrams

Pin Assignment
for DIP and Flatpak



Pin Assignment
for LCC

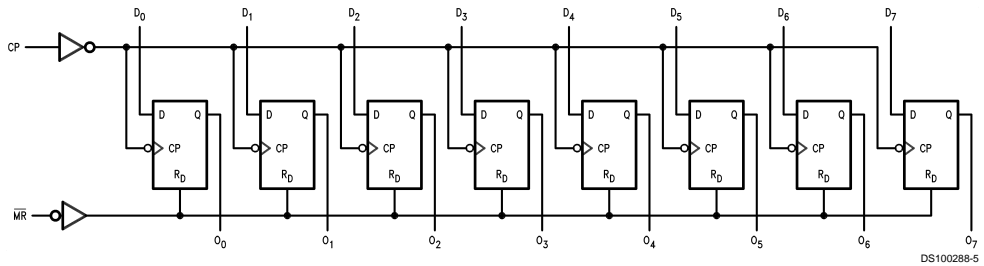


Mode Select-Function Table

Operating Mode	Inputs			Outputs
	MR	CP	D _n	Q _n
Reset (Clear)	L	X	X	L
Load '1'	H	↗	H	H
Load '0'	H	↗	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to to $V_{CC} + 0.5V$
DC Output Source	
or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	-65°C to +150°C

Junction Temperature (T_J)

CDIP

175°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54AC	-55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	54AC	Units	Conditions
			$T_A =$ -55°C to +125°C		
			Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	3.0	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	3.15		
		5.5	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	1.35		
		5.5	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.9	V	$I_{OUT} = -50 \mu A$
		4.5	4.4		
		5.5	5.4		
V_{OL}	Maximum Low Level Output Voltage	3.0	2.4	V	(Note 2) $V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
		4.5	3.7		
		5.5	4.7		
V_{OL}	Maximum Low Level Output Voltage	3.0	0.1	V	$I_{OUT} = 50 \mu A$
		4.5	0.1		
		5.5	0.1		
V_{OL}	Maximum Low Level Output Voltage	3.0	0.50	V	(Note 2) $V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
		4.5	0.50		
		5.5	0.50		
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	μA	$V_I = V_{CC}, GND$
I_{OLD}	(Note 3) Minimum Dynamic Output Current	5.5	50	mA	$V_{OLD} = 1.65V \text{ Max}$
I_{OHD}		5.5	-50	mA	$V_{OHD} = 3.85V \text{ Min}$

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	54AC		Units	Conditions
			T _A = -55°C to +125°C			
			Guaranteed Limits			
I _{CC}	Maximum Quiescent Supply Current	5.5	80.0		μA	V _{IN} = V _{CC} or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V) (Note 5)	54AC		Units	Fig. No.
			T _A = -55°C to +125°C			
			C _L = 50 pF			
			Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0	75 90		MHz	
t _{PLH}	Propagation Delay Clock to Output	3.3 5.0	1.0 1.0	15.0 11.0	ns	
t _{PHL}	Propagation Delay Clock to Output	3.3 5.0	1.0 1.0	16.0 11.5	ns	
t _{PHL}	Propagation Delay MR to Output	3.3 5.0	1.0 1.0	16.0 11.5	ns	

Note 5: Voltage Range 3.3 is 3.3V ±0.3V. Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V _{CC} (V) (Note 6)	54AC		Units	Fig. No.
			T _A = -55°C to +125°C			
			C _L = 50 pF			
			Guaranteed Minimum			
t _s	Setup Time, HIGH or LOW Data to CP	3.3 5.0	8.0 5.0		ns	
t _h	Hold Time, HIGH or LOW Data to CP	3.3 5.0	0 1.0		ns	
t _w	Clock Pulse Width HIGH or LOW	3.3 5.0	6.5 5.0		ns	
t _w	MR Pulse Width HIGH or LOW	3.3 5.0	10.0 6.5		ns	
t _{rec}	Recovery Time MR to CP	3.3 5.0	6.0 4.0		ns	

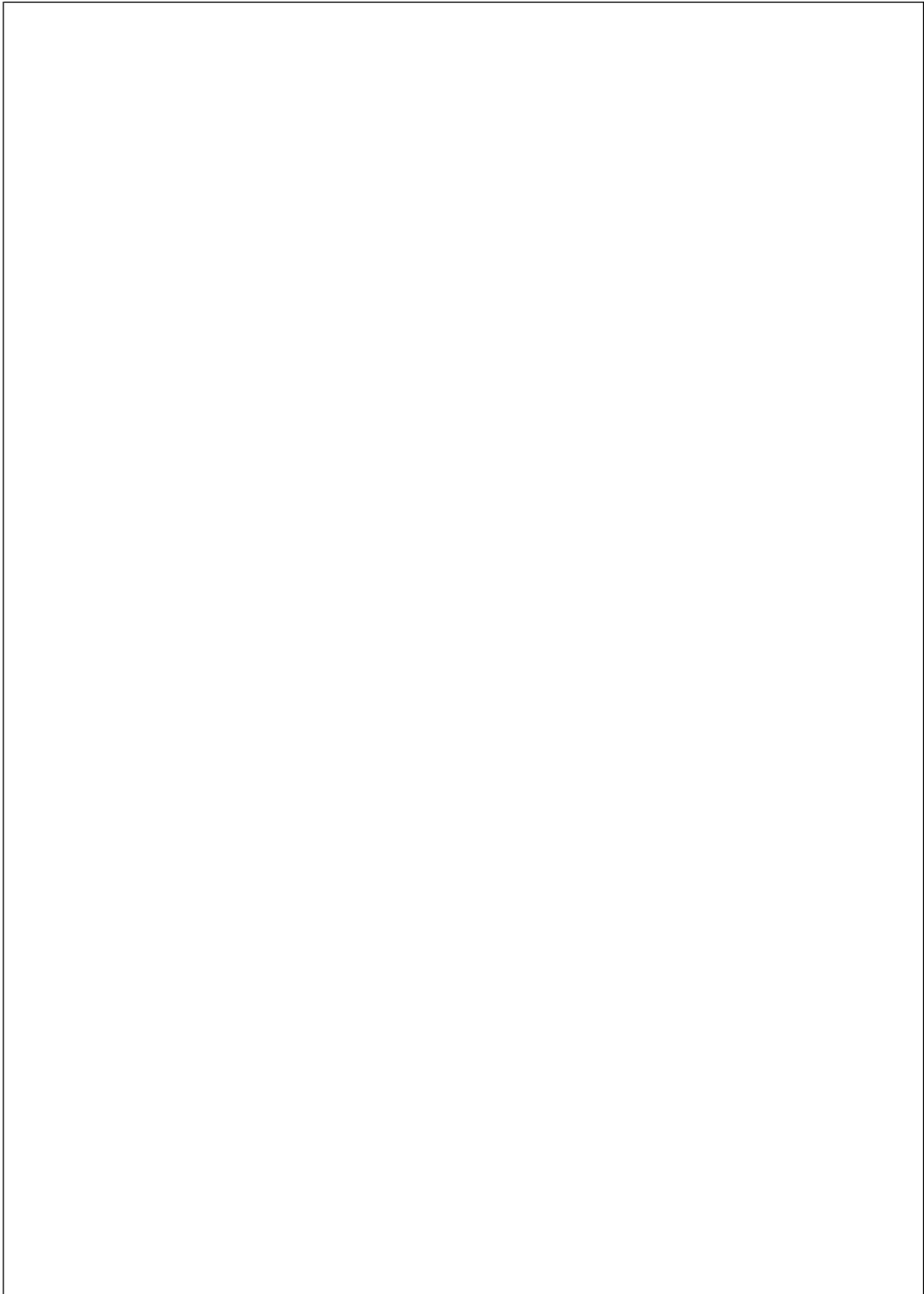
Note 6: Voltage Range 3.3 is 3.3V ±0.3V. Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

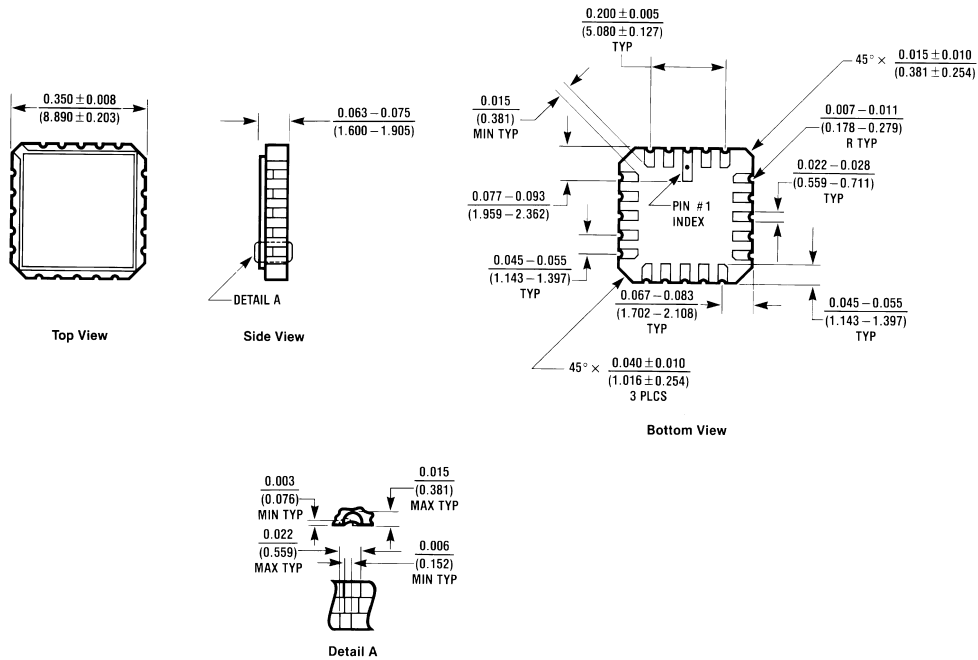
Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = \text{Open}$
C_{PD}	Power Dissipation Capacitance	50.0	pF	$V_{CC} = 5.0V$

Book
Extract
End

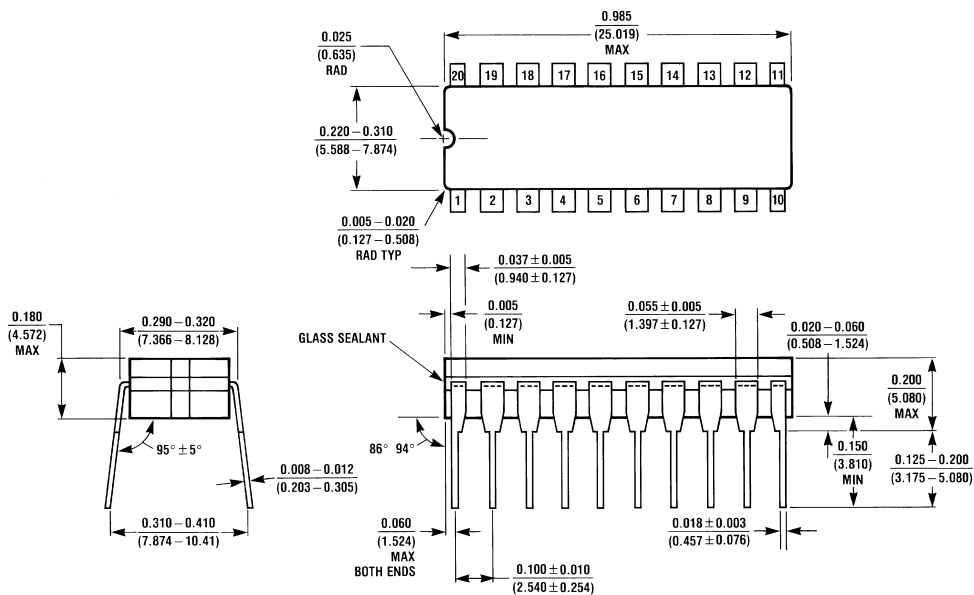
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Physical Dimensions inches (millimeters) unless otherwise noted

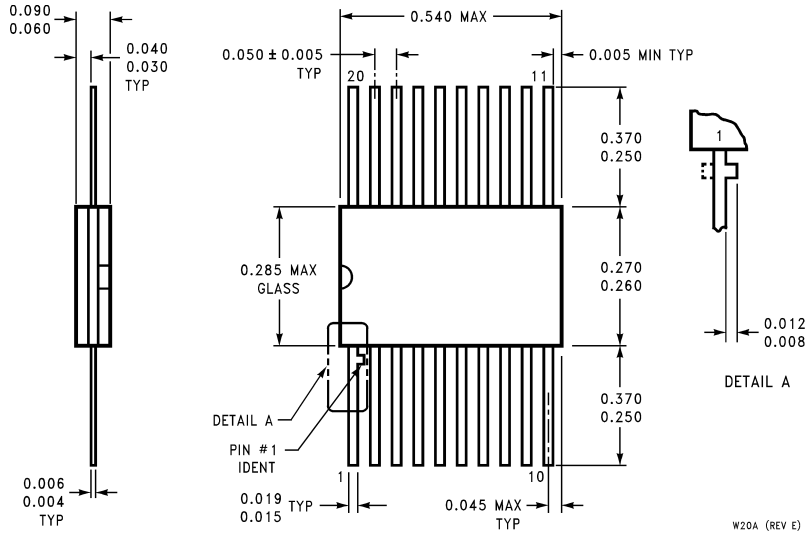


**20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A**



**20 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20 Lead Ceramic Flatpak (F)
NS Package Number W20A**

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