July 1998

National Semiconductor

54AC257 • 54ACT257
Quad 2-Input Multiplexer with TRI-STATE® Outputs

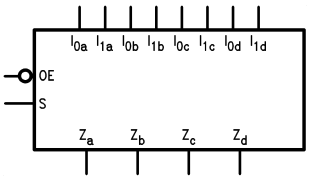
General Description

The 'AC/'ACT257 is a quad 2-input multiplexer with TRI-STATE outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (noninverted) form. The outputs may be switched to a high impedance state by placing a logic HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus-oriented systems.

Features

- I_{CC} and I_{OZ} reduced by 50%
- Multiplexer expansion by tying outputs together
- Noninverting TRI-STATE outputs
- Outputs source/sink 24 mA
- 'ACT257 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - — 'AC257: 5962-88703
  - — 'ACT257: 5962-89689

Logic Symbols



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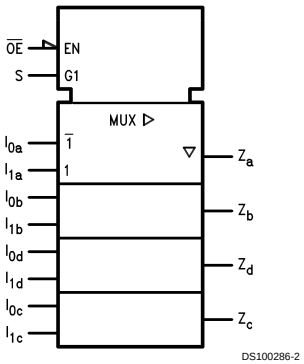
IEEE/IEC



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Pin Names	Description
S	Common Data Select Input
$\overline{OE}$	TRI-STATE Output Enable Input
I_{0a}–I_{0d}	Data Inputs from Source 0
I_{1a}–I_{1d}	Data Inputs from Source 1
Z_a–Z_d	TRI-STATE Multiplexer Outputs

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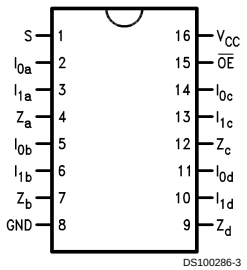
Connection Diagrams

Pin Assignment for DIP and Flatpak



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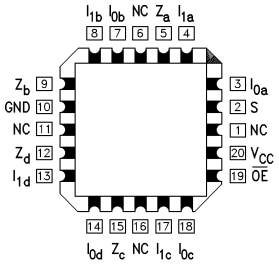
Pin Assignment for LCC



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Functional Description

The 'AC/'ACT257 is quad 2-input multiplexer with TRI-STATE outputs. It selects four bits of data from two sources under control of a Common Data Select input. When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in true (noninverted) form. The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE} \bullet (1_{1a} \bullet S + I_{0a} \bullet \overline{S})$$
$$Z_b = \overline{OE} \bullet (1_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$Z_c = \overline{OE} \bullet (1_{1c} \bullet S + I_{0c} \bullet \overline{S})$$
$$Z_d = \overline{OE} \bullet (1_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

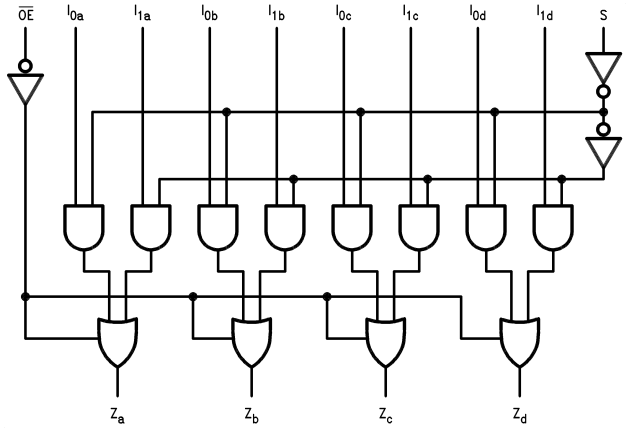
When the Output Enable ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so there is no overlap.

Truth Table

Output Enable	Select Input	Data Inputs		Outputs
$\overline{OE}$	S	I_0	I_1	Z
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



DS100286-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} +0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current Per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65˚C to +150˚C
Junction Temperature (T_J)	
CDIP	175˚C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54AC/ACT	−55˚C to +125˚C
Minimum Input Edge Rate (ΔV/Δt)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	54AC T_A = −55˚C to +125˚C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	3.0	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	3.15		
		5.5	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	1.35		
		5.5	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.9	V	I_{OUT} = −50 μA
		4.5	4.4		
		5.5	5.4		
					(Note 2) V_{IN} = V_{IL} or V_{IH}
		3.0	2.4		−12 mA
		4.5	3.7	V	I_{OH} −24 mA
		5.5	4.7		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.1	V	I_{OUT} = 50 μA
		4.5	0.1		
		5.5	0.1		
					(Note 2) V_{IN} = V_{IL} or V_{IH}
		3.0	0.50		12 mA
		4.5	0.50	V	I_{OL} 24 mA
		5.5	0.50		24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for ’AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	54AC T_A = −55˚C to +125˚C Guaranteed Limits	Units	Conditions
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5	±10.0	µA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	(Note 3) Minimum Dynamic Output Current	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	80.0	µA	V_{IN} = V_{CC} or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

Note 5: I_{CC} for 54AC @ 25˚C is identical to 74AC @ 25˚C.

DC Characteristics for ’ACT Family Devices

Symbol	Parameter	V_{CC} (V)	54ACT T_A = −55˚C to +125˚C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5	2.0	V	V_{OUT} = 0.1V
		5.5	2.0		or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5	0.8	V	V_{OUT} = 0.1V
		5.5	0.8		or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5	4.4	V	I_{OUT} = −50 µA
		5.5	5.4		
					(Note 6) V_{IN} = V_{IL} or V_{IH}
		4.5	3.70	V	I_{OH} −24 mA
		5.5	4.70		−24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.1	V	I_{OUT} = 50 µA
		5.5	0.1		
					(Note 6) V_{IN} = V_{IL} or V_{IH}
		4.5	0.50	V	I_{OL} 24 mA
		5.5	0.50		24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5	±10.0	µA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	1.6	mA	V_I = V_{CC} − 2.1V
I_{OLD}	(Note 7) Minimum Dynamic Output Current	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min

DC Characteristics for 'ACT Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	54ACT T_A = −55°C to +125°C Guaranteed Limits	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	5.5	80.0	µA	$V_{IN} = V_{CC}$ or GND

Note 6: All outputs loaded; thresholds on input associated with output under test.

Note 7: Maximum test duration 2.0 ms, one output loaded at a time.

Note 8: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 9)	54AC T_A = −55°C to +125°C C_L = 50 pF		Units
t_{PLH}	Propagation Delay	3.3	1.0	11.0	ns
	I_n to Z_n	5.0	1.0	8.0	
t_{PHL}	Propagation Delay	3.3	1.0	11.0	ns
	I_n to Z_n	5.0	1.0	8.5	
t_{PLH}	Propagation Delay	3.3	1.0	14.5	ns
	S to Z_n	5.0	1.0	11.0	
t_{PHL}	Propagation Delay	3.3	1.0	14.5	ns
	S to Z_n	5.0	1.0	11.0	
t_{PZH}	Output Enable Time	3.3	1.0	13.0	ns
		5.0	1.0	10.0	
t_{PZL}	Output Enable Time	3.3	1.0	11.0	ns
		5.0	1.0	9.5	
t_{PHZ}	Output Disable Time	3.3	1.0	13.0	ns
		5.0	1.0	11.0	
t_{PLZ}	Output Disable Time	3.3	1.0	10.5	ns
		5.0	1.0	9.5	

Note 9: Voltage Range 3.3 is 3.0V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 10)	54ACT T_A = −55°C to +125°C C_L = 50 pF		Units
t_{PLH}	Propagation Delay	5.0	1.0	8.0	ns
	I_n to Z_n				
t_{PHL}	Propagation Delay	5.0	1.0	9.5	ns
	I_n to Z_n				
t_{PLH}	Propagation Delay	5.0	1.0	11.0	ns
	S to Z_n				
t_{PHL}	Propagation Delay	5.0	1.0	11.5	ns
	S to Z_n				
t_{PZH}	Output Enable Time	5.0	1.0	9.5	ns

AC Electrical Characteristics (Continued)

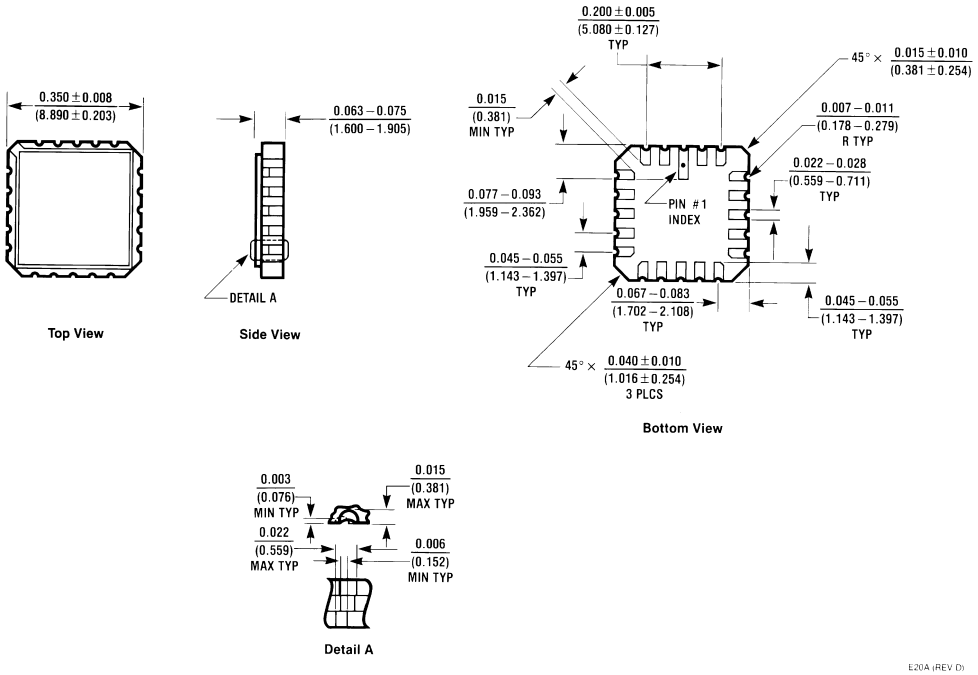
Symbol	Parameter	V_{CC} (V) (Note 10)	54ACT $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF		Units
t_{PZL}	Output Enable Time	5.0	1.0	9.5	ns
t_{PHZ}	Output Disable Time	5.0	1.0	10.5	ns
t_{PLZ}	Output Disable Time	5.0	1.0	9.5	ns

Note 10: Voltage Range 5.0 is 5.0V ±0.5V

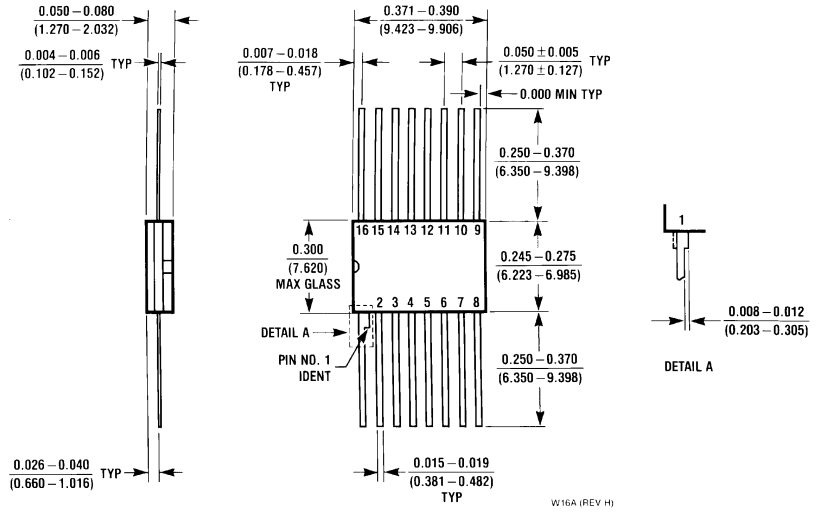
Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	50.0	pF	V_{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted



20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A



16 Lead Ceramic Flatpak (F)
NS Package Number W16A

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