

September 1998

54ACTQ377

Octal D Flip-Flop with Clock Enable

General Description

The ACTQ377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable (CE) is LOW.

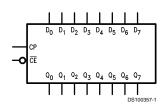
The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{\text{CE}}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

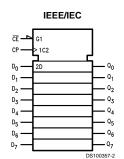
The ACTQ377 utilizes FACT Quiet Series® technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series features GTO® output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- Ideal for addressable register applications
- Clock enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- Outputs source/sink 24 mA
- See '273 for master reset version
- See '373 for transparent latch version
- See '374 for TRI-STATE® version
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- TTL-compatible inputs and outputs
- Standard Microcircuit Drawing (SMD) 5962-9219001

Logic Symbols





Pin	Description			
Names				
D ₀ -D ₇	Data Inputs			
CE	Clock Enable (Active LOW)			
Q ₀ -Q ₇	Data Outputs			
СР	Clock Pulse Input			

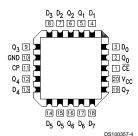
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Connection Diagrams

Pin Assignment for DIP and Flatpak



Pin Assignment for LCC

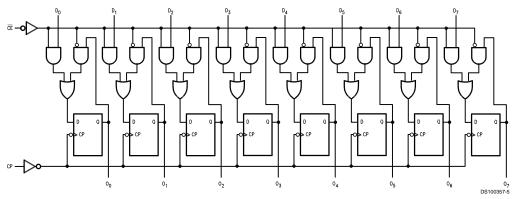


Mode Select-Function Table

Operating Mode		Inputs	Outputs	
	СР	CE	D _n	Qn
Load '1'	N	L	Н	Н
Load '0'	N	L	L	L
Hold (Do Nothing)	N	Н	Х	No Change
	X	Н	X	No Change

- H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 N = LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

-0.5V to +7.0V Supply Voltage (V_{CC}) DC Input Diode Current (I_{IK}) $V_1 = -0.5V$ -20 mA $V_I = V_{CC} + 0.5V$ +20 mA -0.5V to $V_{\rm CC}$ + 0.5V DC Input Voltage (V_I) DC Output Diode Current (I_{OK}) $V_{O} = -0.5V$ -20 mA $V_{\rm O} = V_{\rm CC} + 0.5V$ +20 mA DC Output Voltage (V_O) -0.5V to $V_{\rm CC}$ + 0.5V DC Output Source

Junction Temperature (T_J)

CDIP 175°C

Recommended Operating Conditions

Supply Voltage (V_{CC})

 $\begin{tabular}{lll} 'ACTQ & 4.5V to 5.5V \\ Input Voltage (V_i) & 0V to V_{CC} \\ Output Voltage (V_O) & 0V to V_{CC} \\ \end{tabular}$

Operating Temperature (T_A)

Minimum Input Edge Rate ($\Delta V/\Delta t$)

'ACTQ Devices V_{IN} from 0.8V to 2.0V

V_{CC} @ 4.5V, 5.5V 125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

DC Characteristics for 'ACTQ Family Devices

			54ACTQ			
Symbol	Parameter	V _{cc}	T _A =	Units	Conditions	
		(V)	-55°C to +125°C			
			Guaranteed Limits			
V _{IH}	Minimum High Level	4.5	2.0	V	V _{OUT} = 0.1V	
	Input Voltage	5.5	2.0		or V _{CC} – 0.1V	
V _{IL}	Maximum Low Level	4.5	0.8	V	V _{OUT} = 0.1V	
	Input Voltage	5.5	0.8		or V _{CC} – 0.1V	
V _{OH}	Minimum High Level	4.5	4.4	V	I _{OUT} = -50 μA	
	Output Voltage	5.5	5.4			
					(Note 2)	
					$V_{IN} = V_{IL} \text{ or } V_{IH}$	
		4.5	3.70	V	I _{OH} = -24 mA	
		5.5	4.70		$I_{OH} = -24 \text{ mA}$	
V _{OL}	Maximum Low Level	4.5	0.1	V	I _{OUT} = 50 μA	
	Output Voltage	5.5	0.1			
					(Note 2)	
					$V_{IN} = V_{IL} \text{ or } V_{IH}$	
		4.5	0.50	V	I _{OL} = 24 mA	
		5.5	0.50		I _{OL} = 24 mA	
I _{IN}	Maximum Input	5.5	±1.0	μA	$V_{I} = V_{CC}$, GND	
	Leakage Current					
I _{CCT}	Maximum	5.5	1.6	mA	$V_{I} = V_{CC} - 2.1V$	
	I _{CC} /Input					
I _{OLD}	(Note 3)	5.5	50	mA	V _{OLD} = 1.65V Max	
	Minimum Dynamic					
I _{OHD}	Output Current	5.5	-50	mA	V _{OHD} = 3.85V Min	
I _{cc}	Maximum Quiescent	5.5	160.0	μA	V _{IN} = V _{CC}	
	Supply Current				or GND	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	5.0	1.5	V	(Note 4)	

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DC Characteristics for 'ACTQ Family Devices (Continued)

			54ACTQ		
Symbol	Parameter	V _{cc}	T _A =	Units	Conditions
		(V)	−55°C to +125°C		
			Guaranteed Limits	1	
V _{OLV}	Quiet Output Minimum Dynamic Vol	5.0	-1.2	V	(Note 4)

Note 2: *All outputs loaded; thresholds on input associated with output under test.

Note 3: †Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. one output GND.

AC Electrical Characteristics

Symbol	Parameter	V _{cc} (V) (Note 5)	54ACTQ T _A = -55°C to +125°C C _L = 50 pF		Units	Fig. No.
			Min	Max		
f _{max}	Maximum Clock	5.0	85		MHz	
	Frequency					
t _{PLH}	Propagation Delay	5.0	1.5	10.0	ns	
	CP to Q _n					
t _{PHL}	Propagation Delay	5.0	1.5	10.0	ns	
	CP to Q _n					

Note 5: Voltage Range 5.0 is 5.0V ±0.5V

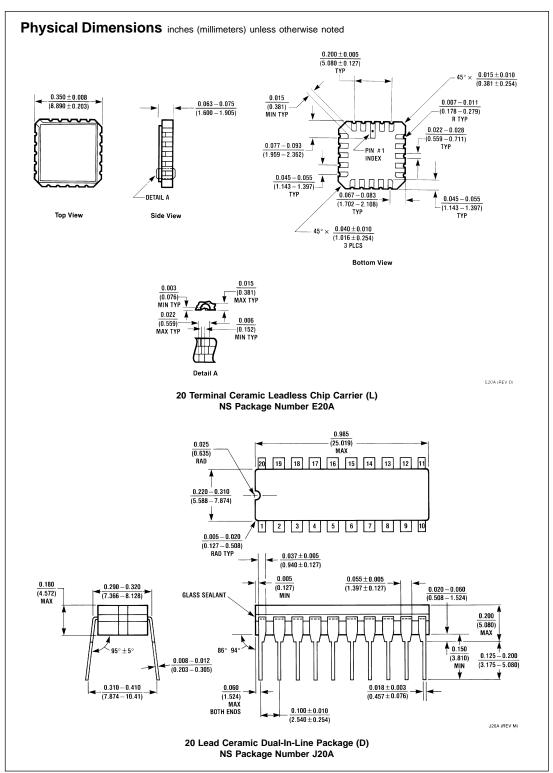
AC Operating Requirements

Symbol	Parameter	V _{cc} (V) (Note 6)	54ACTQ T _A = -55°C to +125°C C _L = 50 pF Guaranteed Minimum	Units	Fig. No.
t _s	Setup Time, HIGH or LOW D _n to CP	5.0	4.0	ns	
t _h	Hold Time, HIGH or LOW D _n to CP	5.0	1.5	ns	
t _s	Setup Time, HIGH or LOW CE to CP	5.0	5.0	ns	
t _h	Hold Time, HIGH or LOW CE to CP	5.0	1.5	ns	
t _w	CP Pulse Width HIGH or LOW	5.0	5.0	ns	

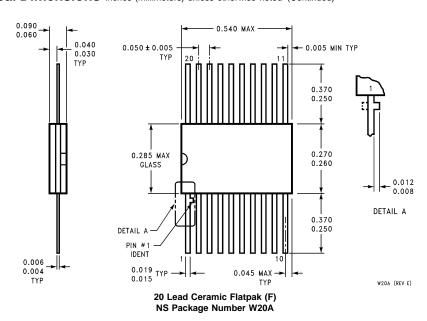
Note 6: Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Тур	Units	Conditions
C _{IN}	Input Capacitance	10.0	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation	80.0	pF	V _{CC} = 5.0V
	Capacitance			



Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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