National Semiconductor

August 1998

54ACQ573 • 54ACTQ573
Quiet Series Octal Latch with TRI-STATE® Outputs

General Description

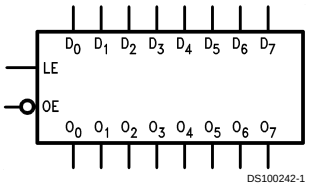
The 'ACQ/'ACTQ573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs. The 'ACQ/'ACTQ573 is functionally identical to the 'ACQ/'ACTQ373 but with inputs and outputs on opposite sides of the package. The 'ACQ/'ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Outputs source/sink 24 mA
- Faster prop delays than standard 'ACT573
- 4 kV minimum ESD immunity
- Standard Microcircuit Drawing (SMD)
  - — 'ACTQ573: 5962-92194
  - — 'ACQ573: 5962-92180

Features

- I_{CC} and I_{OZ} reduced by 50%

Logic Symbols



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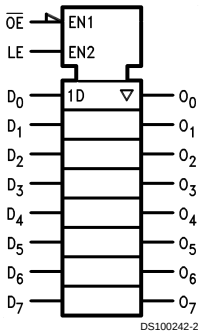
IEEE/IEC



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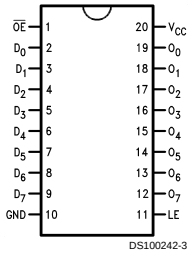
Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

Connection Diagrams

Pin Assignment for DIP and Flatpak



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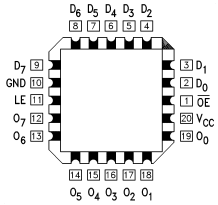
Pin Assignment for LCC



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Functional Description

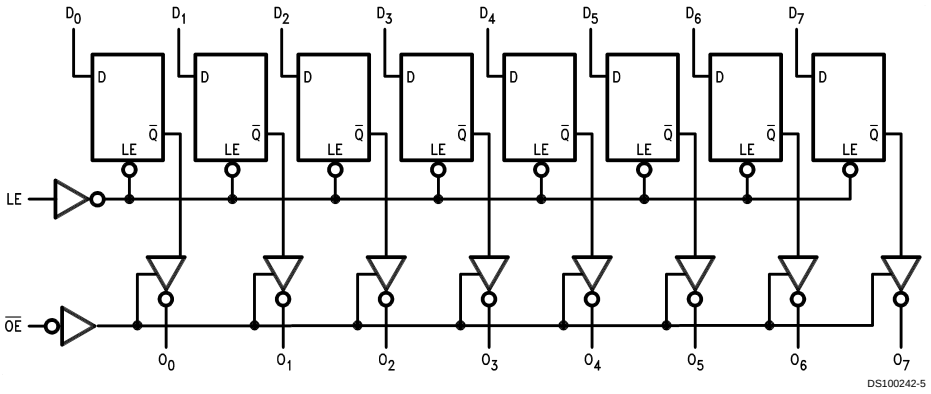
The 'ACQ/'ACTQ573 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are enabled. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
$\overline{OE}$	LE	D	O_n
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage
L = LOW Voltage
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH-to-LOW transition of Latch Enable

Logic Diagram



DS100242-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source	
or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latchup Source	
or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACQ	2.0V to 6.0V
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54ACQ/ACTQ	−55°C to +125°C
Minimum Input Edge Rate ΔV/Δt	
'ACQ Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ΔV/Δt	
'ACTQ Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from −40°C to +125°C.

Note 2: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

DC Characteristics for 'ACQ Family Devices

Symbol	Parameter	V_{CC} (V)	54ACQ T_A = −55°C to +125°C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	3.0	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	3.15		
		5.5	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	1.35		
		5.5	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.9	V	I_{OUT} = −50 μA
		4.5	4.4		
		5.5	5.4		
					(Note 3) V_{IN} = V_{IL} or V_{IH}
		3.0	2.4	V	I_{OH} = −12 mA
		4.5	3.7		I_{OH} = −24 mA
		5.5	4.7		I_{OH} = −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.1	V	I_{OUT} = 50 μA
		4.5	0.1		
		5.5	0.1		
					(Note 3) V_{IN} = V_{IL} or V_{IH}
		3.0	0.50	V	I_{OL} = 12 mA
		4.5	0.50		I_{OL} = 24 mA
		5.5	0.50		I_{OL} = 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	μA	V_I = V_{CC}, GND (Note 5)

DC Characteristics for 'ACQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	54ACQ T_A = −55°C to +125°C Guaranteed Limits	Units	Conditions
I_{OLD}	(Note 4) Minimum Dynamic Output Current	5.5	50	mA	V_{OLD} = 1.65 V_{Max}
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85 V_{Min}
I_{CC}	Maximum Quiescent Supply Current	5.5	80.0	µA	V_{IN} = V_{CC} or GND (Note 5)
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5	±5.0	µA	V_I(OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.75	V	(Notes 6, 7)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−1.2	V	(Notes 6, 7)

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

Note 5: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54ACQ @ 25°C is identical to 74ACQ @ 25°C.

Note 6: Plastic DIP package.

Note 7: Max number of outputs defined as (n). Data Inputs are driven 0V to 5V. One output @ GND.

DC Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	54ACTQ T_A = −55°C to +125°C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.4 5.4	V	I_{OUT} = −50 µA
		4.5 5.5	3.70 4.70	V	(Note 8) V_{IN} = V_{IL} or V_{IH} I_{OH} = −24 mA I_{OH} = −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.1 0.1	V	I_{OUT} = 50 µA
		4.5 5.5	0.50 0.50	V	(Note 8) V_{IN} = V_{IL} or V_{IH} I_{OL} = 24 mA I_{OL} = 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5	±5.0	µA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	1.6	mA	V_I = V_{CC} − 2.1V

DC Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	54ACTQ $T_A = -55^\circ C$ to $+125^\circ C$ Guaranteed Limits	Units	Conditions
I_{OLD}	(Note 9) Minimum Dynamic Output Current	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	80.0	µA	$V_{IN} = V_{CC}$ or GND (Note 10)
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.5	V	(Notes 11, 12)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−1.2	V	(Notes 11, 12)

Note 8: All outputs loaded; thresholds on input associated with output under test.

Note 9: Maximum test duration 2.0 ms, one output loaded at a time.

Note 10: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 11: Plastic DIP package.

Note 12: Max number of outputs defined as (n). Data Inputs are driven 0V to 3V. One output @ GND.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 13)	54ACQ $T_A = -55^\circ C$ to $+125^\circ C$ C_L = 50 pF		Units	Fig. No.
			Min	Max		
t_{PHL}, t_{PLH}	Propagation Delay D_n to O_n	3.3	1.5	16.0	ns	
		5.0	1.5	11.0		
t_{PLH}, t_{PHL}	Propagation Delay LE to O_n	3.3	1.5	15.0	ns	
		5.0	1.5	11.0		
t_{PZL}, t_{PZH}	Output Enable Time	3.3	1.5	13.5	ns	
		5.0	1.5	10.0		
t_{PHZ}, t_{PLZ}	Output Disable Time	3.3	1.5	13.0	ns	
		5.0	1.0	10.5		

Note 13: Voltage Range 5.0 is 5.0V ±0.5V

Voltage Range 3.3 is 3.3V ±0.3V

AC Operating Requirements

Symbol	Parameter	V_{CC} (V) (Note 14)	54ACQ $T_A = -55^\circ C$ to $+125^\circ C$ C_L = 50 pF Guaranteed Minimum	Units
t_S	Setup Time, HIGH or LOW D_n to LE	3.3	4.0	ns
		5.0	4.0	
t_H	Hold Time, HIGH or LOW D_n to LE	3.3	2.0	ns
		5.0	2.0	
t_W	LE Pulse Width, HIGH	3.3	5.0	ns
		5.0	5.0	

Note 14: Voltage Range 5.0 is 5.0V ±0.5V

Voltage Range 3.3 is 3.3V ±0.3V

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 15)	54ACTQ $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Max		
t_{PHL}, t_{PLH}	Propagation Delay D_n to O_n	5.0	1.5	10.0	ns	
t_{PLH}, t_{PHL}	Propagation Delay LE to O_n	5.0	1.5	11.0	ns	
t_{PZL}, t_{PZH}	Output Enable Time	5.0	1.5	11.0	ns	
t_{PHZ}, t_{PLZ}	Output Disable Time	5.0	1.5	11.0	ns	

Note 15: Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

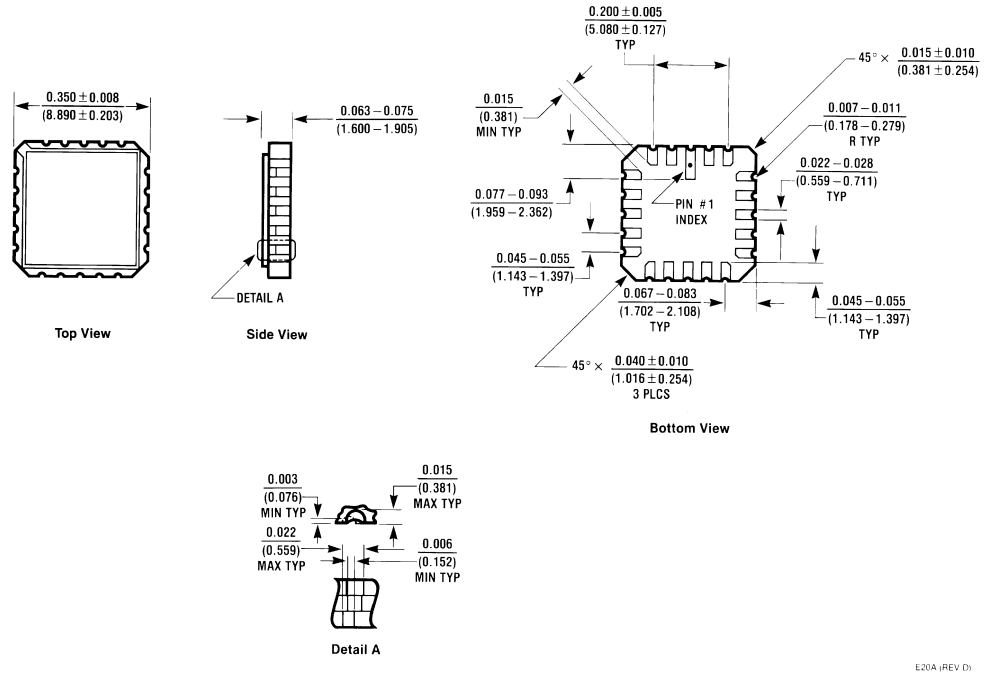
Symbol	Parameter	V_{CC} (V) (Note 16)	54ACTQ $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF	Units	Fig. No.
			Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW D_n to LE	5.0	3.5	ns	
t_H	Hold Time, HIGH or LOW D_n to LE	5.0	1.5	ns	
t_W	LE Pulse Width, HIGH	5.0	5.0	ns	

Note 16: Voltage Range 5.0 is 5.0V ±0.5V

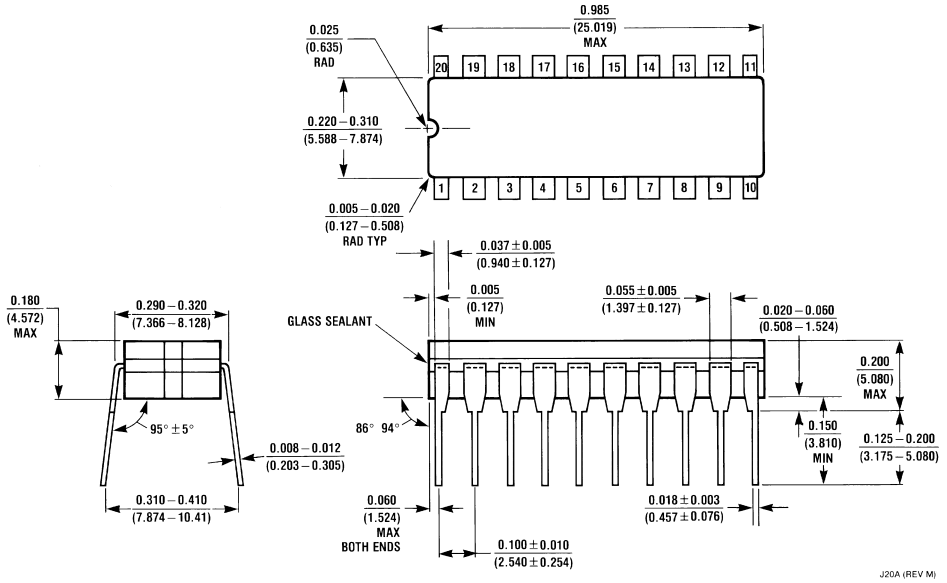
Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	42.0	pF	V_{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted

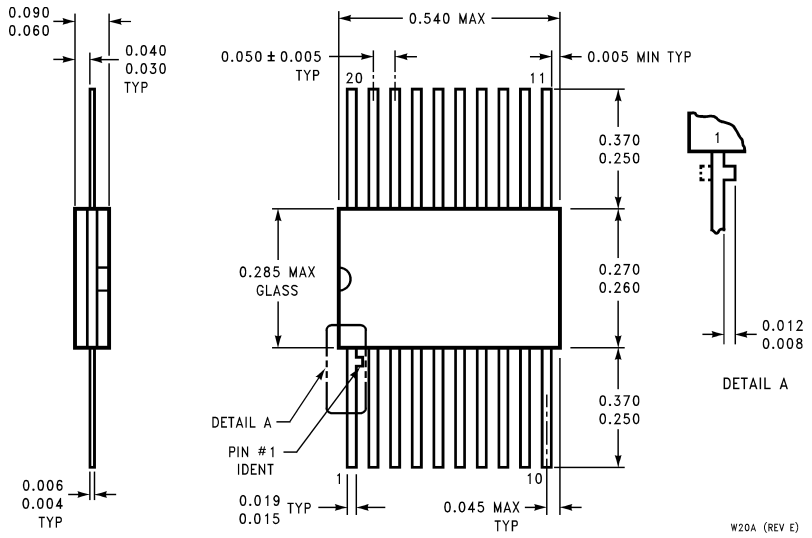


20-Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A



20-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Ceramic Flatpak (F)
NS Package Number W20A

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