National Semiconductor

August 1998

54ACTQ841
Quiet Series 10-Bit Transparent Latch with TRI-STATE® Outputs

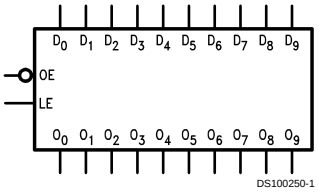
General Description

The 'ACTQ841 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The '841 is a 10-bit transparent latch, a 10-bit version of the '373. The 'ACTQ841 utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance, FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

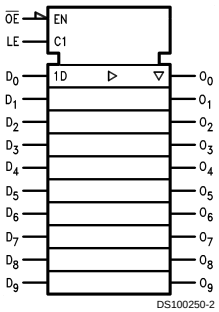
Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Improved latch-up immunity
- Outputs source/sink 24 mA
- 'ACTQ841 has TTL-compatible inputs
- Standard Microcircuit Drawing (SMD) 5962-92200

Logic Symbols



DS100250-1



DS100250-2

Pin Names	Description
D_0–D_9	Data Inputs
O_0–O_9	TRI-STATE Outputs
$\overline{OE}$	Output Enable
LE	Latch Enable

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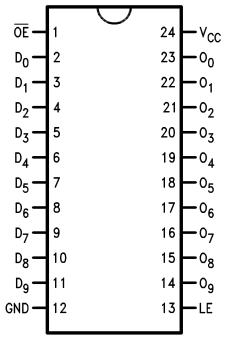
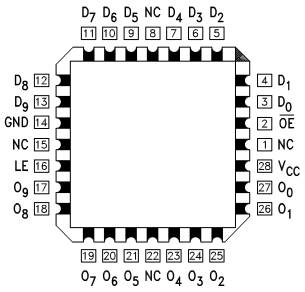
Connection Diagrams

Pin Assignment for DIP and Flatpack



DS100250-3

Pin Assignment for LCC



DS100250-4

Functional Description

The 'ACTQ841 consists of ten D-type latches with TRI-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition.

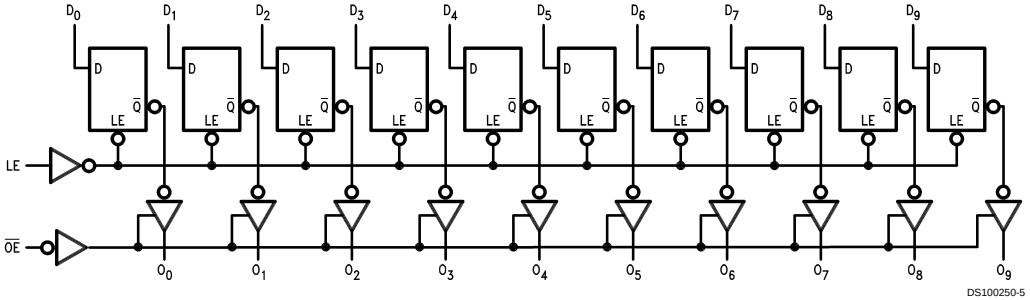
On the LE HIGH-to-LOW transition, the data that meets the setup and hold time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

Function Table

Inputs			Internal	Output	Function
$\overline{OE}$	LE	D	Q	O	
X	X	X	X	Z	High Z
H	H	L	L	Z	High Z
H	H	H	H	Z	High Z
H	L	X	NC	Z	Latched
L	H	L	L	L	Transparent
L	H	H	H	H	Transparent
L	L	X	NC	NC	Latched

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impendance
NC = No Change

Logic Diagram



DS100250-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}) −0.5V to +7.0V
DC Input Diode Current (I_{IK})
V_I = −0.5V −20 mA
V_I = V_{CC} + 0.5V +20 mA
DC Input Voltage (V_I) −0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})
V_O = −0.5V −20 mA
V_O = V_{CC} + 0.5V +20 mA
DC Output Voltage (V_O) −0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O) ±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND}) ±50 mA
Storage Temperature (T_{STG}) −65˚C to +150˚C
DC Latch-Up Source or Sink Current ±300 mA
Junction Temperature (T_J)
CDIP 175˚C

Recommended Operating Conditions

Supply Voltage (V_{CC})
'ACTQ 4.5V to 5.5V
Input Voltage (V_I) 0V to V_{CC}
Output Voltage (V_O) 0V to V_{CC}
Operating Temperature (T_A)
54ACTQ −55˚C to +125˚C
Minimum Input Edge Rate ΔV/Δt
'ACTQ Devices
V_{IN} from 0.8V to 2.0V
V_{CC} @ 4.5V, 5.5V 125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

Note 2: All outputs loaded; thresholds on input associated with output under test.

DC Electrical Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	54ACTQ T_A = −55˚C to +125˚C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.4	V	I_{OUT} = −50 μA
		5.5	5.4		
					(Note 3) V_{IN} = V_{IL} or V_{IH}
		4.5	3.70	V	I_{OH} = −24 mA
		5.5	4.70		I_{OH} = −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.1	V	I_{OUT} = 50 μA
		5.5	0.1		
					(Note 3) V_{IN} = V_{IL} or V_{IH}
		4.5	0.50	V	I_{OL} = −24 mA
		5.5	0.50		I_{OL} = −24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5	±10.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	1.6	mA	V_I = V_{CC} − 2.1V

DC Electrical Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	54ACTQ T_A = −55°C to +125°C Guaranteed Limits	Units	Conditions
I_{OLD}	Minimum Dynamic	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}	Output Current (Note 4)	5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	160.0	µA	V_{IN} = V_{CC} or GND (Note 5)
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.5	V	(Note 6)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−1.2	V	(Note 6)

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

Note 5: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 6: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 7)	54ACTQ T_A = −55°C to +125°C C_L = 50 pF		Units	Fig. No.
			Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay D_n to O_n	5.0	2.0 2.0	9.5 11.0	ns	*Figure 4*
t_{PLH}, t_{PHL}	Propagation Delay LE to O_n	5.0	2.0 2.0	11.0 11.0	ns	*Figure 4*
t_{PZH}, t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	5.0	1.5 1.5	11.0 13.0	ns	*Figure 5*
t_{PHZ}, t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	1.5 1.5	8.5 5.5	ns	*Figure 5*

Note 7: Voltage Range 5.0 is 5.0V ±0.5V.

Note 8: Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design. Not tested.

AC Operating Requirements

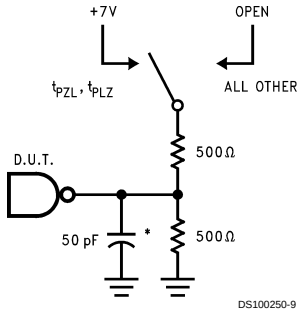
Symbol	Parameter	V_{CC} (V) (Note 9)	54ACTQ T_A = −55°C to +125°C C_L = 50 pF Guaranteed Minimum	Units	Fig. No.
t_S	Setup Time, HIGH or LOW D_n to LE	5.0	3.0	ns	*Figure 7*
t_H	Hold Time, HIGH or LOW D_n to LE	5.0	1.5	ns	*Figure 7*
t_W	LE Pulse Width, HIGH	5.0	4.0	ns	*Figure 6*

Note 9: Voltage Range 5.0 is 5.0V ±0.5V.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	85.0	pF	V_{CC} = 5.0V

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

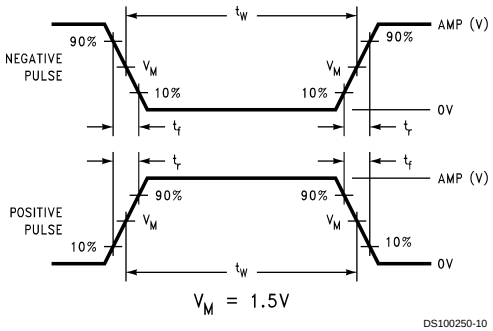


FIGURE 2. Test Input Signal Levels

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

AC Waveforms

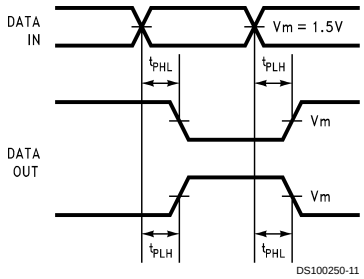


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

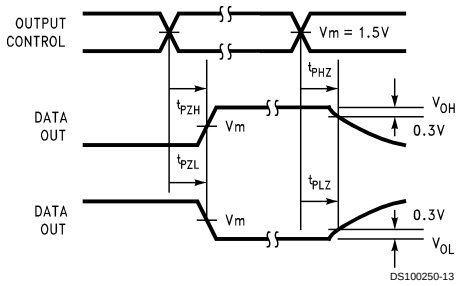


FIGURE 5. TRI-STATE Output HIGH and LOW Enable and Disable Time

AC Waveforms (Continued)

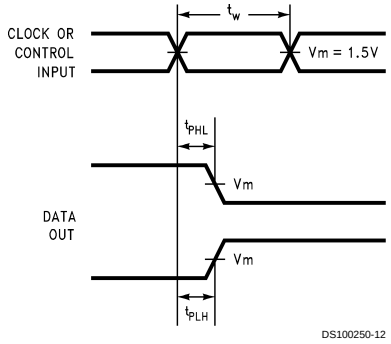


FIGURE 6. Propagation Delay, Pulse Width Waveforms

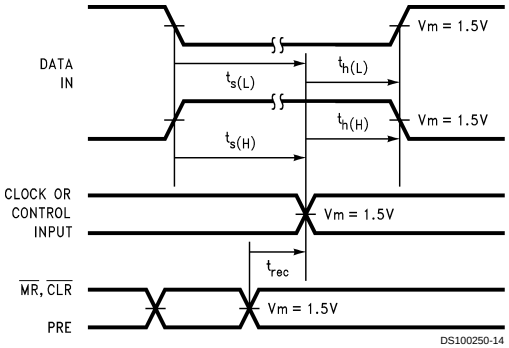
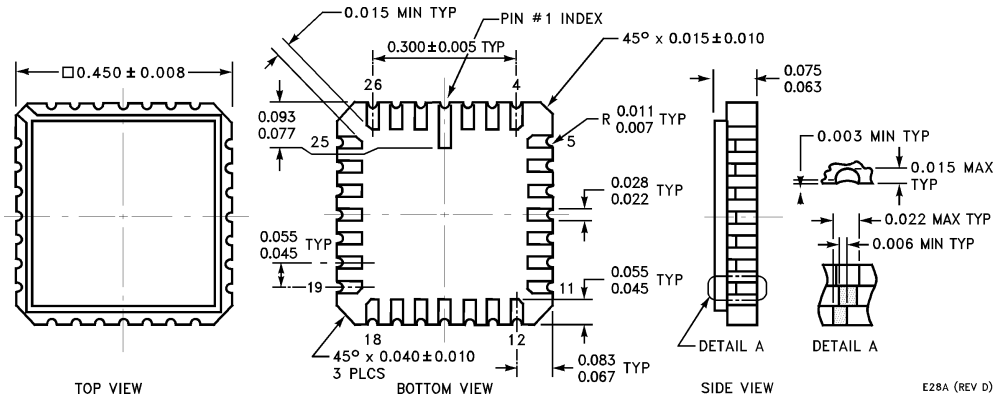
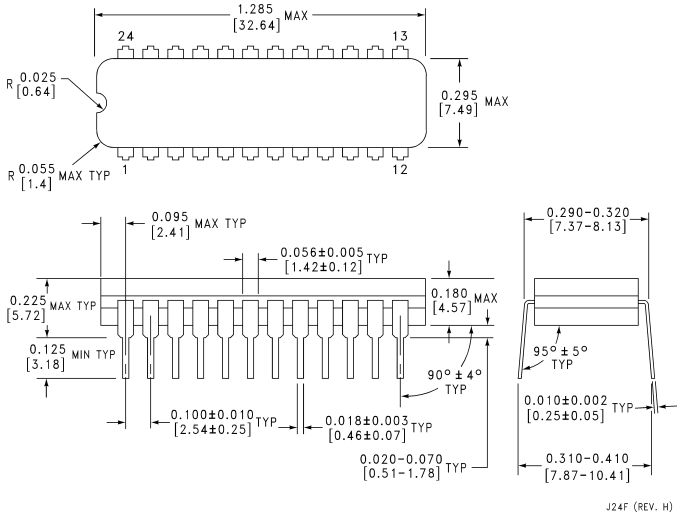


FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

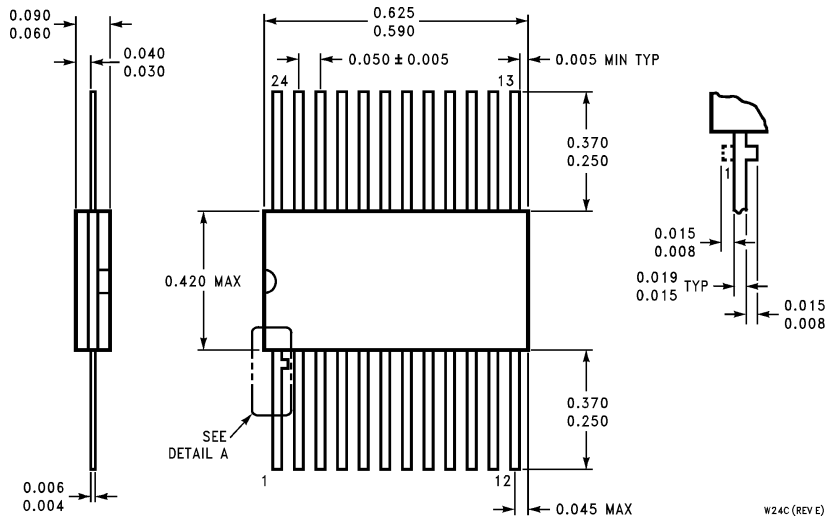


28-Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E28A



24-Lead Slim (0.300" Wide) Ceramic Dual-In-Line Package (SD)
NS Package Number J24F

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Ceramic Flatpak (F)
NS Package Number W24C

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