National Semiconductor

54F/74F175 Quad D Flip-Flop

General Description

The 'F175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, LOW.
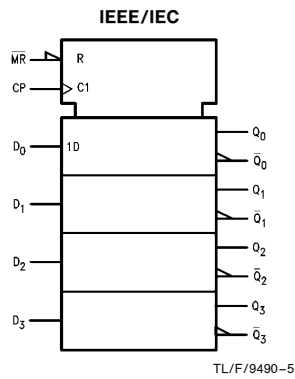
Features

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- Asynchronous common reset
- True and complement output
- Guaranteed 4000V minimum ESD protection

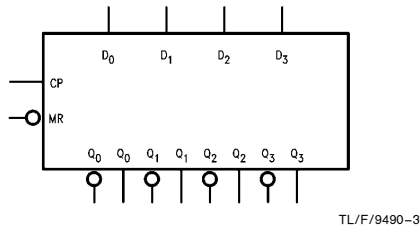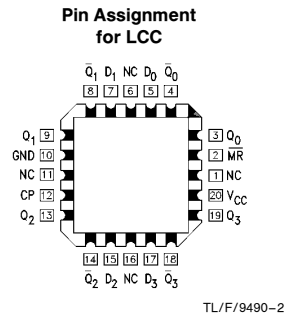| Commercial	Military	Package Number	Package Description
74F175PC		N16E	16-Lead (0.300″ Wide) Molded Dual-In-Line
	54F175DM (Note 2)	J16A	16-Lead Ceramic Dual-In-Line
74F175SC (Note 1)		M16A	16-Lead (0.150″ Wide) Molded Small Outline, JEDEC
74F175SJ (Note 1)		M16D	16-Lead (0.300″ Wide) Molded Small Outline, EIAJ
	54F175FM (Note 2)	W16A	16-Lead Cerpack
	54F175LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13″ reel. Use suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Logic Symbols

IEEE/IEC

TL/F/9490–5

TL/F/9490–3

Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak

TL/F/9490–1

Pin Assignment for LCC

TL/F/9490–2
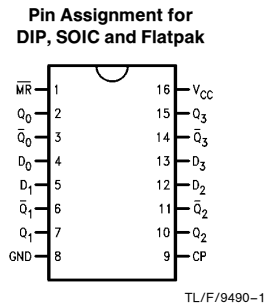
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Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_0–D_3	Data Inputs	1.0/1.0	20 μA/$-$0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/$-$0.6 mA
$\overline{MR}$	Master Reset Input (Active LOW)	1.0/1.0	20 μA/$-$0.6 mA
Q_0–Q_3	True Outputs	50/33.3	$-$1 mA/20 mA
$\overline{Q}_0$–$\overline{Q}_3$	Complement Outputs	50/33.3	$-$1 mA/20 mA

Functional Description

The 'F175 consists of four edge-triggered D flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and $\overline{Q}$ outputs to follow. A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH independent of Clock or Data inputs. The 'F175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

Truth Table

Inputs			Outputs	
$\overline{MR}$	CP	D_n	Q_n	$\overline{Q}_n$
L	X	X	L	H
H	⌐	H	H	L
H	⌐	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition

Logic Diagram
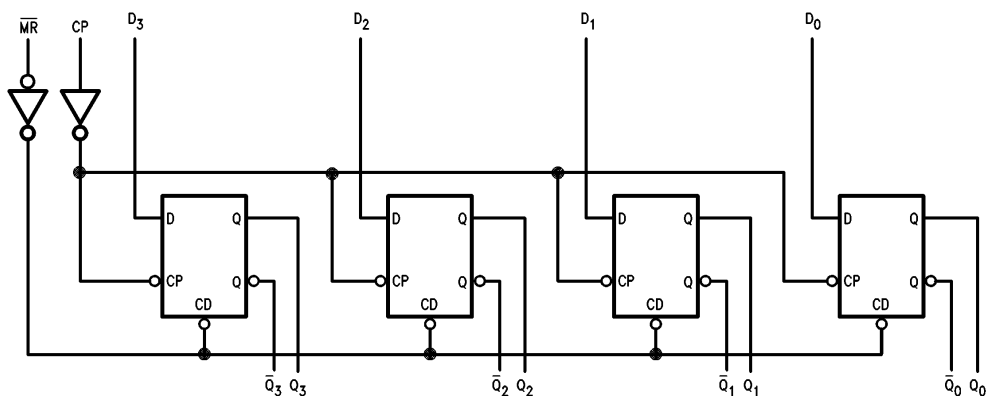
TL/F/9490–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	$-65°C$ to $+150°C$
Ambient Temperature under Bias	$-55°C$ to $+125°C$
Junction Temperature under Bias	$-55°C$ to $+175°C$
Plastic	$-55°C$ to $+150°C$
V_{CC} Pin Potential to	
Ground Pin	$-0.5V$ to $+7.0V$
Input Voltage (Note 2)	$-0.5V$ to $+7.0V$
Input Current (Note 2)	-30 mA to $+5.0$ mA
Voltage Applied to Output	
in HIGH State (with $V_{CC} = 0V$)	
Standard Output	$-0.5V$ to V_{CC}
TRI-STATE® Output	$-0.5V$ to $+5.5V$
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	$-55°C$ to $+125°C$
Commercial	$0°C$ to $+70°C$
Supply Voltage	
Military	$+4.5V$ to $+5.5V$
Commercial	$+4.5V$ to $+5.5V$

DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V_{CC}	Conditions
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				-1.2	V	Min	$I_{IN} = -18$ mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	$I_{OH} = -1$ mA
		74F 10% V_{CC}	2.5					$I_{OH} = -1$ mA
		74F 5% V_{CC}	2.7					$I_{OH} = -1$ mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	$I_{OL} = 20$ mA
		74F 10% V_{CC}			0.5			$I_{OL} = 20$ mA
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	$V_{IN} = 2.7V$
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	$V_{IN} = 7.0V$
		74F			7.0			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	$V_{OUT} = V_{CC}$
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	$I_{ID} = 1.9$ μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	$V_{IOD} = 150$ mV All Other Pins Grounded
I_{IL}	Input LOW Current				-0.6	mA	Max	$V_{IN} = 0.5V$
I_{OS}	Output Short-Circuit Current		-60		-150	mA	Max	$V_{OUT} = 0V$
I_{CC}	Power Supply Current			22.5	34.0	mA	Max	$CP = \diagup$ $D_n = \overline{MR} = HIGH$

AC Electrical Characteristics

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			54F $T_A, V_{CC} = $ Mil $C_L = 50$ pF		74F $T_A, V_{CC} = $ Com $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	100	140		80		100		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n or $\overline{Q}_n$	4.0 4.0	5.0 6.5	6.5 8.5	3.5 4.0	8.5 10.5	4.0 4.0	7.5 9.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	4.5	9.0	11.5	4.5	15.0	4.5	13.0	ns
t_{PLH}	Propagation Delay $\overline{MR}$ to $\overline{Q}_n$	4.0	6.5	8.0	4.0	10.0	4.0	9.0	ns

AC Operating Requirements

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		54F $T_A, V_{CC} = $ Mil		74F $T_A, V_{CC} = $ Com		Units
		Min	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to CP	3.0 3.0		3.0 3.0		3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to CP	1.0 1.0		1.0 2.0		1.0 1.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	4.0 5.0		4.0 5.0		4.0 5.0		ns
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW	5.0		5.0		5.0		ns
t_{rec}	Recovery Time, $\overline{MR}$ to CP	5.0		5.0		5.0		ns

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Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

74F 175 S C X

Temperature Range Family
74F = Commercial
54F = Military

Device Type

Package Code
P = Plastic DIP
D = Ceramic DIP
F = Flatpak
L = Leadless Chip Carrier (LCC)
S = Small Outline SOIC JEDEC
SJ = Small Outline SOIC EIAJ

Special Variations
QB = Military grade device with environmental and burn-in processing
X = Devices shipped in 13″ reel

Temperature Range
C = Commercial (0°C to +70°C)
M = Military (−55°C to +125°C)

Physical Dimensions inches (millimeters)

0.350 ± 0.008
(8.890 ± 0.203)

$\dfrac{0.063 - 0.075}{(1.600 - 1.905)}$

Top View

Side View

DETAIL A

$\dfrac{0.200 \pm 0.005}{(5.080 \pm 0.127)}$ TYP

$45° \times \dfrac{0.015 \pm 0.010}{(0.381 \pm 0.254)}$

$\dfrac{0.015}{(0.381)}$ MIN TYP

$\dfrac{0.007 - 0.011}{(0.178 - 0.279)}$ R TYP

$\dfrac{0.022 - 0.028}{(0.559 - 0.711)}$ TYP

$\dfrac{0.077 - 0.093}{(1.959 - 2.362)}$

PIN #1 INDEX

$\dfrac{0.045 - 0.055}{(1.143 - 1.397)}$ TYP

$\dfrac{0.067 - 0.083}{(1.702 - 2.108)}$ TYP

$\dfrac{0.045 - 0.055}{(1.143 - 1.397)}$ TYP

$45° \times \dfrac{0.040 \pm 0.010}{(1.016 \pm 0.254)}$ 3 PLCS

Bottom View

$\dfrac{0.003}{(0.076)}$ MIN TYP

$\dfrac{0.015}{(0.381)}$ MAX TYP

$\dfrac{0.022}{(0.559)}$ MAX TYP

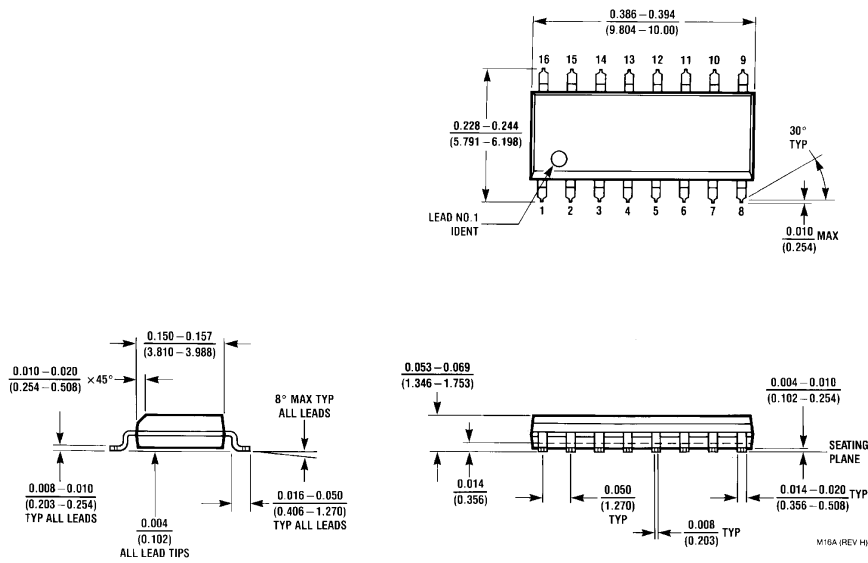$\dfrac{0.006}{(0.152)}$ MIN TYP

Detail A

E20A (REV D)

20-Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A
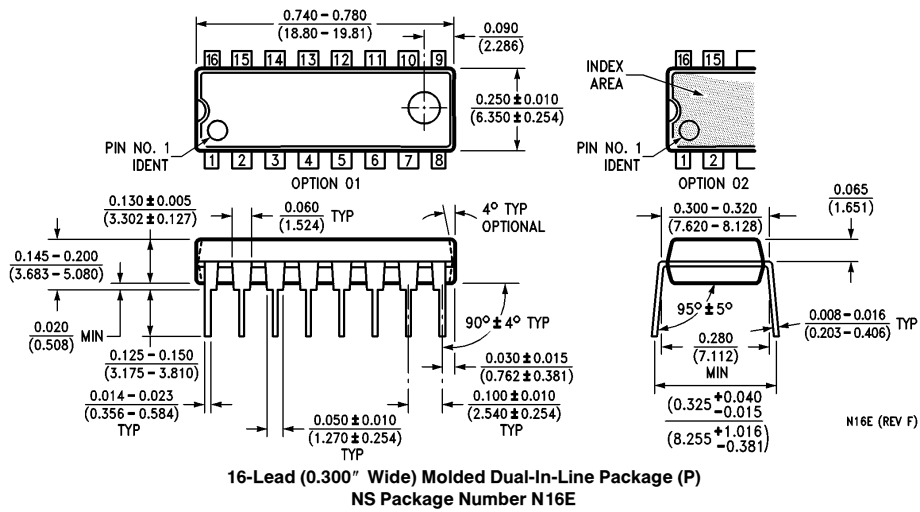
Physical Dimensions inches (millimeters) (Continued)
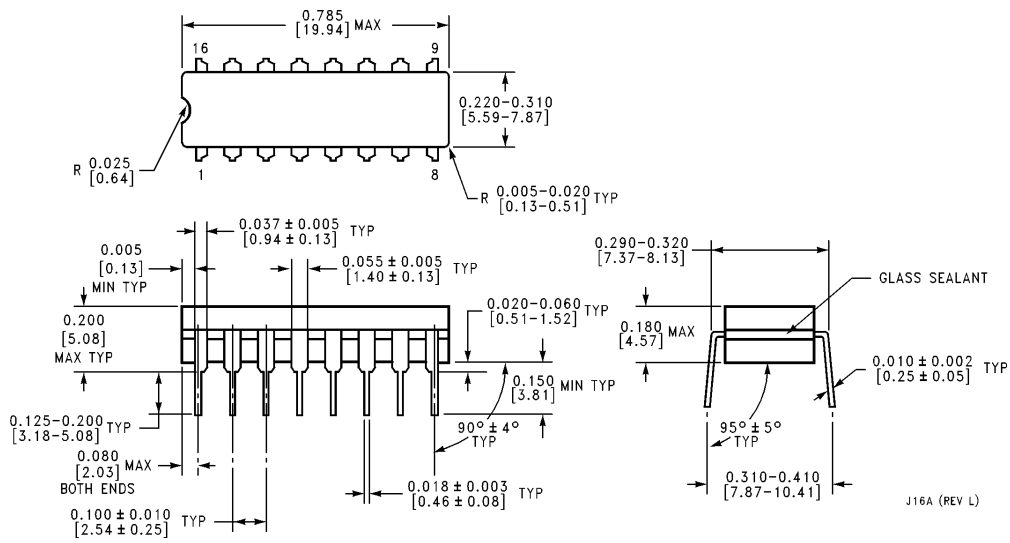
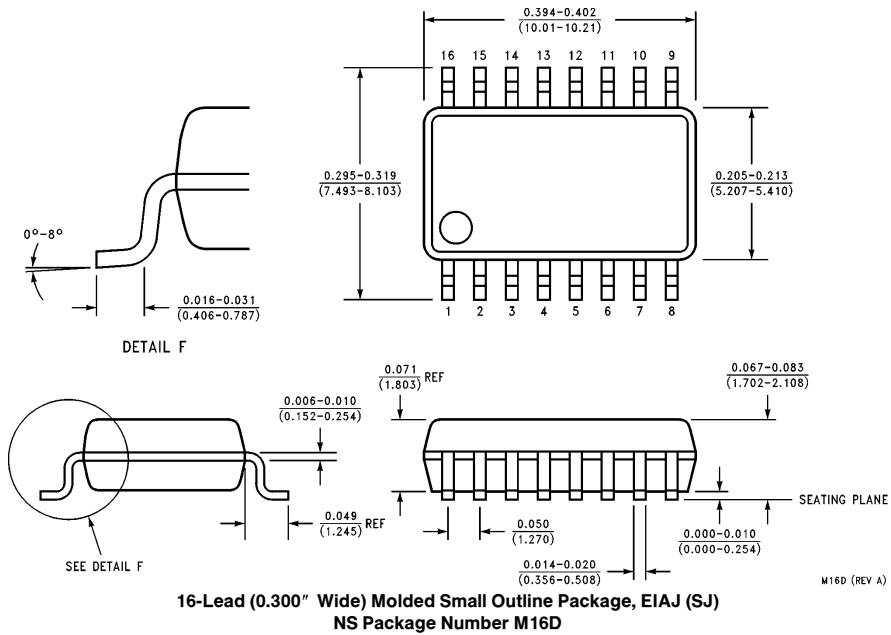**16-Lead Ceramic Dual-In-Line Package (D)**
NS Package Number J16A

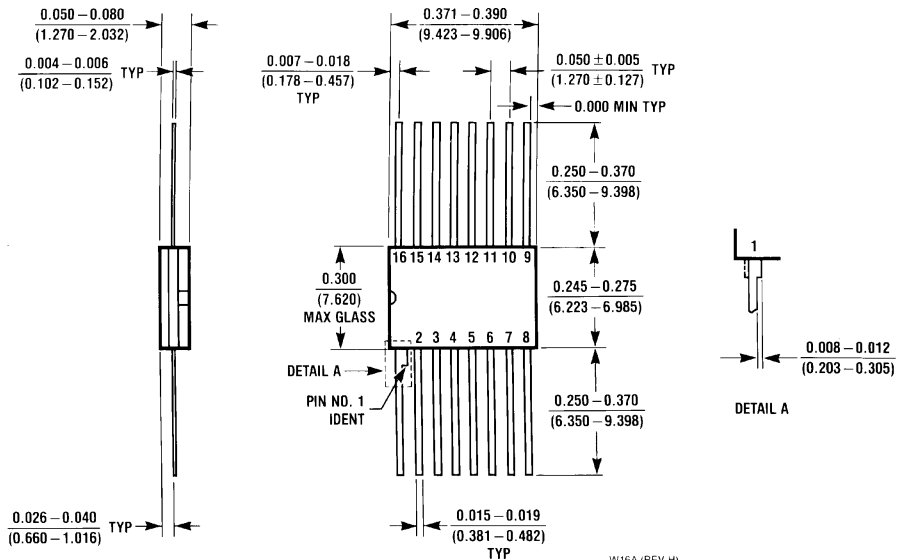J16A (REV L)

16-Lead (0.150″ Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M16A

M16A (REV H)

$\frac{0.394-0.402}{(10.01-10.21)}$

16 15 14 13 12 11 10 9

1 2 3 4 5 6 7 8

$\frac{0.295-0.319}{(7.493-8.103)}$

$\frac{0.205-0.213}{(5.207-5.410)}$

0°–8°

$\frac{0.016-0.031}{(0.406-0.787)}$

DETAIL F

$\frac{0.071}{(1.803)}$ REF

$\frac{0.067-0.083}{(1.702-2.108)}$

$\frac{0.006-0.010}{(0.152-0.254)}$

$\frac{0.049}{(1.245)}$ REF

$\frac{0.050}{(1.270)}$

SEE DETAIL F

$\frac{0.014-0.020}{(0.356-0.508)}$

$\frac{0.000-0.010}{(0.000-0.254)}$

SEATING PLANE

M16D (REV A)

16-Lead (0.300″ Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M16D

$\frac{0.740-0.780}{(18.80-19.81)}$

$\frac{0.090}{(2.286)}$

16 15 14 13 12 11 10 9

1 2 3 4 5 6 7 8

PIN NO. 1
IDENT

OPTION 01

$\frac{0.250\pm0.010}{(6.350\pm0.254)}$

INDEX
AREA

16 15

1 2

PIN NO. 1
IDENT

OPTION 02

$\frac{0.130\pm0.005}{(3.302\pm0.127)}$

$\frac{0.060}{(1.524)}$ TYP

4° TYP
OPTIONAL

$\frac{0.145-0.200}{(3.683-5.080)}$

$\frac{0.020}{(0.508)}$ MIN

$\frac{0.125-0.150}{(3.175-3.810)}$

$\frac{0.014-0.023}{(0.356-0.584)}$ TYP

$\frac{0.050\pm0.010}{(1.270\pm0.254)}$ TYP

90°±4° TYP

$\frac{0.030\pm0.015}{(0.762\pm0.381)}$

$\frac{0.100\pm0.010}{(2.540\pm0.254)}$ TYP

$\frac{0.300-0.320}{(7.620-8.128)}$

$\frac{0.065}{(1.651)}$

95°±5°

$\frac{0.280}{(7.112)}$ MIN

$\frac{0.008-0.016}{(0.203-0.406)}$ TYP

$\frac{(0.325^{+0.040}_{-0.015})}{(8.255^{+1.016}_{-0.381})}$

N16E (REV F)

16-Lead (0.300″ Wide) Molded Dual-In-Line Package (P)
NS Package Number N16E

7

Physical Dimensions inches (millimeters) (Continued)

$\dfrac{0.050-0.080}{(1.270-2.032)}$

$\dfrac{0.004-0.006}{(0.102-0.152)}$ TYP

$\dfrac{0.007-0.018}{(0.178-0.457)}$ TYP

$\dfrac{0.371-0.390}{(9.423-9.906)}$

$\dfrac{0.050\pm0.005}{(1.270\pm0.127)}$ TYP

0.000 MIN TYP

$\dfrac{0.250-0.370}{(6.350-9.398)}$

16 15 14 13 12 11 10 9

$\dfrac{0.300}{(7.620)}$ MAX GLASS

$\dfrac{0.245-0.275}{(6.223-6.985)}$

2 3 4 5 6 7 8

DETAIL A

PIN NO. 1 IDENT

$\dfrac{0.250-0.370}{(6.350-9.398)}$

$\dfrac{0.026-0.040}{(0.660-1.016)}$ TYP

$\dfrac{0.015-0.019}{(0.381-0.482)}$ TYP

W16A (REV H)

1

$\dfrac{0.008-0.012}{(0.203-0.305)}$

DETAIL A

16 Lead Ceramic Flatpak (F)
NS Package Number W16A

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