

## 54F/74F646 • 74F646B • 54F/74F648 Octal Transceiver/Register with TRI-STATE® Outputs

### General Description

These devices consist of bus transceiver circuits with TRI-STATE, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Control  $\bar{G}$  and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control  $\bar{G}$  is Active LOW. In the isolation mode (control  $\bar{G}$  HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

### Features

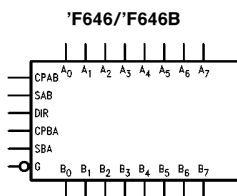
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- 'F648 has inverting data paths
- 'F646/'F646B have non-inverting data paths
- 'F646B is a faster version of the 'F646
- TRI-STATE outputs
- 300 mil slim DIP
- Guaranteed 4000V minimum ESD protection

Commercial	Military	Package Number	Package Description
74F646SPC		N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
	54F646DM (Note 2)	J24F	24-Lead (0.300" Wide) Ceramic Dual-In-Line
74F646SC (Note 1)		M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F646MSA (Note 1)		MSA24	24-Lead Molded Shrink Small Outline, EIAJ, Type II
	54F646FM (Note 2)	W24C	24-Lead Cerpack
	54F646LM (Note 2)	E28A	28-Lead Ceramic Leadless Chip Carrier, Type C
74F646BSPC		N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
74F646BSC (Note 1)		M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F648SPC		N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
	54F648SDM (Note 2)	J24F	24-Lead (0.300" Wide) Ceramic Dual-In-Line
74F648SC (Note 1)		M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC
	54F648FM (Note 2)	W24C	24-Lead Cerpack
	54F648LM (Note 2)	E28A	28-Lead Ceramic Leadless Chip Carrier, Type C

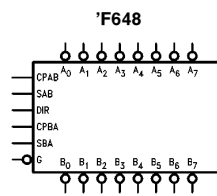
**Note 1:** Devices also available in 13" reel. Use suffix = SCX.

**Note 2:** Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

### Logic Symbols



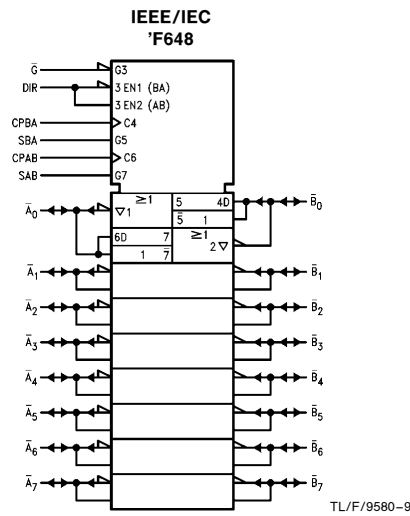
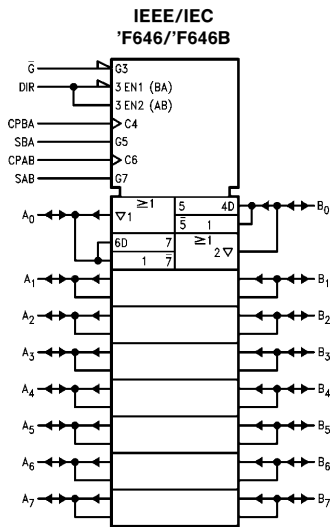
TL/F/9580-1



TL/F/9580-7

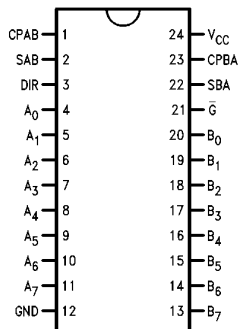
TRI-STATE® is a registered trademark of National Semiconductor Corporation.

## Logic Symbols (Continued)

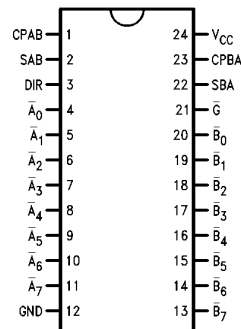


## Connection Diagrams

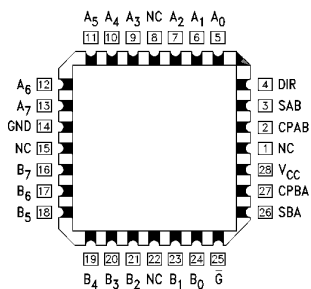
**Pin Assignment  
for DIP, SOIC and Flatpak  
'F646/'F646B**



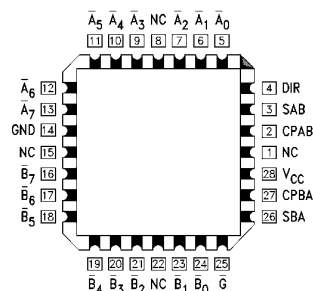
**Pin Assignment  
for DIP, SOIC and Flatpak  
'F648**



**Pin Assignment  
for LCC  
'F646/'F646B**









**Pin Assignment  
for LCC  
'F648**




## Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
A <sub>0</sub> –A <sub>7</sub>	Data Register A Inputs/ TRI-STATE Outputs	3.5/1.083 600/106.6 (80)	70 $\mu$ A / –650 $\mu$ A –12 mA/64 mA (48 mA)
B <sub>0</sub> –B <sub>7</sub>	Data Register B Inputs/ TRI-STATE Outputs	3.5/1.083 600/106.6 (80)	70 $\mu$ A / –650 $\mu$ A –12 mA/64 mA (48 mA)
CPAB, CPBA	Clock Pulse Inputs	1.0/1.0	20 $\mu$ A / –0.6 mA
SAB, SBA	Select Inputs	1.0/1.0	20 $\mu$ A / –0.6 mA
$\overline{G}$	Output Enable Input	1.0/1.0	20 $\mu$ A / –0.6 mA
DIR	Direction Control Input	1.0/1.0	20 $\mu$ A / –0.6 mA

Function Table

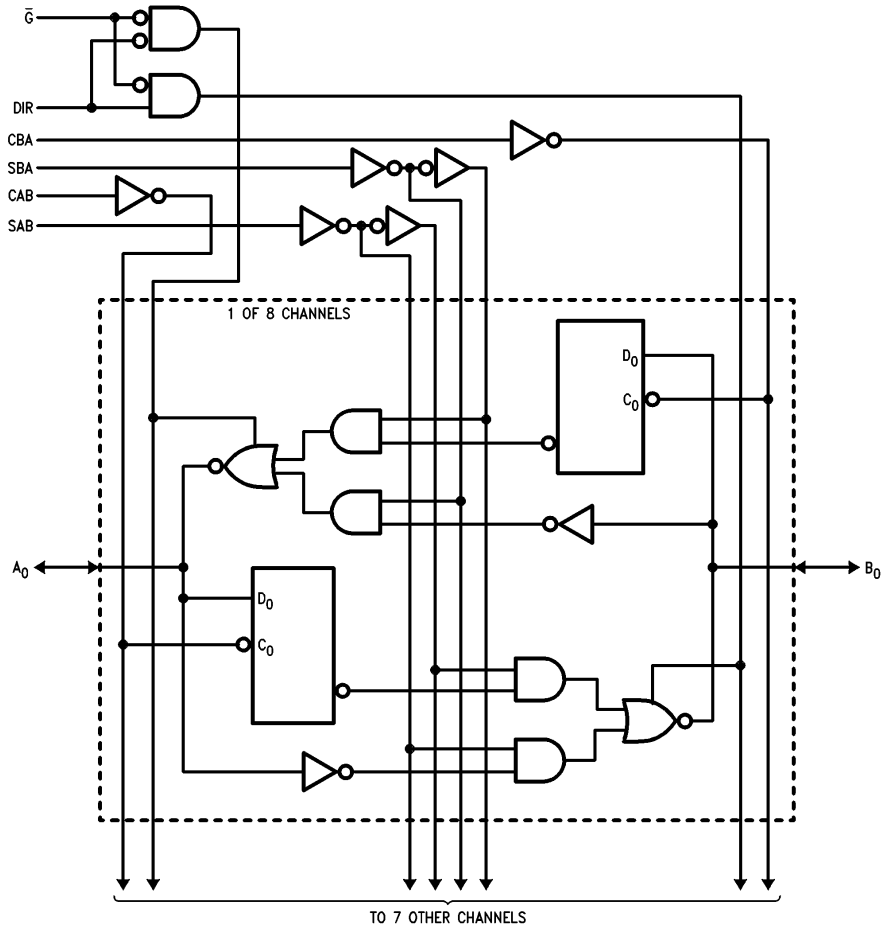
Inputs						Data I/O*		Function
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A <sub>0</sub> –A <sub>7</sub>	B <sub>0</sub> –B <sub>7</sub>	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X		X	X	X			Clock A <sub>n</sub> Data into A Register
H	X	X		X	X			Clock B <sub>n</sub> Data into B Register
L	H	X	X	L	X	Input	Output	A <sub>n</sub> to B <sub>n</sub> —Real Time (Transparent Mode)
L	H		X	L	X			Clock A <sub>n</sub> Data into A Register
L	H	H or L	X	H	X			A Register to B <sub>n</sub> (Stored Mode)
L	H		X	H	X			Clock A <sub>n</sub> Data into A Register and Output to B <sub>n</sub>
L	L	X	X	X	L	Output	Input	B <sub>n</sub> to A <sub>n</sub> —Real Time (Transparent Mode)
L	L	X		X	L			Clock B <sub>n</sub> Data into B Register
L	L	X	H or L	X	H			B Register to A <sub>n</sub> (Stored Mode)
L	L	X		X	H			Clock B <sub>n</sub> Data into B Register and Output to A <sub>n</sub>

\*The data output functions may be enabled or disabled by various signals at the  $\overline{G}$  and DIR Inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Irrelevant  
 = LOW-to-HIGH Transition

**Logic Diagrams** (Continued)

'F646/'F646B

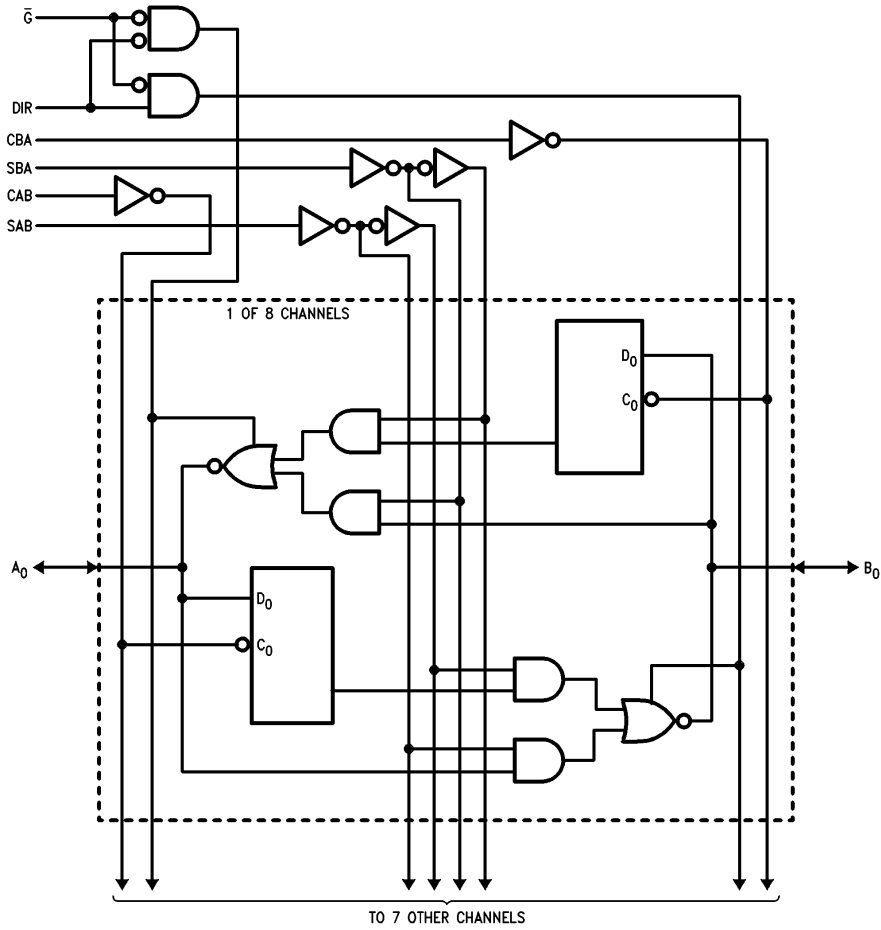


TL/F/9580-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Logic Diagrams** (Continued)

'F648



TL/F/9580-6

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	–55°C to +175°C
Plastic	–55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V
Input Current (Note 2)	–30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	–0.5V to V <sub>CC</sub>
TRI-STATE Output	–0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	–55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage	–1.2			V	Min	I <sub>IN</sub> = –18 mA (Non I/O Pins)
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>	2.0 2.0		V	Min	I <sub>OH</sub> = –12 mA (A <sub>n</sub> , B <sub>n</sub> ) I <sub>OH</sub> = –15 mA (A <sub>n</sub> , B <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>	0.55 0.55		V	Min	I <sub>OL</sub> = 48 mA (A <sub>n</sub> , B <sub>n</sub> ) I <sub>OL</sub> = 64 mA (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current	54F 74F	20.0 5.0		μA	Max	V <sub>IN</sub> = 2.7V (Non I/O Pins)
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F	100 7.0		μA	Max	V <sub>IN</sub> = 7.0V (Non I/O Pins)
I <sub>BVIT</sub>	Input HIGH Current Breakdown (I/O)	54F 74F	1.0 0.5		mA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F	250 50		μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F	3.75		μA	0.0	V <sub>ID</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current				mA	Max	V <sub>IN</sub> = 0.5V (Non I/O Pins)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current				μA	Max	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current				μA	Max	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current	–100		–225	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test				μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current				mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current				mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current				mA	Max	V <sub>O</sub> = HIGH Z

## 'F646/'F648

### AC Electrical Characteristics

Symbol	Parameter	74F		54F		74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Max	Min	Max	Min	Max	
$f_{\text{max}}$	Maximum Clock Frequency	90		75		90		MHz
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay Clock to Bus	2.0 2.0	7.0 8.0	2.0 2.0	8.5 9.5	2.0 2.0	8.0 9.0	ns
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay Bus to Bus ('F646)	1.0 1.0	7.0 6.5	1.0 1.0	8.0 8.0	1.0 1.0	7.5 7.0	ns
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay Bus to Bus ('F648)	2.0 1.0	8.5 7.5	1.0 1.0	10.0 9.0	2.0 1.0	9.0 8.0	ns
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay SBA or SAB to A or B	2.0 2.0	8.5 8.0	2.0 2.0	11.0 10.0	2.0 2.0	9.5 9.0	ns
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Enable Time $\text{OE}$ to A or B	2.0 2.0	8.5 12.0	2.0 2.0	10.0 13.5	2.0 2.0	9.0 12.5	ns
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Disable Time $\text{OE}$ to A or B	1.0 2.0	7.5 9.0	1.0 2.0	9.0 11.0	1.0 2.0	8.5 9.5	ns
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Enable Time DIR to A or B	2.0 2.0	14.0 13.0	2.0 2.0	16.0 15.0	2.0 2.0	15.0 14.0	ns
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Disable Time DIR to A or B	1.0 2.0	9.0 11.0	1.0 2.0	10.0 12.0	1.0 2.0	9.5 11.5	ns

## 'F646/'F648

### AC Operating Requirements

Symbol	Parameter	74F		54F		74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$		
		Min	Max	Min	Max	Min	Max	
$t_{\text{s}}(\text{H})$ $t_{\text{s}}(\text{L})$	Setup Time, HIGH or LOW Bus to Clock	5.0 5.0		5.0 5.0		5.0 5.0		ns
$t_{\text{h}}(\text{H})$ $t_{\text{h}}(\text{L})$	Hold Time, HIGH or LOW Bus to Clock	2.0 2.0		2.5 2.5		2.0 2.0		ns
$t_{\text{w}}(\text{H})$ $t_{\text{w}}(\text{L})$	Clock Pulse Width HIGH or LOW	5.0 5.0		5.0 5.0		5.0 5.0		ns

## 'F646B

### AC Electrical Characteristics

Symbol	Parameter	74F		54F		74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Max	Min	Max	Min	Max	
$f_{\text{max}}$	Maximum Clock Frequency	165				150		MHz
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay Clock to Bus	2.5 3.0	7.0 7.5			2.5 3.0	8.0 8.0	ns
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay Bus to Bus	2.0 2.0	6.0 6.0			2.0 2.0	7.0 7.0	ns
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay SBA or SAB to A or B	2.5 2.5	7.5 7.5			2.5 2.5	8.5 8.5	ns
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Enable Time OE to A or B	2.5 2.5	6.5 9.0			2.5 2.5	8.0 10.0	ns
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Disable Time OE to A or B	1.5 2.0	6.5 7.0			1.5 2.0	7.5 8.5	ns
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Enable Time DIR to A or B	2.0 3.0	7.0 9.5			2.0 3.0	8.5 10.0	ns
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Disable Time DIR to A or B	1.5 2.5	7.5 8.5			1.5 2.5	8.5 9.5	ns

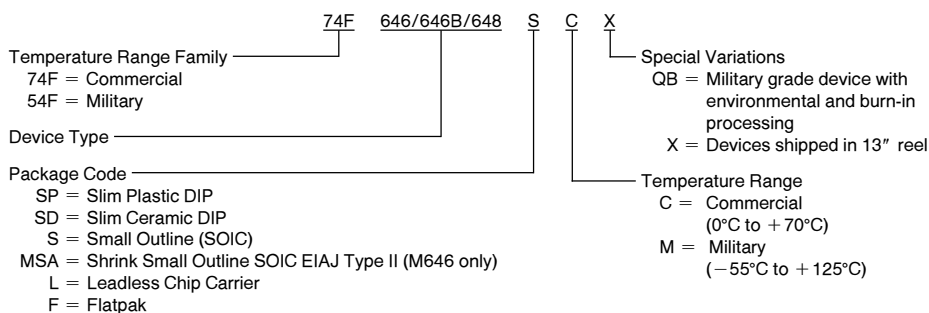
## 'F646B

### AC Operating Requirements

Symbol	Parameter	74F		54F		74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$		
		Min	Max	Min	Max	Min	Max	
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW Bus to Clock	5.0 5.0				4.0 4.0		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW Bus to Clock	1.5 1.5				1.5 1.5		ns
$t_w(\text{H})$ $t_w(\text{L})$	Clock Pulse Width HIGH or LOW	5.0 5.0				5.0 5.0		ns

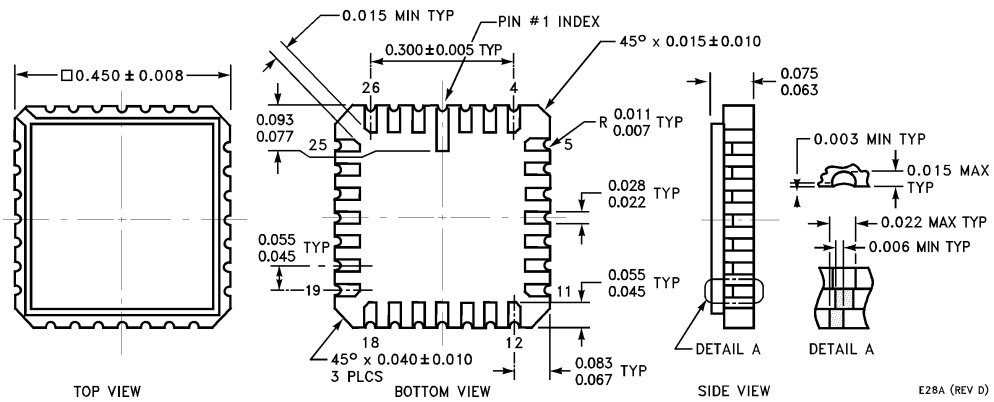
### Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

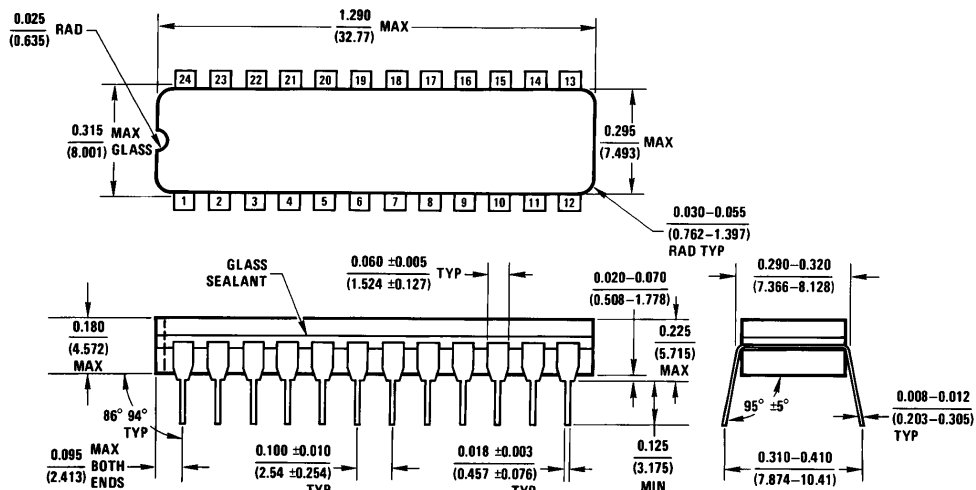




**Physical Dimensions** inches (millimeters)

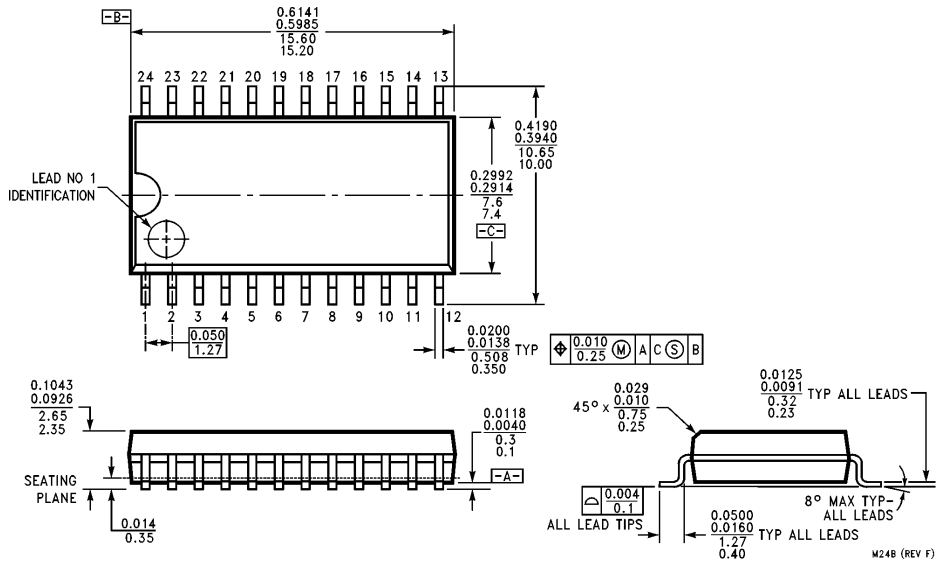


**28-Lead Ceramic Leadless Chip Carrier, Type C**  
NS Package Number E28A



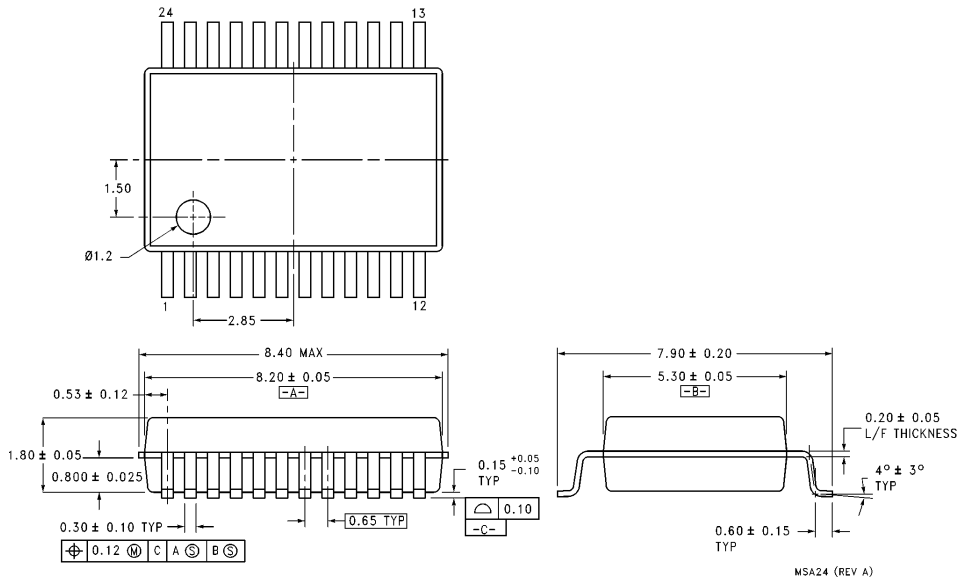
**24-Lead (0.300" Wide) Ceramic Dual-In-Line Package (SD)**  
NS Package Number J24F

**Physical Dimensions** inches (millimeters) (Continued)

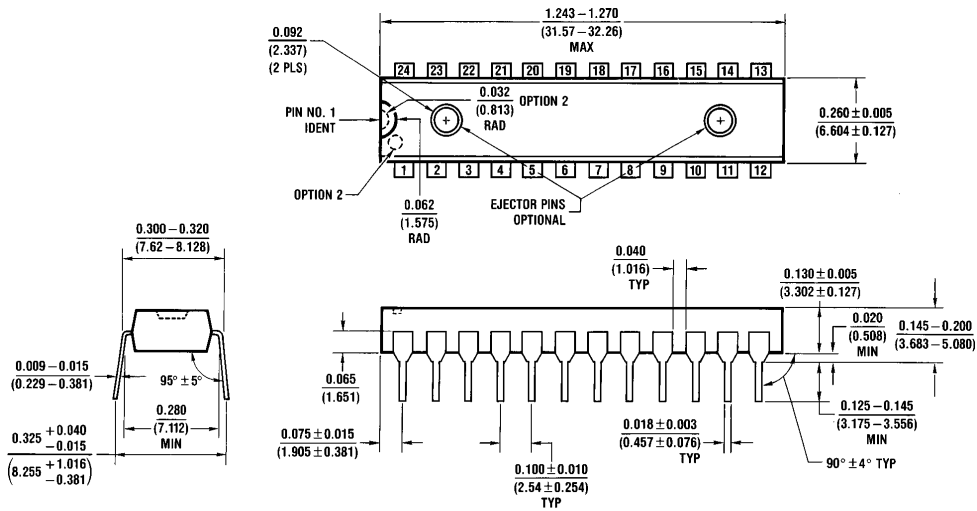


**24-Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)  
NS Package Number M24B**

**Physical Dimensions** inches (millimeters) (Continued)

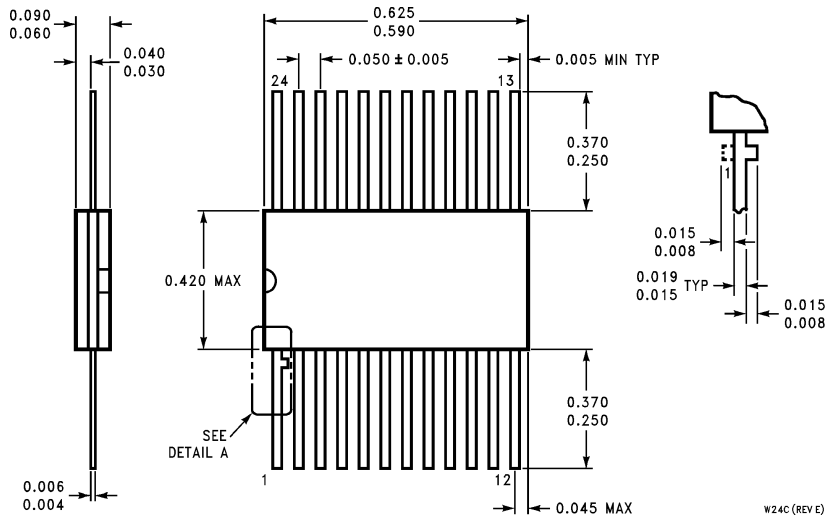


**24-Lead Molded Shrink Small Outline Package, EIAJ, Type II**  
NS Package Number MSA24



**24-Lead (0.300" Wide) Molded Dual-In-Line Package (SP)**  
NS Package Number N24C

**Physical Dimensions** inches (millimeters) (Continued)



**24-Lead Cerpack  
NS Package Number W24C**

W24C (REV E)

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