

54FCT521 8-Bit Identity Comparator

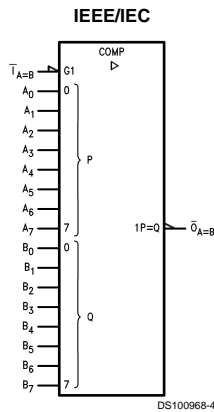
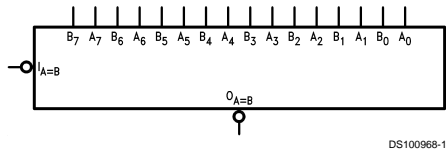
General Description

The 54FCT521 is an expandable 8-bit comparator. It compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. The expansion input $\bar{T}_{A=B}$ also serves as an active LOW enable input.

Features

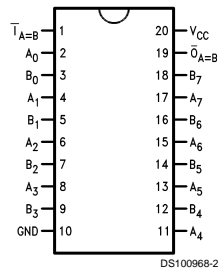
- Expandable to any word length
- Outputs sink capability of 32mA, source capability of 12 mA
- TTL input and output level compatible
- CMOS power consumption
- Standard microcircuit Drawing (SMD) 5962-8854301

Logic Symbols

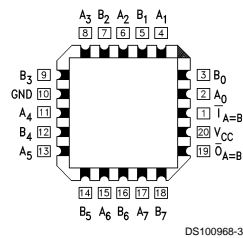


Connection Diagram

Pin Assignment for DIP and CERPACK



Pin Assignment for LCC



Pin Descriptions

Pin Names	Description
A ₀ -A ₇	Word A Inputs
B ₀ -B ₇	Word B Inputs
T _{A=B}	Expansion or Enable Input
$\bar{O}_{A=B}$	Identity Output

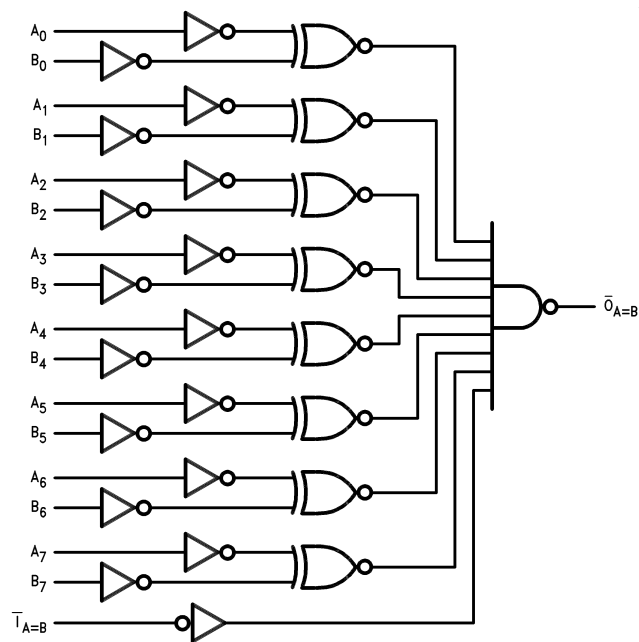
Truth Table

Inputs		Outputs
$\bar{i}_{A=B}$	A, B	$\bar{O}_{A=B}$
L	A = B (Note 1)	L
L	A \neq B	H
H	A = B (Note 1)	H
H	A \neq B	H

H = HIGH Voltage Level
L = LOW Voltage Level

Note 1: $A_0 = B_0, A_1 = B_1, A_2 = B_2$, etc.

Logic Diagram



DS100968-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	± 50 mA

Storage Temperature (T_{STG})	-65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
FCT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54FCT	-55°C to +125°C

Note 2: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for 'FCT Family Devices

Symbol	Parameter	54FCT		Units	V_{CC}	Conditions
		Min	Max			
V_{IH}	Input HIGH Voltage	2.0		V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage		0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage		-1.2	V	Min	$I_{IN} = -18$ mA
V_{OH}	Output HIGH Voltage	54FCT	4.3	V	Min	$I_{OH} = -300$ μ A
		54FCT	2.4	V	Min	$I_{OH} = -12$ mA
V_{OL}	Output LOW Voltage	54FCT	0.2	V	Min	$I_{OL} = 300$ μ A
		54FCT	0.5	V	Min	$I_{OL} = 32$ mA
I_{IH}	Input HIGH Current		5	μ A	Max	$V_{IN} = V_{CC}$
I_{IL}	Input LOW Current		-5	μ A	Max	$V_{IN} = 0.0V$
I_{OS}	Output Short-Circuit Current		-60	mA	Max	$V_{OUT} = 0.0V$
I_{CCQ}	Quiescent Power Supply Current		1.5	mA	Max	$V_{IN} < 0.2V$ or $V_{IN} = 5.3V$, $V_{CC} = 5.5V$
ΔI_{CC}	Quiescent Power Supply Current		2.0	mA	Max	$V_I = V_{CC} - 2.1V$
I_{CCD}	Dynamic I_{CC}		0.25	mA/ MHz	Max	$V_{CC} = 5.5V$, Outputs Open, One Bit Toggling, 50% Duty Cycle, $\overline{OE}_n = GND$
I_{CC}	Total Power Supply Current		5.0	mA	Max	$V_{CC} = 5.5V$, Outputs Open, $f_l = 10MHz$, $\overline{OE}_n = GND$, One Bit Toggling, 50% Duty Cycle

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics for 'FCT Family Devices

Symbol	Parameter	V _{CC} (V) (Note 5)	T _A = -55°C to +125°C C _L = 50 pF		Units
			Min	Max	
t _{PLH}	Propagation Delay A _n or B _n to $\overline{O}_{A=B}$	5.0	1.5	15.0	ns
t _{PHL}	Propagation Delay A _n or B _n to $\overline{O}_{A=B}$	5.0	1.5	15.0	ns
t _{PLH}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	5.0	1.5	9.0	ns
t _{PHL}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	5.0	1.5	9.0	ns

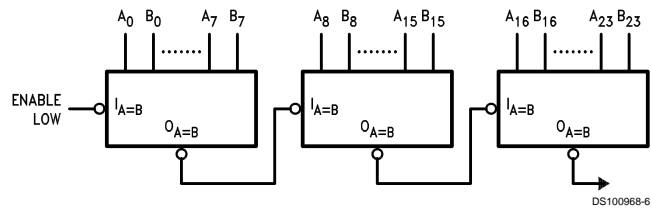
Note 5: Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

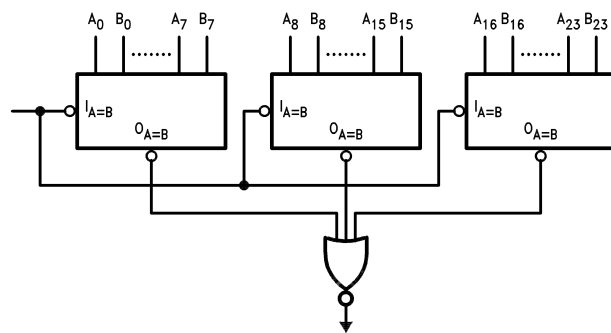
Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	40	pF	V _{CC} = 5.0V

Applications

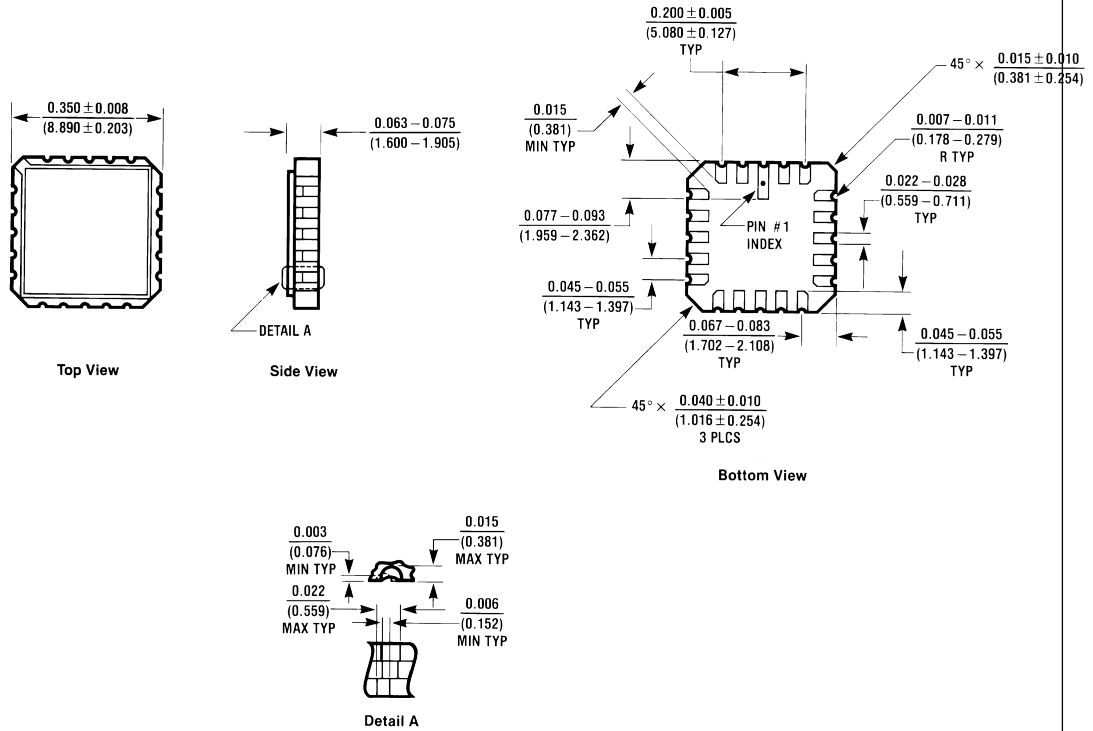
Ripple Expansion



Parallel Expansion



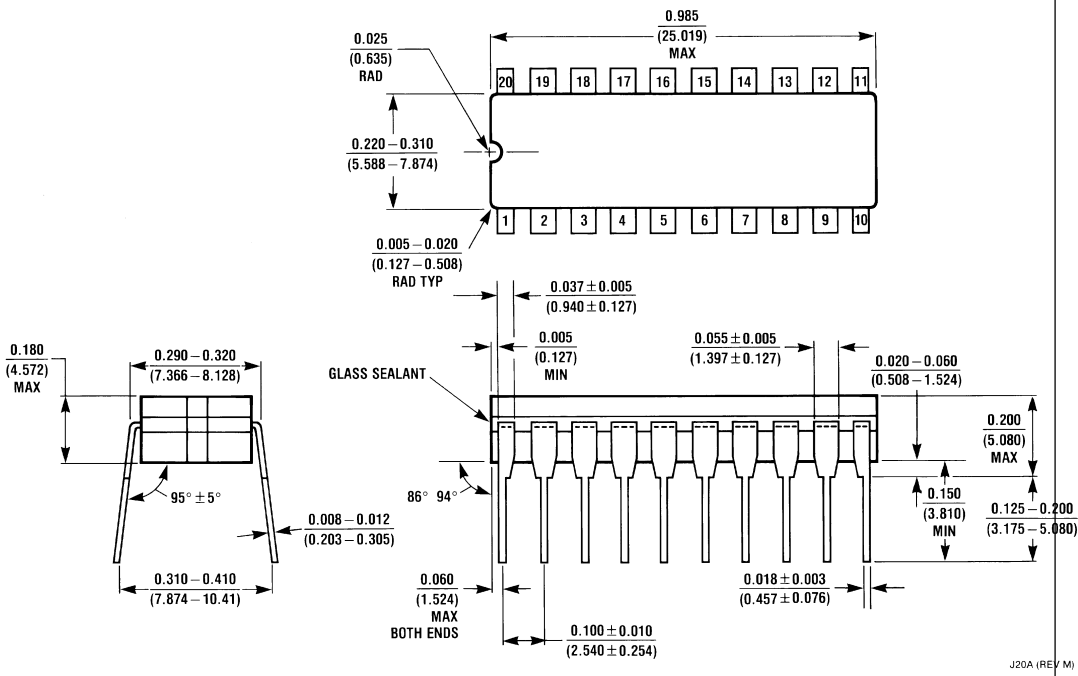
Physical Dimensions inches (millimeters) unless otherwise noted



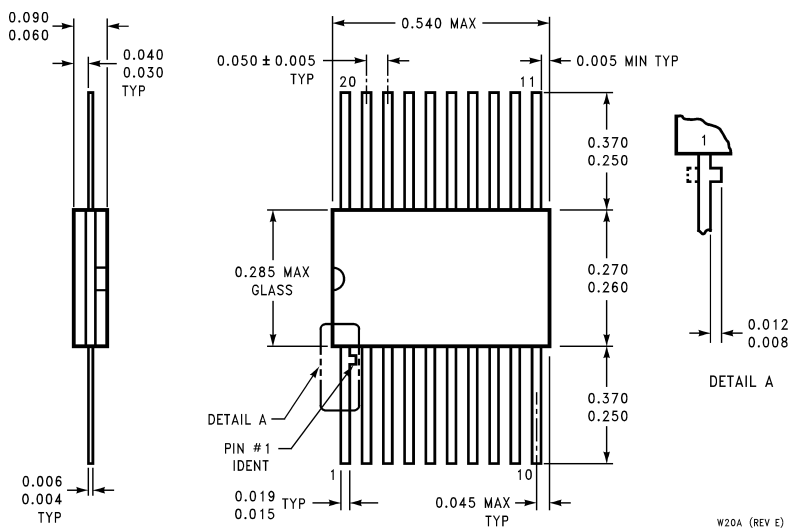
**20-Lead Ceramic Leadless Chip Carrier
Package Number E20A**

E20A (REV D)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Ceramic Dual-in-line
J20A**



**20-Lead Cerpack
Package Number W20A**

J20A (REV M)

W20A (REV E)

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