National Semiconductor

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54FCT533
Octal Transparent Latch with TRI-STATE® Outputs

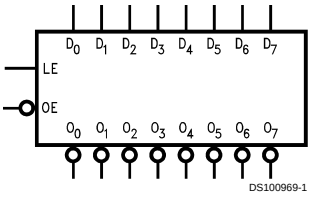
General Description

The FCT533 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is low, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the bus output is in the high impedance state.

Features

- Eight latches in a single package
- TTL input and output level compatible
- CMOS power consumption
- TRI-STATE outputs drive bus lines or buffer memory address registers
- Output sink capability of 32mA, source capability of 12 mA
- Inverted version of the FCT373
- Standard Microcircuit Drawing (SMD) 5962-8865101

Logic Symbols



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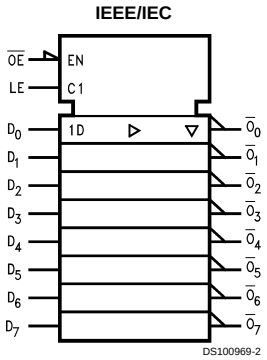

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Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	TRI-STATE Latch Outputs

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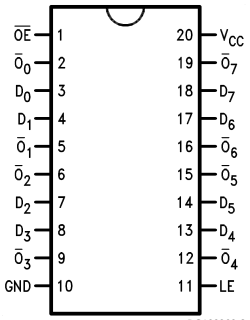
Connection Diagrams

Pin Assignment for DIP and Flatpak



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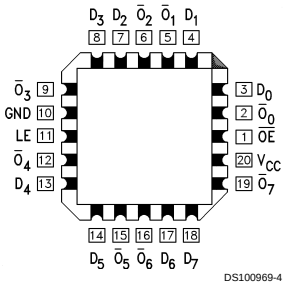
Pin Assignment for LCC



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Functional Description

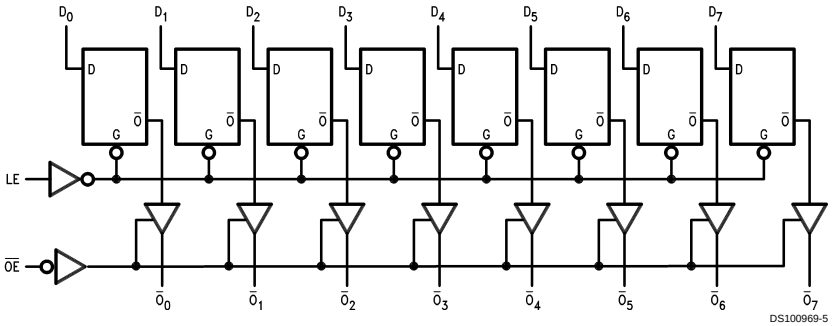
The FCT533 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
LE	**$\overline{OE}$**	**D_n**	**$\overline{O}_n$**
X	H	X	Z
H	L	L	H
H	L	H	L
L	L	X	$\overline{O}_0$

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
$\overline{O}_0$ = Previous $\overline{O}_0$ before HIGH to Low transition of Latch Enable

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65˚C to +150˚C
DC Latchup Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175˚C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'FCT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54FCT	−55˚C to +125˚C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

DC Characteristics for 'FCT Family Devices

Symbol	Parameter		FCT541 Min	FCT541 Typ	FCT541 Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54FCT	4.3			V	Min	I_{OH} = −300 µA
		54FCT	2.4			V	Min	I_{OH} = −12 mA
V_{OL}	Output LOW Voltage	54FCT			0.2	V	Min	I_{OL} = 300 µA
		54FCT			0.5	V	Min	I_{OL} = 32 mA
I_{IH}	Input HIGH Current				5	µA	Max	V_{IN} = V_{CC}
I_{IL}	Input LOW Current				−5	µA	Max	V_{IN} = 0.0V
I_{OZH}	Output Leakage Current				10	µA	Max	V_{OUT} = 5.5V; $\overline{OE}_n$ = 2.0V
I_{OZL}	Output Leakage Current				−10	µA	Max	V_{OUT} = 0.0V; $\overline{OE}_n$ = 2.0V
I_{OS}	Output Short-Circuit Current				-60	mA	Max	V_{OUT} = 0.0V
I_{CCQ}	Quiescent Power Supply Current				1.5	mA	Max	V_{IN} < 0.2V or V_{IN} 5.3V, V_{CC} = 5.5V
ΔI_{CC}	Quiescent Power Supply Current				2.0	mA	Max	V_I = V_{CC} − 2.1V
I_{CCD}	Dynamic I_{CC}				0.4	mA/ MHz	Max	V_{CC} = 5.5V, Outputs Open, One Bit Toggling, 50% Duty Cycle, $\overline{OE}_n$ = GND
I_{CC}	Total Power Supply Current				6.0	mA	Max	V_{CC} = 5.5V, Outputs Open, fI = 10MHz, $\overline{OE}_n$ = GND, One Bit Toggling, 50% Duty Cycle

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 4)	54FCT $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Max		
t_{PHL}, t_{PLH}	Propagation Delay D_n to O_n	5.0	1.5	12.0	ns	
t_{PHL}, t_{PLH}	Propagation Delay LE to O_n	5.0	2.0	14.0	ns	
t_{PZL}, t_{PZH}	Output Enable Time	5.0	1.5	12.5	ns	
t_{PHZ}, t_{PLZ}	Output Disable Time	5.0	1.5	8.5	ns	

Note 4: Voltage Range 5.0 is 5.0V ±0.5V.

AC Operating Requirements

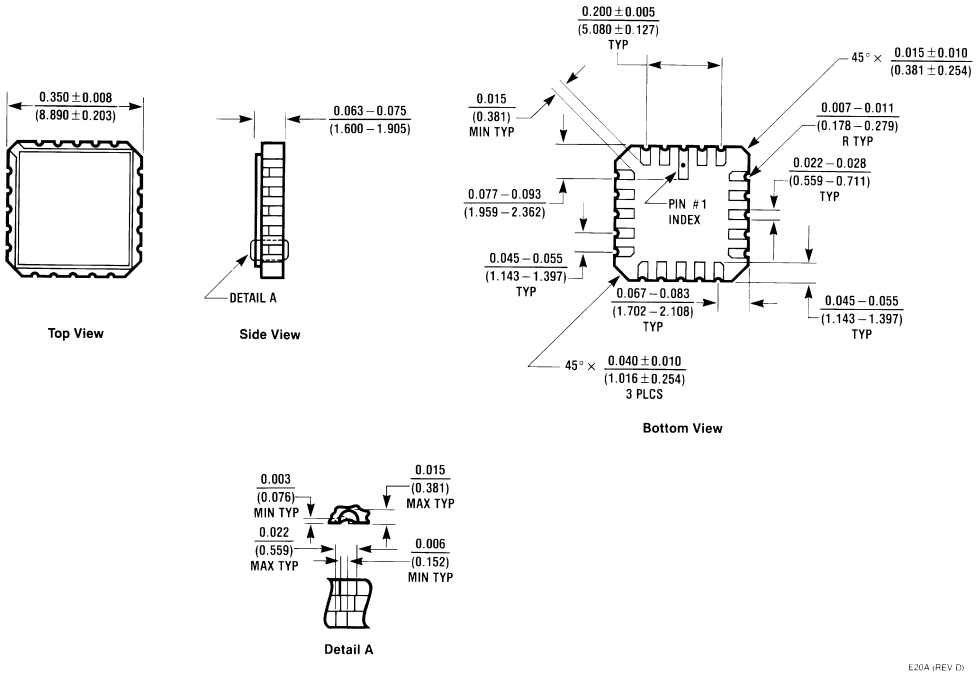
Symbol	Parameter	V_{CC} (V) (Note 5)	54FCT $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF	Units	Fig. No.
			Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW D_n to LE	5.0	2.0	ns	
t_H	Hold Time, HIGH or LOW D_n to LE	5.0	3.0	ns	
t_W	LE Pulse Width, HIGH	5.0	6.0	ns	

Note 5: Voltage Range 5.0 is 5.0V ±0.5V.

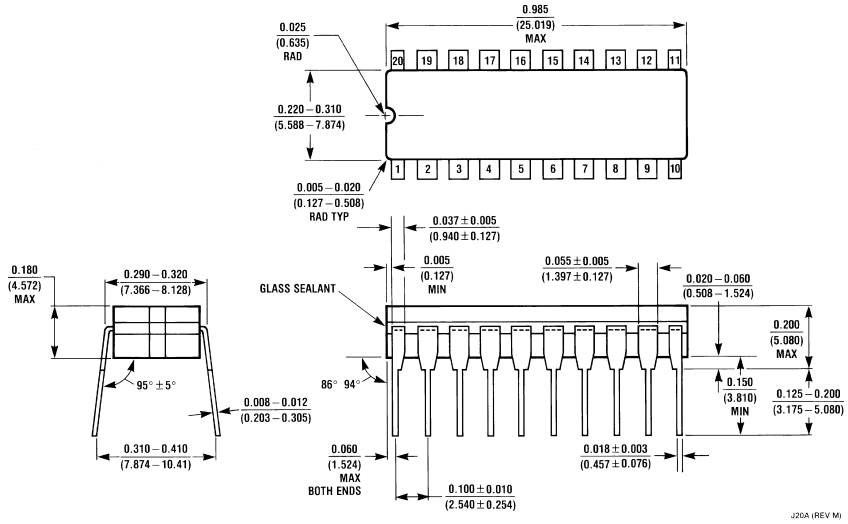
Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	10	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	40	pF	V_{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted

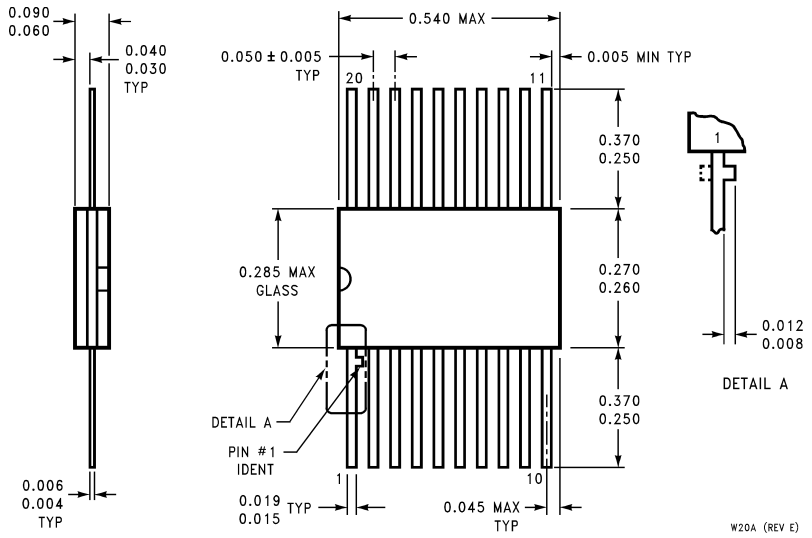


20-Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A



20-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Ceramic Flatpak (F)
NS Package Number W20A

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