July 1998

National Semiconductor

CLC016
Data Retiming PLL with Automatic Rate Selection

General Description

National's Comlinear CLC016 is a low-cost, monolithic, data retiming phase-locked loop (PLL) designed for high-speed serial clock and data recovery. The CLC016 simplifies high-speed data recovery in multi-rate systems by incorporating auto-rate select (ARS) circuitry on chip. This function allows the user to configure the CLC016 to recognize up to four different data rates and automatically adjust to provide accurate, low-jitter clock and data recovery. A single resistor is used to set each data rate anywhere between 40 Mbps and 400 Mbps. No potentiometers, crystals, or other external ICs are required to set the rate.

The CLC016 has output jitter of only 130 ps_{pp} at a 270 Mbps data rate and 0.25% fractional loop bandwidth. Low phase detector output offset and low VCO injection combine to ensure that the CLC016 does not generate bit errors or large phase transients in response to extreme fluctuations in data transition density. The result is improved performance when handling the pathological patterns inherent in the SMPTE 259M video industry standard.

The carrier detect and output mute functions may be used together to automatically latch the outputs when no data is present, preventing random transitions. The external loop filter allows the user to tailor the loop response to the specific application needs. The CLC016 will operate with either +5V or −5.2V power supplies. The serial data inputs and outputs, as well as the recovered clock outputs, allow single- or differential-ECL interfacing. The logic control inputs are TTL-compatible.

Applications

- SMPTE 259M serial digital interfaces: NTSC/PAL, 4:2:2 component, 360 Mbps wide screen
- Serial digital video routing and distribution
- Clock and data recovery for high-speed data transmission
- Re-synchronization of serial data for SONET/SDH, ATM, CAD networks, medical and industrial imaging

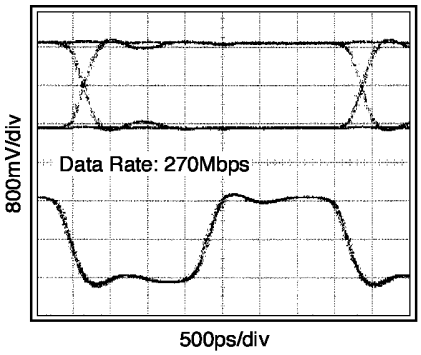
Features

- Retimed data output
- Recovered clock output
- Auto and manual rate select modes
- Four user-configurable data rates
- No potentiometers required
- External loop bandwidth control
- Frequency detector for lock acquisition
- Carrier detect output
- Output MUTE function
- Single supply operation: +5V or −5.2V
- Low cost

Key Specifications

- Low jitter: 130 ps_{pp} @ 270 Mbps, 0.25% fractional loop bandwidth (0.675 MHz)
- High data rates: 40 Mbps − 400 Mbps
- Low supply current: 100 mA, including output biasing
- Flexible fractional loop bandwidth: from 0.05% to 0.5%

Output Data and Clock, Differential



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Order Number	Temperature	Package
CLC016ACQ	0˚C to +70˚C	PLCC V28A
CLC016AJQ	–40˚C to +85˚C	PLCC V28A

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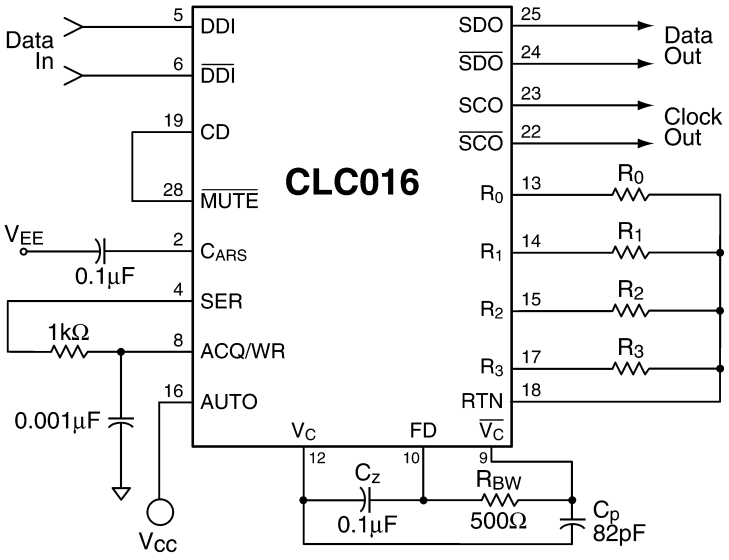
Typical Application

Four-Rate Clock and Data Recovery with Automatic Rate Selection



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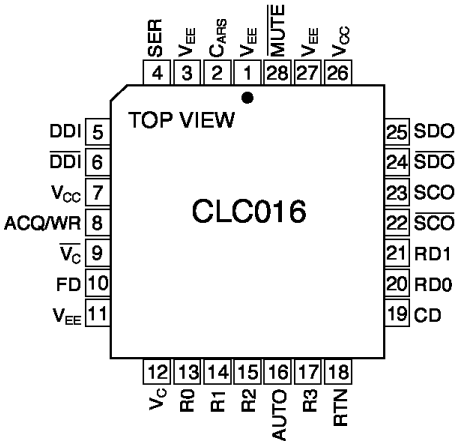
Pinout



DS100087-3

28-pin PLCC

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}–V_{EE})	−0.3, +6.0V
Maximum Junction Temperature	+150˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature (Soldering 4 sec)	+260˚C
ESD Rating (Note 12)	2kV
Package Thermal Resistance	
θ_{JA} 28-Pin PLCC	85˚C/W
θ_{JC} 28-Pin PLCC	35˚C/W
Reliability Information	
MTTF (based on limited life test data)	2.6×10^7 hours

Recommended Operating Conditions

Supply Voltage (V_{CC}–V_{EE})	4.5V to 5.5V
Operating Temperature	–40˚C to +85˚C
Jitter Transfer Function Fractional Loop Bandwidth	0.05% to 0.5%
SCO/$\overline{SCO}$, SDO/$\overline{SDO}$ Minimum Voltage (Note 13)	V_{CC} – 1.6V

Electrical Characteristics

(V_{CC} = 0V, V_{EE} = −5V, R_{BW} = 500Ω; C_Z = 0.1 µF; C_P = 82 pF; R_n = 3504, C_{ARS} = 0.1 µF; unless specified).

Parameter	Conditions	Typ +25˚C	Min/Max +25˚C	Min/Max Full Temp. Range	Units
DYNAMIC PERFORMANCE					
Residual Jitter	270 Mbps PRN sequence (Notes 3, 4)	150	250	300	ps_{pp}
Acquisition Time	270 Mbps PRN sequence	6×10^5			bit cells
Minimum Average Data Rate, f_{CLK}	$4.5V \le (V_{CC} - V_{EE}) \le 5.5V$ (Note 3)		100	100	Mbps
Full Temperature Range					
0 to 70˚	$4.5V \le (V_{CC} - V_{EE}) \le 5.5V$	40			Mbps
Maximum Average Data Rate, f_{CLK}	$4.5V \le (V_{CC} - V_{EE}) \le 5.5V$ (Note 3)		400	400	Mbps
Tracking and Capture Range	$4.5V \le (V_{CC} - V_{EE}) \le 5.5V$ (Notes 3, 5)	±8.3	±5.0/ ±13.0	±2.5/ ±18.0	$\%f_{CLK}$
VCO Power Supply Sensitivity	(Note 3)	±0.8	±1.2	±1.3	%V
VCO Temperature Sensitivity		±250			ppm/˚C
Jitter Transfer Function −3 dB bandwidth (Fractional Loop Bandwidth), λ_{BW}	R_{BW} = 100Ω (Notes 6, 7)	0.05			$\%f_{CLK}$
	R_{BW} = 500Ω (Notes 6, 7)	0.25			$\%f_{CLK}$
	R_{BW} = 1000Ω (Notes 6, 7)	0.5			$\%f_{CLK}$
Jitter Transfer Function Peaking	R_{BW} = 500Ω, 270 Mbps (Note 6)	<0.1			dB
STATIC PERFORMANCE					
Power Supply Current, I_{EE}	(Note 3)	105	125	133	mA
Voltage on Selected R_n Resistor	(Note 8)	V_{CC} −2.2			V
Voltage on Unselected R_n Resistor	(Note 8)	V_{CC}			V
V_C/$\overline{V_C}$ Common-Mode Voltage, V_{CM}	(Note 8)	V_{CC} −1.5			V
V_C/$\overline{V_C}$ Diff-Mode Voltage Range, V_{DM}	(Note 8)	±300			mV
DDI/$\overline{DDI}$			V_{CC}		V
Input Range Upper Limit, V_H					
Input Range Lower Limit, V_L			V_{EE} +2.5		V
Minimum Differential Input Amplitude, V_Δ			200	200	mV
Input Current	(Note 3)	3	6	6	µA
SCO/$\overline{SCO}$, SDO/$\overline{SDO}$					
Output Current, I_{OUT}	(Note 3)	11	9.3/12	8.6/12.7	mA
Output Voltage Swing, V_{OUT}	$R_{collector}$ = 75Ω (Note 3)	725	625/900		mV
ACQ/WR, $\overline{MUTE}$, RDO/RD1	(Note 9)				
Voltage Input — LOW, V_{IL}			V_{EE} + 0.8	V_{EE} + 0.8	V
Voltage Input — HIGH, V_{IH}	(Note 3)		V_{EE} + 2.0	V_{EE} + 2.0	V
Input Current (I_{IN})	(Note 3)		±100	±500	nA

Electrical Characteristics (Continued)

(V_{CC} = 0V, V_{EE} = −5V, R_{BW} = 500Ω; C_Z = 0.1 µF; C_P = 82 pF; R_n = 3504, C_{ARS} = 0.1 µF; unless specified).

Parameter	Conditions	Typ +25˚C	Min/Max +25˚C	Min/Max Full Temp. Range	Units
STATIC PERFORMANCE					
CD, UNL, RDO/RD1	(Note 9)				
Current Output — LOW, I_{OL}	$V_{OL} \le V_{EE}$+0.5V	800			µA
Current Output — HIGH, I_{OH}	$V_{OH} \ge V_{CC}$−0.5V	−700			µA
TIMING PERFORMANCE					
Delay: SCO to SDO, t_d		200			ps
SCO Duty Cycle	(Note 3)	50	44/56	44/56	%
Rise/Fall Time: SCO, SDO, t_r/t_f	20%–80%, $R_{collector}$ = 75Ω (Note 10)	230			ps
SDO Duty Cycle Distortion		35			ps
Minimum Setup Time: RDO/RD1 to ACQ/WR, t_{SU}		4	20	20	ns
Minimum Hold Time: ACQ/WR to SS1/SS0, t_h		3	20	20	ns
Minimum Pulse Width: ACQ/WR, t_w		5	20	20	ns
ARS Oscillator Period, t_{OSC}	(Note 3)	10.5	8.5/15.5		ms
CD Pulse Width, t_{PW}	(Note 11)	1			µs
$\overline{\text{MUTE}}$ Response Time, t_M		5			ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Note 3: J-level spec. is 100% tested at +25˚C.

Note 4: Peak-to-peak jitter is defined as 6 times the rms jitter.

Note 5: Tracking and capture range are specified as a percentage of the input data rate f_{CLK}. The minimum and maximum are guaranteed so long as R_n has been chosen according to the equation in ***Resistor Selection for Data Rates.***

Note 6: Average data transition density of 1 transition per 2 bit cells.

Note 7: When the value of R_{BW} changes it is necessary to also change the values of C_P and C_Z. See ***Loop Filter Design.***

Note 8: This information is provided for system troubleshooting purposes only.

Note 9: RD0/RD1 are inputs when AUTO = 0 and outputs when AUTO = 1.

Note 10: Includes typical pc board capacitance.

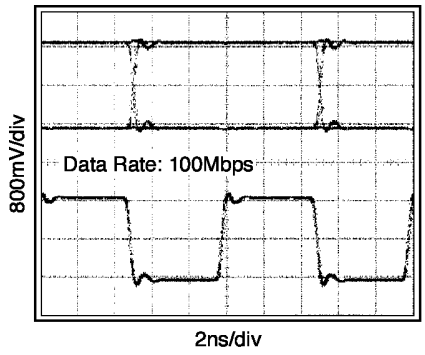
Note 11: The CD circuit is a retriggerable one-shot which retriggers on every data transition.

Note 12: Human body model, 1.5 kΩ in series with 100 pF.

Note 13: To maintain specified performance, SCO/$\overline{\text{SCO}}$ and SDO/$\overline{\text{SDO}}$ should not drop below this level.

Typical Performance Characteristics

Output Data and Clock, Differential



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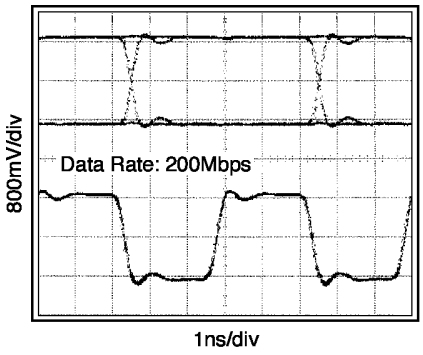
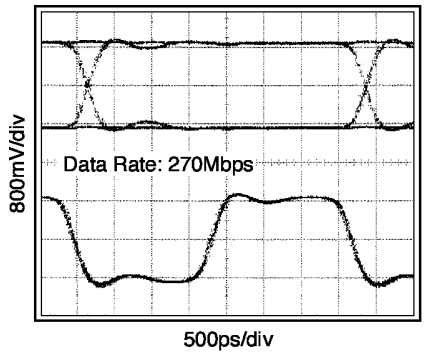
Output Data and Clock, Differential



DS100087-5

Output Data and Clock, Differential



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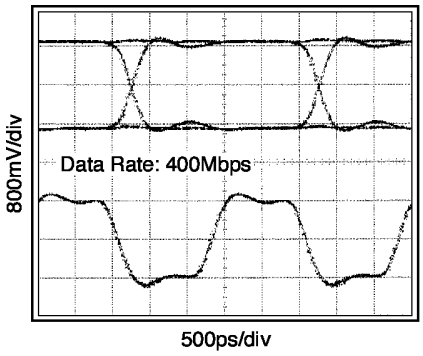
Output Data and Clock, Differential



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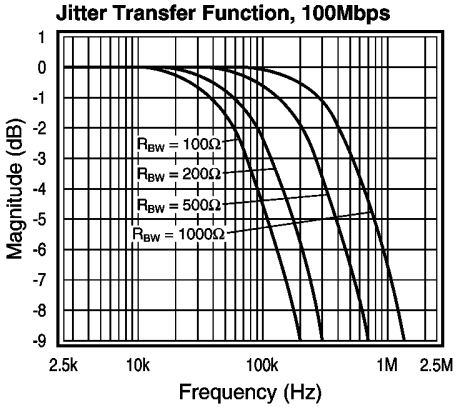
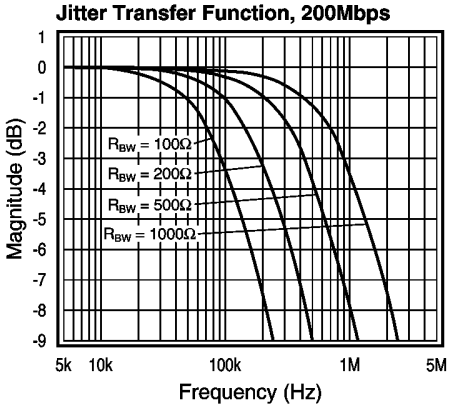
Jitter Transfer Function, 100Mbps



DS100087-8

Jitter Transfer Function, 200Mbps



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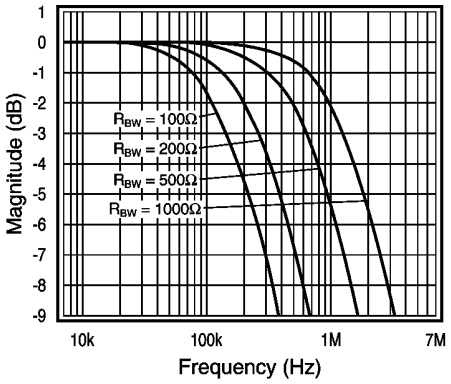
Typical Performance Characteristics (Continued)

Jitter Transfer Function, 270Mbps



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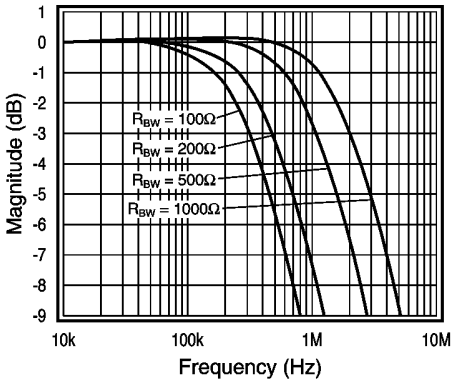
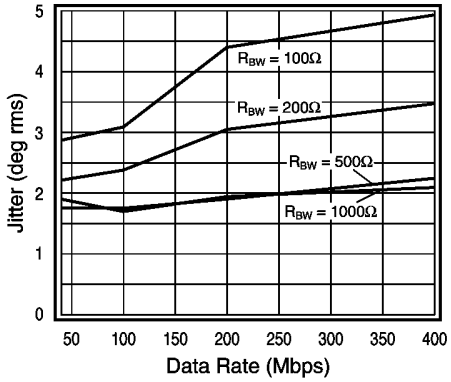
Jitter Transfer Function, 400Mbps



DS100087-11

Residual Jitter vs. Data Rate



DS100087-12

Product Description

The CLC016 Data Retiming PLL is a monolithic circuit that recovers clock and data from a serial NRZ or NRZI data stream. The Data Retiming PLL incorporates an Auto-Rate Selection function which automatically selects one of four user-configurable data rates. The following outline lists the material covered in this data sheet:

- Typical schematics for +5V or −5.2V operation
- Block diagram description
- Pin definitions
- Design guidelines
- Interface connections
- Measurement
- Typical applications
- Printed circuit layout and evaluation boards

For application assistance, refer to the list of telephone numbers on the pack page of this data sheet.

Data Retimer Typical Connections

The CLC016 schematics provided in *Figure 1* and *Figure 2* show typical +5V or −5.2V connections with Auto-Rate Selection configured for SMPTE 259M standard video data rates: 143, 177, 270 and 360 Mbps. The section ***Resistor Selection for Data Rates*** gives tables and equations for determining R_n resistor values for any data rate from 50 Mbps to 400 Mbps. A resistor value table is also given for SONET/SDH data rates. The schematics in *Figure 1* and *Figure 2* do not include input termination. The high impedance inputs on the CLC016 allow the user to define the termination. The ***Interfaces*** section suggests recommended terminations for the inputs and outputs of the CLC016.

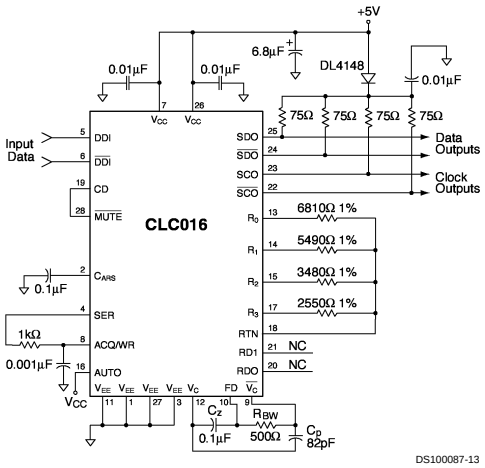


FIGURE 1. Typical +5V Connection

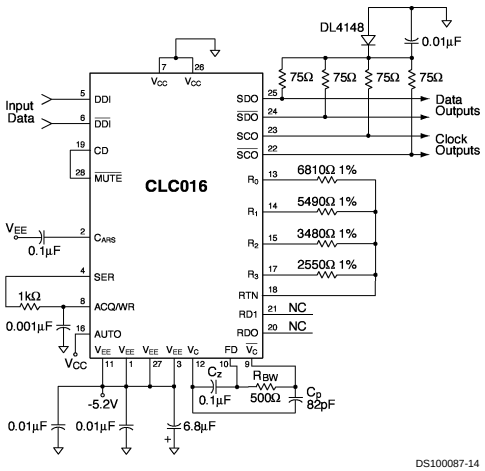


FIGURE 2. Typical −5.2V Connection

Product Description (Continued)

Pin Definitions

Name	Pin #	Description
DDI, $\overline{DDI}$	5, 6	Differential (ECL, PECL) data inputs.
SCO, $\overline{SCO}$	23, 22	Differential collector (ECL, PECL compatible) clock outputs
SDO, $\overline{SDO}$	25, 24	Differential collector (ECL, PECL compatible) retimed data outputs
RDO, RD1	20, 21	Bi-directional (TTL, CMOS) VCO data rate bus. See *Table 3* for state table.
R_n	13, 14, 15, 17	VCO rate configuration resistors (n = 0, 1, 2, 3).
RTN	18	Return for R_n
SER	4	Loop unlock output (TTL, CMOS) indicator. High when loop is unlocked or harmonic-locked.
CD	19	Carrier detector (TTL, CMOS) output. Low when no signal is present.
$\overline{MUTE}$	28	Output mute (TTL, CMOS) control. Connect to CD to latch outputs when no signal is present.
AUTO	16	Auto- or manual-rate mode control (TTL, CMOS) input. Assert high for auto-rate mode.
ACQ/WR	8	ARS oscillator enable and rate latch enable (TTL, CMOS) input. Connect to SER (see diagrams) for auto-rate mode.
C_{ARS}	2	External capacitor connections for controlling the rate of the ARS search.
V_C, $\overline{V_C}$	12, 9	VCO control lines. Loop filter connects across these and FD.
FD	10	Frequency detector output. C_Z must connect from FD to V_C.
V_{CC}	7, 26	Positive supply pins (ground or +5V).
V_{EE}	1, 3, 11, 27	Negative supply pins (−5.2V or ground).

Operation Description

The CLC016 Data Retiming PLL, *Figure 3*, has three main functions: Frequency Detector (FD), Phase-Locked Loop (PLL) and Auto-Rate Select (ARS).

The Frequency Detector detects the frequency difference between the input data rate and the VCO frequency, and forces a rapid change in VCO frequency to minimize that difference. As the frequency difference approaches zero, the PLL acquires phase lock and the Frequency Detector becomes inactive. In Auto-Rate Select mode, the Frequency Detector requests the ARS function to search for a new data rate.

The PLL consists of a Voltage Controlled Oscillator (VCO), a Phase Detector (PD), and an external Loop Filter (LF). The PLL recovers a low-jitter clock for data retiming. The data is re-synchronized (retimed) at the Data Latch. The data and clock are buffered outputs.

The ARS block has two modes of operation: Auto-Rate Mode (ARM) and Manual-Rate Mode (MRM). Once the ARS function is activated (ARM), it sequences through the user-selected data rates until phase lock is achieved. The user has control over the rate at which ARS steps through the data rates (see ***Auto-Rate Selection*** section).

The Carrier Detect (CD) block detects the presence of input data and is an input to the ARS block. When CD is connected to $\overline{MUTE}$ and no data is present, the clock and data outputs are latched.

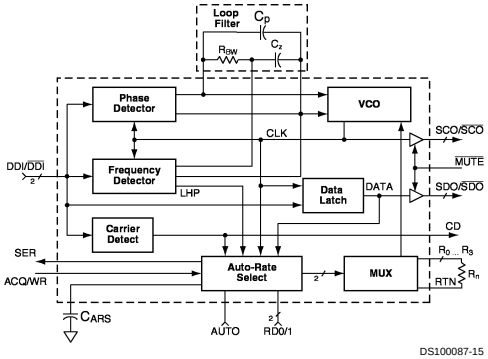


FIGURE 3. Functional Block Diagram

Product Description (Continued)

Functional Block Descriptions

Frequency Detector (FD)

The Frequency Detector detects the difference between VCO rate and the input data rate, then forces the frequency (rate) difference to zero. In Auto-Rate Mode, when a difference is detected, FD requests the ARS block to start a search to match the rate. Once the PLL acquires phase lock, the PLL takes control and the FD goes inactive.

Phase Detector (PD)

The PD compares the phase of the VCO to the phase of the input data. The PD output is a differential current which is proportional to the phase error. The PD gain has units of amperes per radian and is dependent upon the data transition density (ρ). The data transition density is defined as the average number of data transitions per clock cycle, and is bounded by $0 \leq \rho \leq 1$. The PD output is connected to the VCO through the external loop filter network. This network translates the PD output current to a voltage that controls the VCO.

Loop Filter (LF)

The external Loop Filter shown in *Figure 3* is made up of passive components R_{BW}, C_Z, and C_P. This external loop filter controls the PLL dynamics and acquisition time.

The Frequency Detector supplies its signal to the C_Z capacitor, and takes control of the VCO under the condition of frequency unlock. The selection of the filter components is covered in the ***Loop Filter Design*** section.

Voltage Controlled Oscillator (VCO)

The VCO is a temperature-compensated, factory-trimmed multivibrator that requires no external capacitors for tuning. It is stable over temperature and power supply variations. This eliminates the need for potentiometers to adjust each of the VCO center frequencies to correspond with the input data rates. Instead, an external resistor (R_n) is used to set each of four data rates in the range of 40 Mbps to 400 Mbps.

Carrier Detector (CD)

The CD circuit is a retriggerable one-shot which retriggers on every data transition. When data transitions occur at a rate ≥1 transition per µs, CD indicates the presence of data at the input pins DDI and $\overline{\text{DDI}}$. CD also inputs a signal to ARS that inhibits any rate search from occurring in the absence of input data. When CD in connected to the $\overline{\text{MUTE}}$ pin, and no data is present, the output clock (SCO, $\overline{\text{SCO}}$) and data (SDO, $\overline{\text{SDO}}$) lines are latched.

Auto-Rate Select (ARS) and Multiplexer (MUX)

The ARS, in conjunction with the MUX, sequences through the user-configured resistor values (R_n) in an unlocked condition. The ARS has two modes: Auto-Rate Mode (ARM) and Manual-Rate Mode (MRM). It incorporates additional features and functions that are discussed in the section named ***Auto-Rate Selection.***

When ARS is in Auto-Rate Mode, its inputs are the FD (the LHP control line), the Carrier Detect (CD), the VCO (CLK), and Latched Data output. These input signals produce an external Search (SER) signal that, when connected to the ACQ/WR input, enables the ARM operation. A single capacitor, C_{ARS}, sets the ARM sequence time for stepping through the different user-configured data rates.

The timing section of the ARS block controls the digital input analog multiplexer (MUX). Under the control of ARS, the MUX steps through each data rate starting with the previously-selected resistor R_n and incrementing to R_{n+1}, etc. in order of R_0, R_1, R_2, R_3, R_0, ... This sequence is repeated until lock is achieved. The 2-bit bidirectional bus, comprised of RD0 and RD1, indicates the selected data rate. The RD0, RD1 bidirectional bus is set to output mode when AUTO is active (high). Therefore, RD0, RD1 can be monitored when AUTO is active. When no data is present at the inputs, CD will inhibit the ARM.

In manual mode the RD0, RD1 lines are set to input mode. Therefore, RD0, RD1 cannot be monitored when AUTO is inactive. The selection of external components for both modes of operation is discussed in sections, ***Resistor Selection for Data Rates,*** and ***Auto-Rate Selection***.

DESIGN GUIDELINES

Resistor Selection for Data Rates

The CLC016 Data Retiming PPL supports 4 different data rates using user-selected resistors that set the VCO center frequency. The resistors found in *Figures 1, 2* are identified by the reference designators R_n, where n is 0, 1, 2 and 3.

It is recommended that the user select resistor values with tolerances of 1% and temperature coefficients of ≤100 ppm/°C. Refer to *Table 1* and *Table 2* for calculated resistor values for SMPTE and SONET standards. Resistors for other data rates are determined from the following equation:

$$R_n = \left(\frac{1000\ \text{Mbps}}{f_{CLK}} - 0.2\right) \cdot 1\ \text{k}\Omega$$

where n = 0, 1, 2, 3 and f_{CLK} is the desired data rate.

TABLE 1. Resistor Values for SMPTE 259M Data Rates

Data Rate (Mbps)	Ref. Des. (in *Figures 1, 2*) R_n	Calculated Resistor (kΩ)	1% Resistors (in *Figures 1, 2*) (kΩ)
143	R_0	6.79	6.81
177	R_1	5.45	5.49
270	R_2	3.50	3.48
360	R_3	2.58	2.55

TABLE 2. DS-3 and SONET/SDH Resistor Values

Data Rate (Mbps)	Calculated Resistor (kΩ)	1% Resistors (kΩ)
44.7	22.1	22.1
51.84	19.1	19.1
155.52	6.23	6.19
311.04	3.02	3.01

Loop Filter Design

The function of the PLL is to low-pass filter the jitter of the incoming data stream. The jitter transfer function for the PLL (or the phase transfer function) is set by the phase detector gain, the loop filter transfer function, and the VCO gain. These elements are shown in the small-signal block diagram, *Figure 4*.

Product Description (Continued)

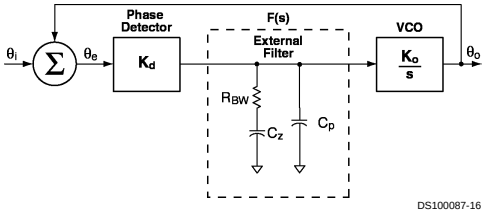


FIGURE 4. PLL Loop

The jitter transfer function is the small signal transfer function, θ_o/θ_i, and is given by:

$$\frac{\theta_o}{\theta_i} = \frac{2\pi f_{BW}(s + 2\pi f_Z)}{s^2 + s2\pi f_{BW} + 4\pi^2 f_{BW} f_Z}$$

where f_{BW} is the PLL bandwidth and f_Z is a zero in the closed loop transfer function.

The phase detector gain and VCO gain are fixed internally. Selection of the external loop filter components defines the overall jitter transfer function. Additionally, the filter components control the acquisition performance of the PLL.

A Bode plot for the closed loop PLL jitter transfer function is shown in *Figure 5*.

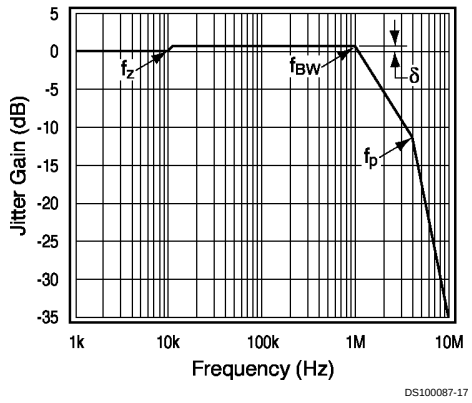


FIGURE 5. Closed-Loop Transfer Function

At frequencies above f_{BW} (the PLL bandwidth) the jitter is attenuated. At frequencies below f_{BW} the jitter is transmitted through the PLL. A small amount of jitter peaking (δ) occurs at frequencies below f_{BW}. The amount of peaking increases when f_Z moves closer to f_{BW}.

Setting the Loop Bandwidth (Selecting R_{BW})

The fractional loop bandwidth, λ_{BW}, is the ratio of f_{BW} to the data rate. The CLC016 is specified for operation with fractional loop bandwidths ranging from 0.05% to 0.5%. For example, if the loop bandwidth is 1 MHz and the data rate is 270 Mbps, then the fractional loop bandwidth is:

$$\lambda_{BW} = \frac{f_{BW}}{f_{CLK}} = \frac{1\ \text{MHz}}{270\ \text{Mbps}} = 0.0037 \text{ or } 0.37\%$$

The fractional loop bandwidth is set by the loop component R_{BW}:

$$\lambda_{BW} = \left(\frac{\rho}{2\pi}\right)\frac{R_{BW}}{16.67\ \text{k}\Omega}$$

where ρ is the data transition density in average number of data transitions per bit cell, and ranges in value from 0 to 1. For example, if a pseudo-random data stream is used, the value of ρ is 1/2, and a data transition will occur once every two bit cells on the average. The phase detector and VCO gain set the constants in the equation.

If the value of R_{BW} is 500Ω and ρ = 1/2, the fractional loop bandwidth is:

$$\lambda_{BW} = \left(\frac{0.5}{2\pi}\right)\frac{500\Omega}{16.67\ \text{k}\Omega} = 0.0024 \text{ or } 0.24\%$$

For a data rate of 270 Mbps this corresponds to a loop bandwidth f_{BW} = 644 kHz. The jitter at frequencies above 644 kHz will be attenuated by the PLL.

The equation may be rearranged to obtain R_{BW} as a function of the desired fractional loop bandwidth:

$$R_{BW} = \frac{2\pi\lambda_{BW} \cdot 16.67\ \text{k}\Omega}{\rho}$$

Setting the Jitter Peaking Factor (Selecting C_Z)

The jitter peaking factor, δ, is set by the ratio of the critical frequencies f_Z and f_{BW}. The ratio is defined as:

$$\alpha = \frac{f_Z}{f_{BW}}$$

Figure 6 shows how the jitter peaking factor, δ, varies with α. For example, if the value of α is 0.1, then the jitter peaking is about 0.6 dB.

The approximation for the required value of α to obtain a given amount of jitter peaking is:

$$\alpha \cong \delta(0.134 + 0.058\delta)$$

The critical frequency f_Z is:

$$f_Z = \frac{1}{(2\pi C_Z R_{BW})}$$

Select C_Z by the following equation:

$$C_Z = \frac{1}{2\pi\alpha R_{BW} f_{BW}}$$

Product Description (Continued)

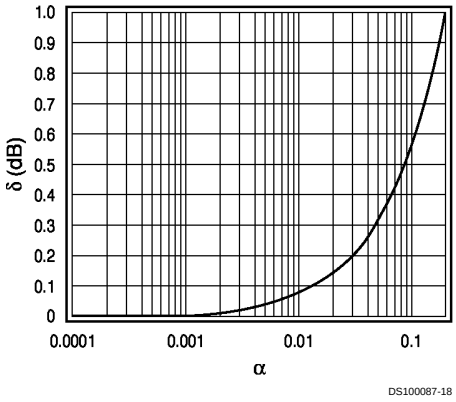


FIGURE 6. Jitter Peaking Curve

As an example, assume that the amount of jitter peaking that can be tolerated is 0.05 dB. From the jitter peaking design equation (or from *Figure 6*) the required value of α is:

$$\alpha \cong 0.05[0.134 + (0.058)(0.05)] = 0.007$$

Now assuming that the loop bandwidth is 644 kHz and that the value of R_{BW} is 500Ω, the value of C_Z is:

$$C_z = \frac{1}{2\pi \cdot 0.007 \cdot 500 \cdot 644 \cdot 10^3} = 0.07\ \mu F$$

The value of C_Z also affects the acquisition performance of the PLL. Estimate the acquisition time with the following equation:

$$t_{ACQ} \cdot f_{CLK} \leq \frac{C_z}{0.14\ pF}$$

where t_{ACQ} x f_{CLK} is the acquisition time in number of bit cells.

Selecting C_P

Capacitor C_P establishes a high frequency pole in the loop filter to remove high frequency spectral components from the phase detector. The pole frequency f_P is:

$$f_p = \frac{1}{2\pi R_{BW} C_p}$$

In general, the pole should be set at least a factor of 4 above the PLL bandwidth, f_{BW}. Therefore, select C_P using:

$$C_p = \frac{1}{8\pi R_{BW} f_{BW}}$$

For example, if R_{BW} is 500Ω and f_{BW} is 644 kHz, then an appropriate value for C_P is:

$$C_p = \frac{1}{8\pi \cdot 500 \cdot 644 \cdot 10^3} = 125\ pF$$

Choosing a value for C_P larger than the value recommended by the selection equation will introduce jitter peaking. Reducing the value of C_P below that recommended by the selection equation is acceptable, but will result in some increase in jitter. This is most noticeable with large fractional loop bandwidths.

In addition, C_P can affect the ability of the PLL to acquire lock, especially at high data rates. Because of this, it is recommended to eliminate C_P entirely for the condition of high data rate (>300 Mbps) combined with narrow loop bandwidth (<0.1%).

Multiple Rate Considerations

R_{BW} establishes the fractional loop bandwidth. For a fixed value of R_{BW}, f_{BW} will vary with the selected data rate. The location of the critical frequencies f_Z and f_P, however, are independent of data rate.

To control jitter peaking for all multi-rate application choose:

- the value of C_Z for the smallest value of f_{BW} (which is obtained at the lowest data rate).
- the value of C_P for the largest value of f_{BW} (which is obtained at the highest data rate).

Loop Filter Element Summary Table

The table below summarizes the recommended loop filter element values for each of the four SMPTE 259M data rates and a fractional loop bandwidth of 0.25%. The final row of the table gives the recommended values for the multi-rate case, where all four of the SMPTE rates are configured.

Data Rate (Mbps)	f_{BW} (kHz)	R_{BW} (Ω)	C_Z (µF)	C_P (pF)
143	358	500	0.10	200
177	443	500	0.10	160
270	675	500	0.047	100
360	900	500	0.04	82
143–360	0.25% f_{CLK}	500	0.10	82

Component Types and Tolerances

It is recommended that R_{BW} resistors have tolerances of 1% and temperature coefficients of ≤100 ppm/°C. The recommended capacitors are ceramic surface mount with 5% tolerance or better.

AUTO-RATE SELECTION

Auto Rate Mode (ARM)

This section provides more detail on the ARS sub-system and how to use it. *Figure 7* shows a detailed view of the ARS portion of the *Figure 3* block diagram

The auto-rate mode is enabled by connecting AUTO to V_{CC} and SER to ACQ/WR through the 1 kΩ/1 nF network. When the VCO is not at the input data rate, SER goes high enabling the ARS oscillator and the Latch. The oscillator increments the 2-bit counter and causes the VCO to sequence through the rates determined by resistor R_n (beginning at the currently selected rate and advancing the index, n, upward). The oscillator period (T_{ARS}) is determined by C_{ARS}. When the VCO rate is at the input data rate, SER goes low and ceases to increment the counter.

Product Description (Continued)

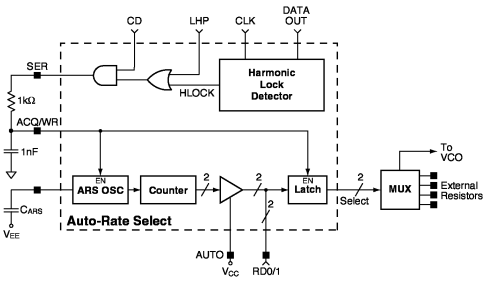


FIGURE 7. Auto-Rate Select

SER goes high when CD is high and either of the following conditions is true:

- The FD is active, causing LHP to go high.
- The harmonic lock detector determines that the VCO is running at a harmonic of the input data rate, causing HLOCK to go high.

Timing diagrams related to locking and unlocking of the PLL and removal of the input data are given in *Figures 8, 9* and *Figure 10*. The term t_{ACQ} in *Figure 8* is defined in the ***Loop Filter Design*** section. Also, t_S is the settling time for the phase error to decay to less than 90°. It is given by the following equation:

$$t_S = R_{BW} \times C_Z \times \ln(2) + 20\ \mu s$$

The ARS oscillator period must be greater than the sum of t_{ACQ} and t_S:

$$t_{ARS} = (140\ ms/\mu F) \times C_{ARS} > t_{ACQ} + t_S$$

The harmonic lock detector senses if the VCO is locked to a data rate harmonic (integer multiple) by looking for the presence of bit changes across 3 consecutive periods of CLK as shown in Case 1 of *Figure 11*. This event occurs on average 25% of the time in random data. HLOCK goes low if the occurrence rate is less than 12.5%. When a harmonic lock condition occurs there is at least a 2 µs delay for HLOCK to go high. Case 2 illustrates the situation where CLK is at the 2nd harmonic of the input data rate and each input bit cell is double-clocked. Bit changes across three consecutive periods are never detected and HLOCK goes high.

During intervals of sparse data transitions, the harmonic lock detector may cause SER to go high. An example of this is the pathological pattern associated with the SMPTE 259M video industry standard. For an interval of 50 µs, the input data transitions can be separated by 20-bit cells; and it appears to the harmonic lock detector as though the VCO is at a harmonic rate. So long as these intervals do not exceed the period of the ARS oscillator, the ARS sub-system will not increment the 2-bit counter. ***T_{ARS} must be the greater of the value calculated by the above equation of the sparse data pattern interval.*** *Figure 12* shows a timing diagram relating to sparse data transition intervals.

In auto-rate mode the user can monitor the RD0/1 bus to determine the automatically selected data rate. Refer to *Table 3* for the correspondence between the data bus state and the selected rate resistor.

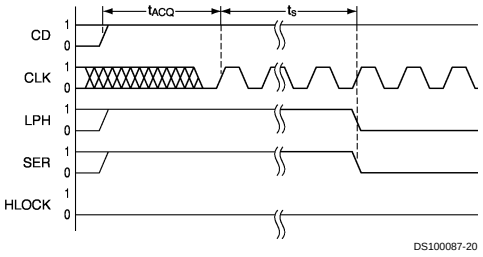


FIGURE 8. Data Rate Applied or Moves within PLL Capture

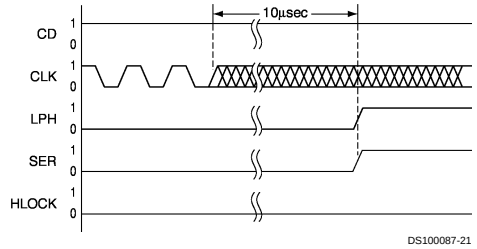


FIGURE 9. Data Rate Moves beyond the PLL Tracking Range

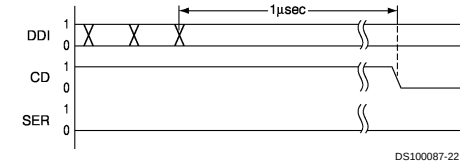


FIGURE 10. Input Data Removed

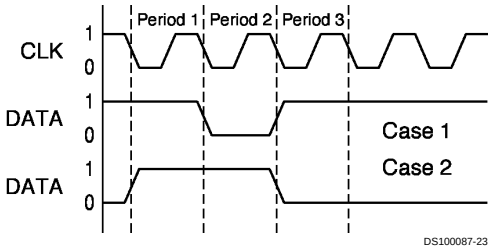


FIGURE 11. Harmonic Lock Detector Operation

Product Description (Continued)

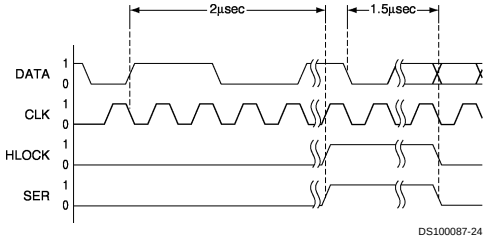


FIGURE 12. Response to Sparse Patterns

Minimum Data Rate Spacing in ARM

RD0 and RD1 indicate which VCO rate configuration resistor (i.e., R_n) is selected. For each resistor there is a range of rates that the PLL will lock to. If two data rates fall within this range, a given RD0/RD1 indication may correspond to either rate. If it is desired that each incoming data rate be uniquely reported by RD0 and RD1, then the minimum spacing between data rates must be great enough to prevent the tracking and capture range of the PLL for one rate configuration resistor from encompassing the adjacent rate. The tracking and capture range is given in the ***Electrical Characteristic*** table. In addition, the tolerance of VCO rate configuration resistor should be added to the guaranteed tracking and capture range in computing minimum data rate spacing.

Manual Rate Mode (MRM)

The Manual Rate Mode provides the user with manual control over the data rate selection. This is done by setting the AUTO line low and shorting the C_{ARS} capacitor to V_{EE}. The manual data rate is set by the 2-bit bus RD0/1 using the ACQ/WR line to initiate a MUX update. *Table 3* gives the state table for resistor selection.

TABLE 3. Rate State Table

ACQ/WR	RD1	RD0	Resistor
1	0	0	R_0
1	0	1	R_1
1	1	0	R_2
1	1	1	R_3
0	X	X	No Change

When in the MRM, the AUTO line is set low as in *Figure 13*. The buffer output is TRI-STATE® which allows the bus lines RD0/1 to be used as inputs to the latch. The inputs RD0/1 are latched by using the ACQ/WR line.

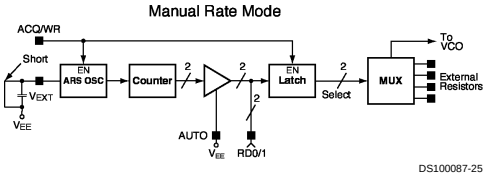


FIGURE 13. Manual Select Mode

The ACQ/WR line and bus lines RD0/1 must observe setup and hold conditions. The minimum requirements are specified in the sub-section ***Timing Performance*** of the ***Electrical Characteristics*** page. The timing diagram in *Figure 14* indicates where the measurements are made.

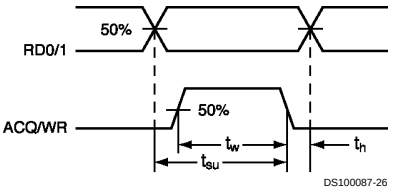


FIGURE 14. ACQ/WR and RD0/1 Timing Diagram

Fixed Rate Mode

For single data rate applications, set AUTO low, ACQ/WR high, and tie RD0 and RD1 to the levels shown in *Table 3*. Also, short C_{ARS} to V_{EE}.

Minimum Data Rate Spacing in MRM

If it is desired that SER goes high (due to the inability of the PLL rate) as an indication that the incoming data rate does not correspond to the intended rate selected by RD0 and RD1, then the minimum spacing between data rates must be great enough to prevent the tracking and capture range of the PLL at one rate from encompassing the adjacent rate. If the data rates are too close, it is possible for the PLL to lock to either rate regardless of which was selected by RD0 and RD1. The tracking and capture range is given in the ***Electrical Characteristics*** table. In addition, the tolerance of VCO rate configuration resistors should be added to the guaranteed tracking and capture range in computing minimum data rate spacing.

Output Timing

The clock-to-output data timing has a small delay of clock-to-data. This delay is specified in the ***Electrical Characteristics*** page under the sub-section ***Timing Performance.*** The delay is measured from the 50% level of the CLK to the eye pattern 50% crossing, as shown in *Figure 15*

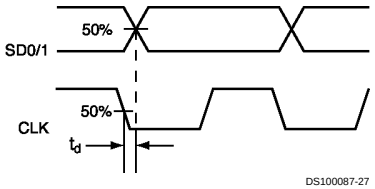


FIGURE 15. Output Timing of Clock and Data

INPUT INTERFACES

The CLC016 provides high impedance inputs which accept differential or single-ended input drive. The detailed electrical specifications are found in the ***Electrical Characteristics*** page. Recommended interfaces for the CLC016 follow.

Four conditions should be observed when interfacing to the CLC016 inputs:

- Keep input levels within specified common-mode input range.
- Provide a bias current path to the inputs.
- Terminate cable in the proper impedance.

Product Description (Continued)

- Observe the output current requirements of the driving device.

Figure 16 and *Figure 17* show DC and AC coupled interface examples which meet these four conditions.

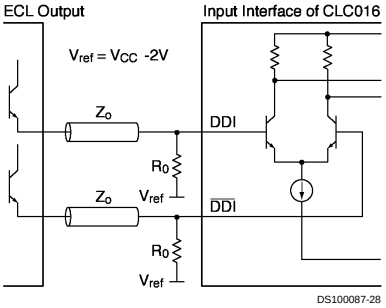


FIGURE 16. Differential 75Ω Source

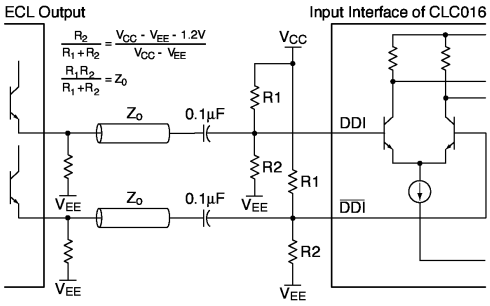


FIGURE 17. AC Coupled Termination

OUTPUT INTERFACES

SDO, $\overline{SDO}$, SCO, and $\overline{SCO}$ swing at ECL logic levels when the correct external components are used. However, the outputs are not standard emitter-coupled logic outputs. Instead, the signals flow from the collectors of the output transistors. The primary advantage of this architecture is lower power dissipation. Some example interfaces follow.

Differential Load-Terminated Output Interface

Figure 18 shows an interface to drive signals differentially over a coaxial cable. The diode establishes V_{OH}. The diode-resistor network sets V_{OL}. The resistors terminate the cable in its characteristic impedance.

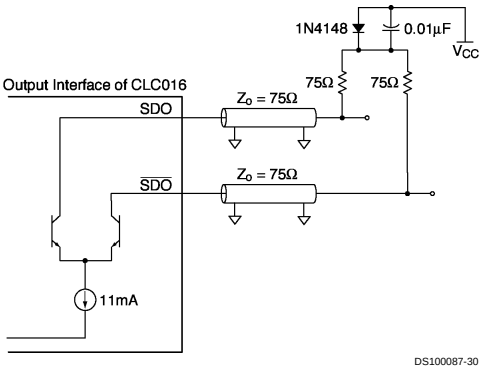


FIGURE 18. Differential Load-Terminated Output Interface

Differential Source-Terminated Output Interface

Figure 19 is similar to *Figure 18* except that the termination is placed near the output pins.

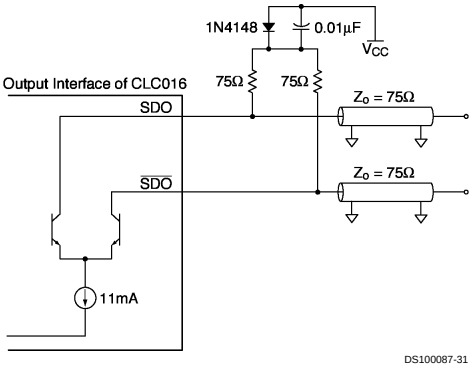


FIGURE 19. Differential Source-Terminated Output Interface

Terminating Physically Separated Outputs

When the circuit design requires the outputs to be routed to separate locations, the recommended interface is depicted in *Figure 20*. Choose the resistors for an equivalent 75Ω termination of the cable impedance (or other cable characteristic impedance, as appropriate).

Product Description (Continued)

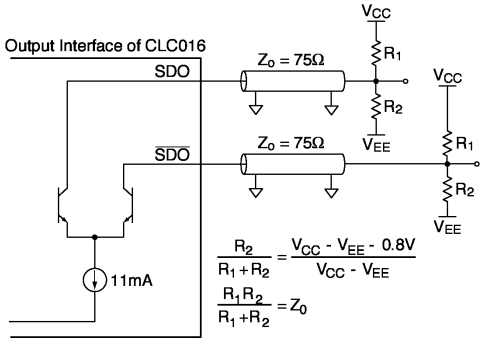


FIGURE 20. Load Terminated Output Interface

CONTROL LINE INTERFACES

The use of the CLC016 with +5V supplies allows the control lines to interface to standard TTL logic signals. Operating the CLC016 at −5.2V requires level-shifting circuits for the control line inputs. Refer to the ***Static Performance*** section of the ***Electrical Characteristics*** page for required input voltage levels.

POWER CONSUMPTION

The power supply current given in the Electrical Characteristics table includes the current required for both the clock and data output buffers to drive a 75Ω load to ECL swings.

TYPICAL APPLICATIONS

The CLC016 was designed as one of a series of data transmission support chips. The CLC016 is recommended for a wide variety of clock and data recovery applications that fit within its range of data rates.

Serial Data Transmission over Cable

Serial data transmission is common for all types of communication channels where the data is sent over coaxial or twisted pair cable. *Figure 21* shows a typical connection using a CLC006 driver chip, CLC014 Adaptive Cable Equalizer, and the CLC016 Data Retiming PLL. The CLC016 extracts the clock and retimes the data from the serial bit stream.

The components recommended in *Figure 21* support the four common data rates specified in SMPTE 259M.

ESD

The CLC016 is a ***CMOS chip.*** Operators are cautioned to ***use grounding straps when handling.***

MEASUREMENTS & EVALUATION

When evaluating the CLC016 Data Retimer, it is recommended that you solder the part to the board or use a leadless chip carrier socket. Probing with capacitive probes will disturb the CLC016 performance. When probing the signal levels use a ***1 pF capacitance*** probe with a 500Ω tip.

The block diagram below shows a simple method of measuring the clock to eye pattern jitter. Use of the CLC016 evaluation board is recommended for jitter evaluation. It also provides a good reference for a user's circuit board design. The plot in *Figure 23* shows a histogram of the jitter and where the measurements were taken.

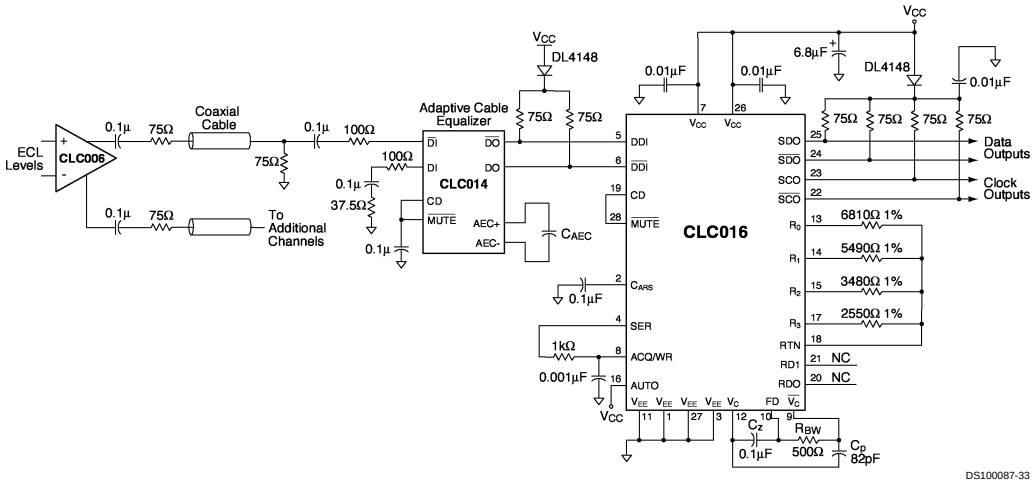


FIGURE 21. Typical Cable Connection

Product Description (Continued)

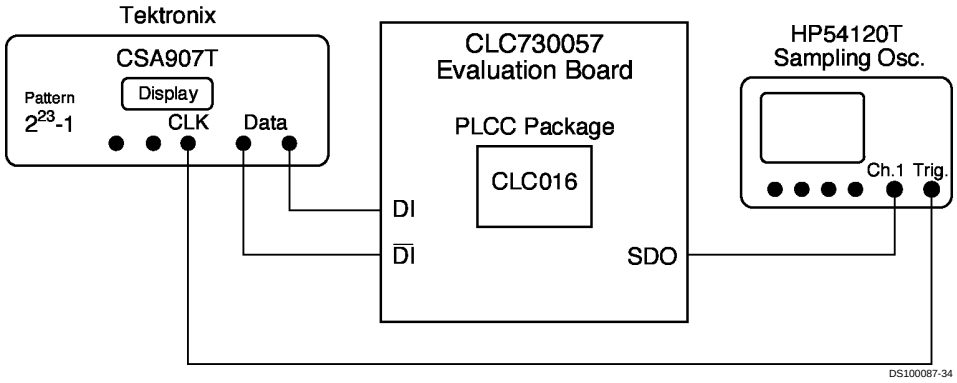


FIGURE 22. Jitter Measurement Setup

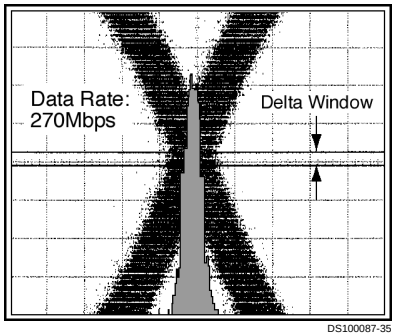


FIGURE 23. Typical Jitter Histogram

PCB LAYOUT RECOMMENDATIONS

Printed circuit board layout affects the performance of the CLC016. The following are PCB layout rules for the CLC016:

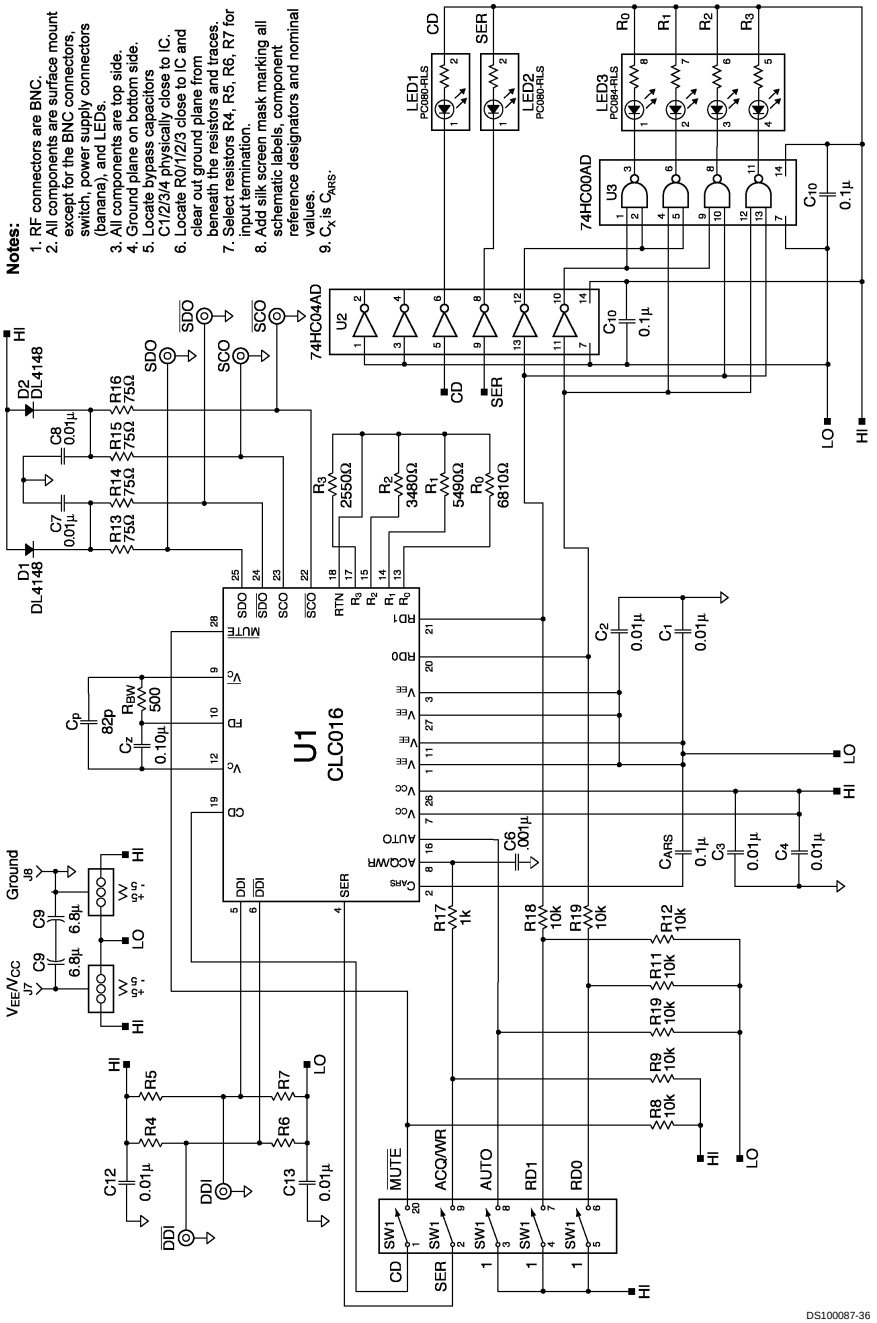
1. Use a ground plane.
2. De-couple V_{CC}/V_{EE} power pins with 0.01 µF ceramic capacitors placed ≤0.1" (3mm) from the power pins and 6.8 µF tantalum capacitors.
3. For long signal runs, match transmission lines to the desired characteristic impedance for the input and output lines.
4. Remove ground plane 0.025" (0.06mm) from all pads.
5. Remove ground plane from the area around the loop filter and frequency selection resistors.
6. Keep digital and analog lines sufficiently away from loop filter or frequency selection resistors.
7. Avoid the use of sockets in production boards.
8. In proto-boards use a low-profile, low impedance, type socket.

EVALUATION BOARD

An evaluation board layout and schematic are shown on the following page. The art work shows the board solder masks, trace layers, and ground plane. ***To order an evaluation board, contact your local sales representative or National support center and request part number CLC730057.***

The evaluation board provides LEDs and switches to operate the PLL in various modes. The board allows the user to select +5V or −5.2V power supplies, identified on the printed board silk screen. Insert all tantalum capacitors as shown in the schematic or silk screen. A complete bill of materials is given in the following table. The components recommended in the materials list are for SMPTE 259M standards.

Product Description (Continued)



Schematic for Evaluation Board CLC730057

Product Description (Continued)

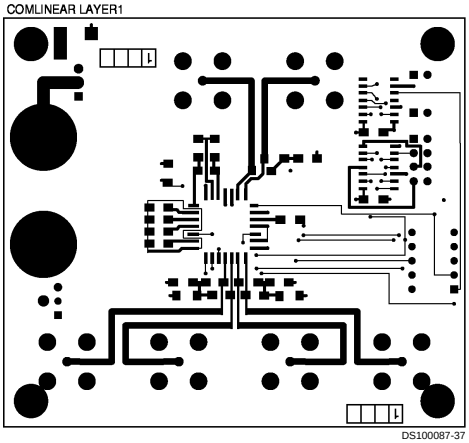
CLC730057 Retimer Evaluation Board Material List

Item	Reference Designator	Description	Qty
1	U1	CLC016AJQ Retimer Chip	1
2	U2	74HC04 Hex Inv. 14 PIN SOIC	1
3	U3	74HC00 Quad 2-Input Pos-Nand Gate	1
4	V_{EE}/V_{CC}	Banana Jack, Red, EF Johnson #108-0902-001	1
5	Gnd	Banana Jack, Black, EF Johnson #108-0993-001	1
6	DDI, $\overline{\text{DDI}}$, SDO, $\overline{\text{SDO}}$, SCO, $\overline{\text{SCO}}$	BNC PC Amphenol #31-5329-52RFX	6
7	C6	0.001 µF SMD Cap, Size 1206	1
8	C1, C2, C3, C4, C7, C8, C12, C13	0.01 µF SMD Cap, Size 1206	8
9	C10, C11, CX, C_Z	0.1 µF SMD Cap, Size 1206	4
10	C_P	82 pF SMD Cap, Size 1206	1
11	C5, C9	6.8 µF SMD Cap, Tantalum Cap, Size 6032 Digikey #PCT3685	2
12	SW1	5 Position Dip Switch Grayhill #GH1216	1
13	D1, D2	DL4148-ND Switching Diode (1N4148 or equivalent)	2
14	RT0, RT1, RT2, RT3	Sub-miniature PCB Mount LED Array PC084-GL5	1
15	CD, UNL	Single Sub-miniature PCB Mount LED PC080-RL5	2
16	R_{BW}	499Ω SMD Resistor, Size 1206	1
17	R8–R12, R18, R19	10 kΩ SMD Resistor, Size 1206	7
18	R17	1 kΩ SMD Resistor, Size 1206	1
19	R13–R16	75Ω SMD Resistor, Size 1206	4
20	R_3	2550Ω SMD 1% Resistor, Size 1206	1
21	R_2	3480Ω SMD 1% Resistor, Size 1206	1
22	R_1	5490Ω SMD 1% Resistor, Size 1206	1
23	R_0	6810Ω SMD 1% Resistor, Size 1206	1
24	R4, R5, R6, R7	Choose for input termination	4
25		Socket Digikey #A2141-ND	1

Product Description (Continued)

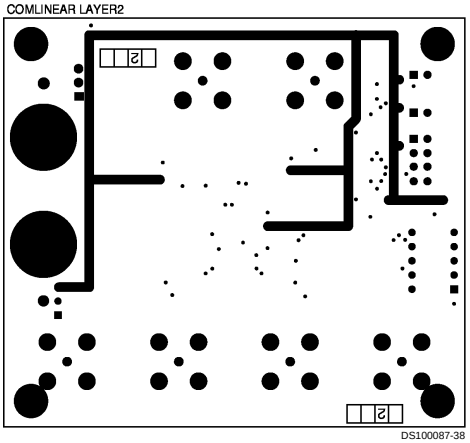
The PC board plots consist of 4-layers depicting signal traces, power planes and ground planes for the CLC730057 evaluation board. Layers not to scale.

COMLINEAR LAYER1



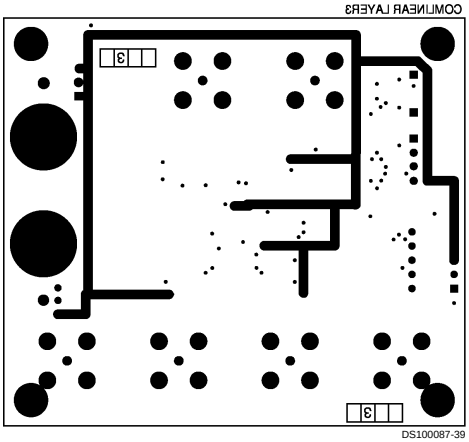
DS100087-37

COMLINEAR LAYER2



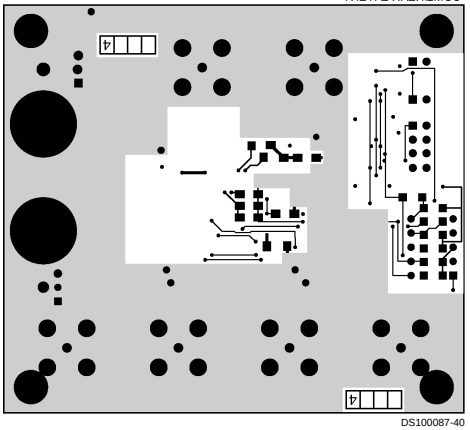
DS100087-38

COMLINEAR LAYER3



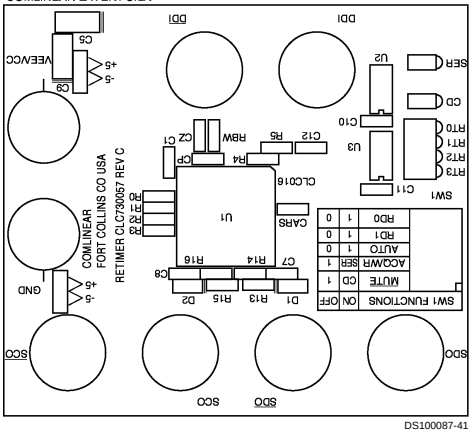
DS100087-39

COMLINEAR LAYER4



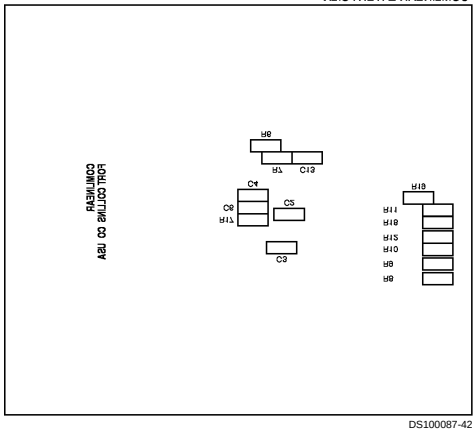
DS100087-40

COMLINEAR LAYER1 SILK



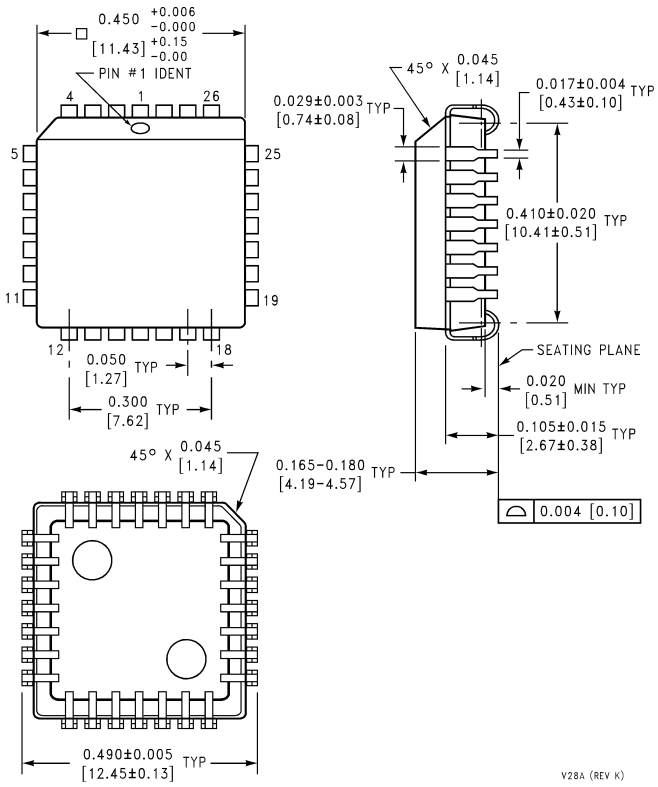
DS100087-41

COMLINEAR LAYER4 SILK



DS100087-42

Physical Dimensions inches (millimeters) unless otherwise noted



Order Number CLC016ACQ or CLC016AJQ
NS Package Number V28A

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