

# CLC115

## Quad, Closed-Loop Monolithic Buffer

### General Description

The CLC115 is a high performance, closed-loop, quad buffer designed for high density applications requiring a low-cost-per-channel solution to buffering high-frequency signals. The CLC115's high performance includes a 700MHz small signal bandwidth (0.5Vpp) and a 2700V/ $\mu$ s slew rate while requiring only 11mA quiescent current per channel. Signal fidelity is maintained with low harmonic distortion ( $-62$ dBc 2nd and 3rd harmonics at 20MHz), and wide channel separation (60dB crosstalk at 10MHz).

Featuring a unique closed-loop design, the CLC115 offers true unity-gain stability and very low output impedance plus a 60mA per channel output drive capability. The CLC115 is ideally suited for buffering video signals with its 0.08%/0.04° differential gain and phase performance at 3.58MHz. Applications such as analog multiplexing and high-speed A/D converters will benefit from the CLC115's high signal fidelity.

The CLC115 offers a low-cost-per-channel solution to high-speed buffering with four high-performance, closed-loop buffers integrated in one 14-pin package.

Constructed using an advanced, complimentary bipolar process and National's proven current feedback architectures, the CLC115 is available in several versions to meet a variety of requirements.

CLC115AJP	-40°C to +85°C	8-pin plastic DIP
CLC115AJE	-40°C to +85°C	8-pin plastic SOIC
CLC115ALC	-40°C to +85°C	dice
CLC115AMC	-55°C to +125°C	dice qualified to Method 5008, MIL-STD-883, Level B MIL-STD-883, Level B

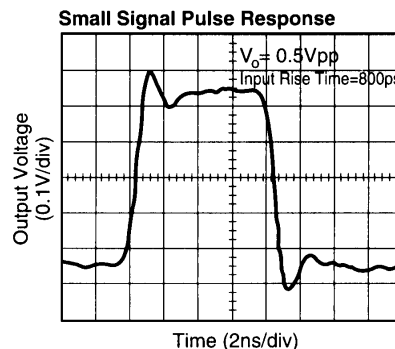
Contact factory for other packages and DESC SMD number.

### Features

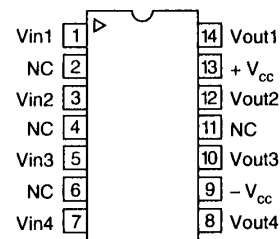
- Closed-loop, quad buffer
- 700MHz small-signal bandwidth
- 270V/ $\mu$ s slew rate
- 0.08%/0.04° differential gain/phase
- 60dB channel isolation (10MHz)
- $-62$ dBc 2nd and 3rd harmonics at 20MHz
- 60mA current output per channel

### Applications

- Multi-channel video distribution
- Video switching buffers
- High-speed analog multiplexing
- Channelized EW
- High-density buffering
- Instrumentation amps
- Active filters



### Pinout



## CLC115 Electrical Characteristics ( $V_{cc} = \pm 5V$ , $R_L = 100\Omega$ ; unless specified)

PARAMETERS	CONDITIONS	TYP	MAX AND MIN RATINGS				UNITS	SYMBOL
			- 40°C	+ 25°C	+ 25°C	+ 85°C		
Ambient Temperature	CLC115AJ	+ 25°C	- 40°C	+ 25°C	+ 85°C			
<b>FREQUENCY DOMAIN RESPONSE</b>								
- 3dB bandwidth	$V_{out} < 0.5V_{pp}$	700	400	400	300	MHz	SSBW	
	$V_{out} < 4V_{pp}$	270	200	200	150	MHz	LSBW	
gain flatness	$V_{out} < 0.5V_{pp}$							
flatness	DC to 30MHz <sup>1</sup>	± 0.0	± 0.1	± 0.1	± 0.1	dB	GFL	
peaking	30MHz to 200MHz	0.4	1.4	1.0	1.0	dB	GFPH	
rolloff	30MHz to 200MHz	0.0	0.5	0.5	0.5	dB	GFRH	
differential gain	4.43MHz, 150Ω load	0.08	0.25	0.15	0.15	%	DG	
differential phase	4.43MHz, 150Ω load	0.04	0.08	0.08	0.08	°	DP	
crosstalk (all hostile)	10MHz	60	57	57	57	dB	XT	
<b>TIME DOMAIN RESPONSE</b>								
rise and fall time	4V step	1.4	2.0	2.0	2.4	ns	TRS	
settling time to 0.1%	2V step	12	17	17	17	ns	TS	
overshoot	4V step input $t_{rise} < 4ns$	5	15	12	12	%	OS1	
	input $t_{rise} > 4ns$	0	2	2	2	%	OS2	
slew rate		2700	2200	2200	1800	V/μs	SR	
<b>DISTORTION AND NOISE RESPONSE</b>								
2nd harmonic distortion	$2V_{pp}$ , 20MHz	- 62	- 45	- 47	- 47	dBc	HD2	
3rd harmonic distortion	$2V_{pp}$ , 20MHz	- 62	- 53	- 53	- 50	dBc	HD3	
equivalent noise input								
noise floor	>1MHz	- 157	- 155	- 155	- 154	dBm <sub>1Hz</sub>	SNF	
<b>STATIC DC PERFORMANCE</b>								
small signal gain	no load	0.995	0.97	0.99	0.99	V/V	GA	
integral endpoint linearity	± 2V, full scale	0.2	1.4	0.5	0.5	%	ILIN	
*output offset voltage		± 2	± 17	± 9	± 9	mV	VIO	
average temperature coefficient		± 25	± 100	-	± 50	μV/°C	DVIO	
*input bias current		± 8	± 35	± 20	± 20	μA	IBN	
average temperature coefficient		± 66	± 187	-	± 125	nA/°C	DIBN	
power supply rejection ratio		54	46	48	46	dB	PSRR	
*supply current	total, no load	45	61	61	61	mA	ICC	
<b>MISCELLANEOUS PERFORMANCE</b>								
input resistance		750	100	450	450	kΩ	RIN	
input capacitance		1.6	2.2	2.2	2.2	pF	CIN	
output resistance	DC	1.1	4.5	2.0	2.0	Ω	RO	
output voltage range	no load	± 4.0	± 3.8	± 3.9	± 3.9	V	VO	
output voltage range	$R_L = 100\Omega$	± 3.7	± 2.2	± 3.4	± 3.0	V	VOL	
output current		± 60	± 25	± 48	± 30	mA	IO	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

### Absolute Maximum Ratings

$V_{cc}$	± 7V
$I_{out}$	output is short circuit protected to ground, however, maximum reliability is obtained if $I_{out}$ does not exceed... 80mA
input voltage	± $V_{cc}$
maximum junction temperature	+ 150°C
operating temperature range	
AJ:	- 40°C to + 85°C
storage temperature range	- 65°C to + 150°C
lead temperature (soldering 10 sec)	+ 300°C
ESD	≥ 4000V

### Miscellaneous Ratings

NOTES:

- \* AJ 100% tested at + 25°C.
- note 1: Specification is guaranteed for ( $50\Omega \leq R_L \leq 200\Omega$ ).

### Package Thermal Resistance

Package	$\theta_{JC}$	$\theta_{JA}$
Plastic (AJP)	55°C/W	105°C/W
Surface Mount (AJE)	45°C/W	115°C/W

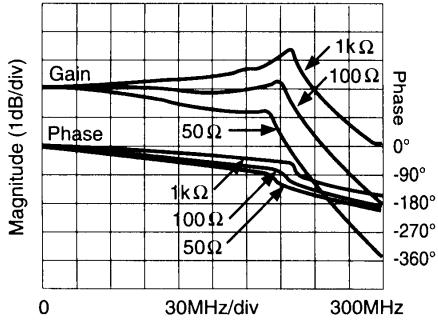
### Reliability Information

Transistor Count

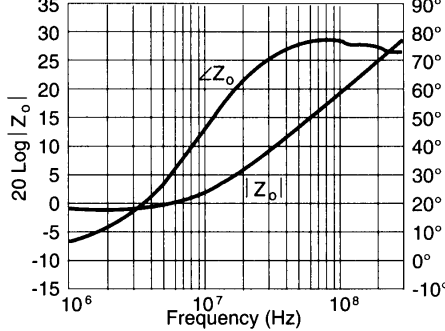
64

# CLC115 Typical Performance Characteristics ( $T_A = +25^\circ\text{C}$ , $V_{CC} = \pm 5\text{V}$ , $R_L = 100\Omega$ ; unless specified)

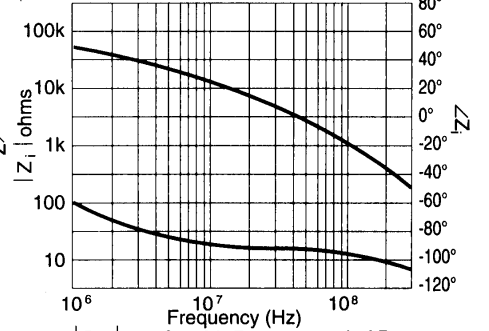
**Gain and Phase vs. Load ( $V_o = 4\text{Vpp}$ )**



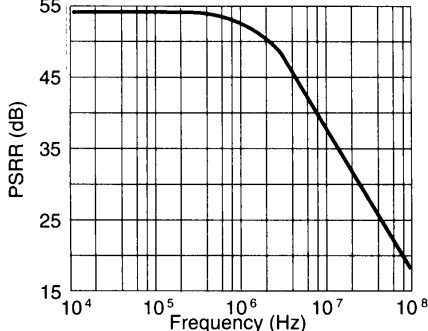
**Output Impedance**



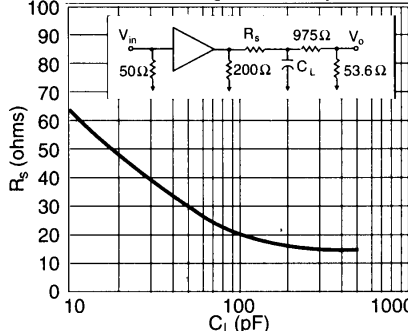
**Input Impedance**



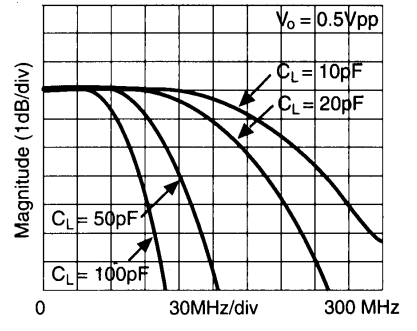
**PSRR**



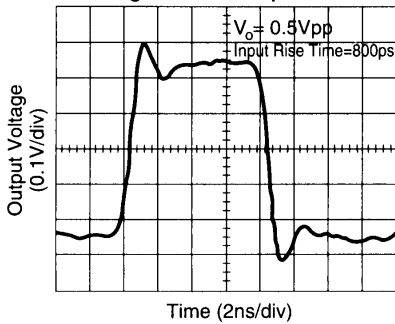
**Recommended  $R_s$  vs. Load Capacitance**



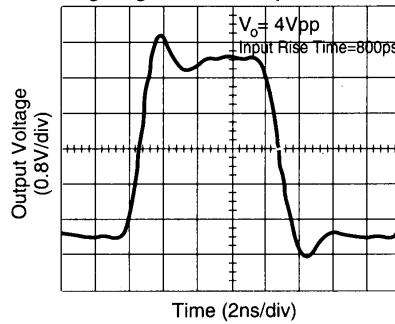
**|S<sub>21</sub>| vs. C<sub>L</sub> with Recommended R<sub>s</sub>**



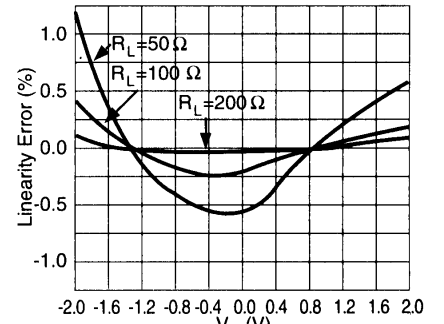
**Small Signal Pulse Response**



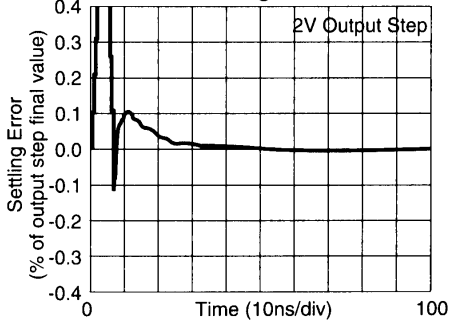
**Large Signal Pulse Response**



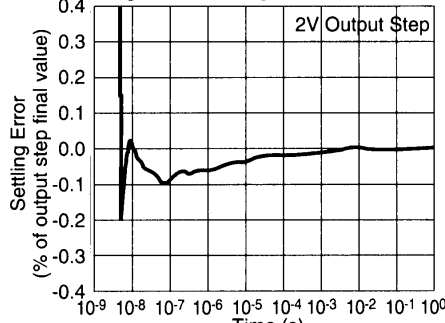
**Integral Linearity Error**



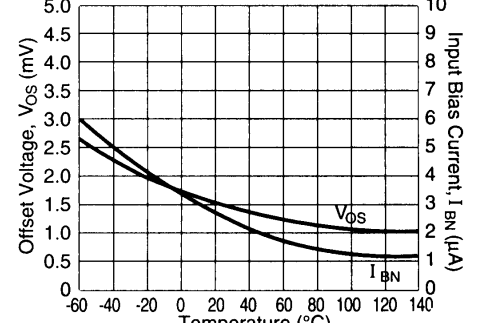
**Short-Term Settling Time**



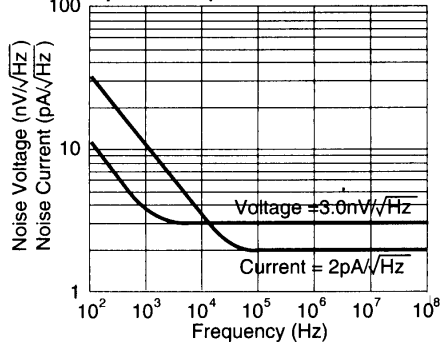
**Long-Term Settling Time**



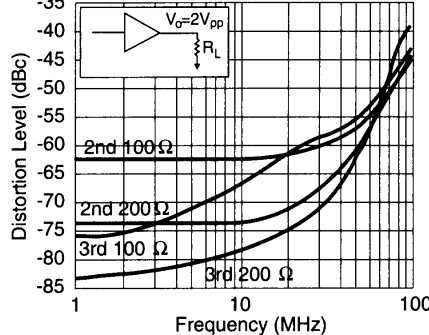
**Typical D.C. Errors vs. Temperature**



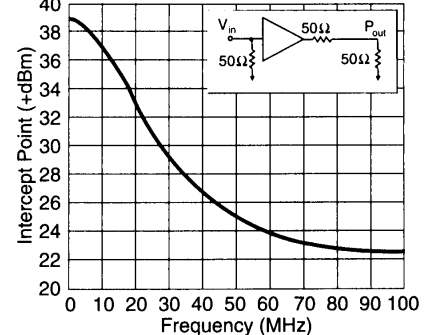
**Equivalent Input Noise**



**2nd and 3rd Harmonic Distortion**



**2-Tone, 3rd Order Intermodulation Intercept**



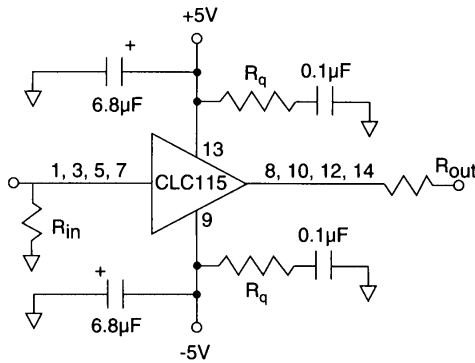


Figure 1: recommended circuit

### PC Board Layout and Circuit Design

For optimum performance, high frequency devices demand a good printed circuit board layout. A ground plane and power supply bypassing with good high-frequency ceramic capacitors in close proximity to the supply pins is essential. Second harmonic distortion can be improved by ensuring equal current return paths for both the positive and negative supplies.

The dominant pole, i.e. the high-frequency compensation of the CLC115, is set by the load resistance,  $R_L$ . Ideally, each buffer of the CLC115 should see a  $100\Omega$  load at high frequency to ensure stability. An unterminated channel is undercompensated and will exhibit gain at several hundred megahertz. Signal coupling may occur between channels through the common power supply connections. Any resonance in the power supply can lead to oscillations in the unterminated or undercompensated channel.

In order to compensate and to guarantee the stability of the four CLC115 channels, each must be terminated with a  $100\Omega$  resistance to ground. If a dc load is not desired, a two picofarad capacitor can be inserted between the  $100\Omega$  load resistor and ground, as shown in Figure 2.

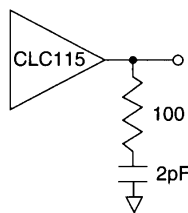


Figure 2: AC load

If the above load conditions are not feasible for your design, the power supply resonance must be addressed. Chip capacitors have less parasitic inductance than leaded ceramic capacitors. The use of  $0.1\mu\text{F}$  chip capacitors mounted immediately adjacent to the power supply pins eliminates the resonance which can lead to oscillations. If chip capacitors are not used, then the only other means to eliminate the possibility of oscillation caused by power supply resonance is to 'de-Q' the resonant structure. 'De-Q'ing is particularly necessary while using leaded capacitors and can be achieved by inserting a  $10\Omega$  resistor,  $R_q$ , in series with the  $0.1\mu\text{F}$  bypass capacitor, as shown in Figure 1. The insertion of the 'de-Q'ing resistor will reduce frequency response peaking as well as the tendency toward oscillation when driving a load resistance greater than  $100\Omega$ , but will increase harmonic distortion by approximately 2dB.

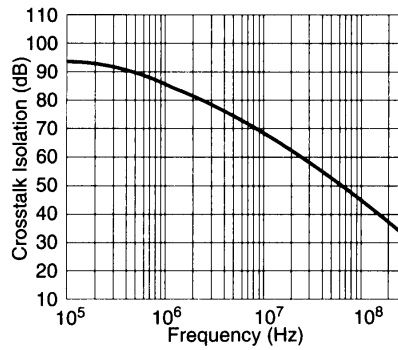


Figure 3: all-hostile crosstalk isolation

**Crosstalk** is strongly dependent on board layout. Closely spaced signal traces on the circuit board will degrade crosstalk due to intertrace capacitance. It is recommended that unused package pins (2,4,6,11) be connected to the ground plane for better isolation at the device pins. Similarly, crosstalk can be improved by using a grounded guard-trace between signal lines. This will reduce the distributed capacitance between signal lines.

Two graphs show the effects of crosstalk. All-hostile crosstalk is measured by driving three of the four buffers simultaneously while observing the fourth, undriven channel. Figure 3, "All-Hostile Crosstalk Isolation", shows this effect as a function of input signal frequency. The load for all four channels of the CLC115 is  $100\Omega$ . Figure 4, "Most Susceptible Channel-to-Channel Pulse Coupling", describes one effect of crosstalk when one channel is driven with a  $4V_{pp}$  step ( $t_r=5\text{ns}$ ) while the output of the undriven channel is measured. From Figure 3 it can be seen that crosstalk improves as the signal frequency is reduced. Similarly, the pulse coupling crosstalk will improve as the time increases.

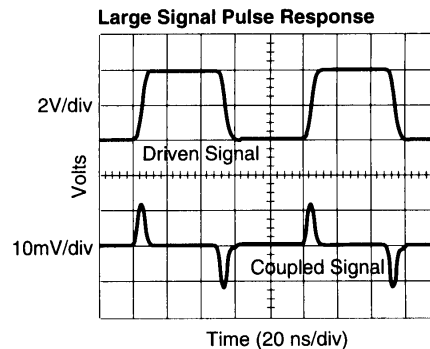


Figure 4: most susceptible channel-to-channel pulse coupling

### Unused Buffers

The output of any unused buffers must be terminated in  $100\Omega$  to ground, as discussed above. It is recommended that unused buffer inputs be terminated in  $50\Omega$  to ground.

### Evaluation Board

An evaluation board for the CLC115 is available. This board may be ordered as part CLC730023.

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