

CLC410

Fast Settling, Video Op Amp with Disable

General Description

The current-feedback CLC410 is a fast-settling, wideband, monolithic op amp with fast disable/enable feature. Designed for low-gain applications ($A_V = \pm 1$ to ± 8), the CLC410 consumes only 160mW of power (180mW max) yet provides a -3dB bandwidth of 200MHz ($A_V = +2$) and 0.05% settling in 12ns (15ns max). Plus, the disable feature provides fast turn-on (100ns) and turn-off (200ns). In addition, the CLC410 offers both high performance and stability without compensation — even at a gain of +1.

The CLC410 provides a simple, high-performance solution for video switching and distribution applications, especially where analog buses benefit from use of the disable function to “multiplex” signals onto the bus. Differential gain/phase of 0.01%/0.01° provide high fidelity and the 70mA output current offers ample drive capability.

The CLC410’s fast settling, low distortion, and high drive capabilities make it an ideal ADC driver. The low 160mW quiescent power consumption and very low 40mW disabled power consumption suggest use where power is critical and/or “system off” power consumption must be minimized.

The CLC410 is available in several versions to meet a variety of requirements. A three-letter suffix determines the version:

| | | |
|-----------|-----------------|--|
| CLC410AJP | -40°C to +85°C | 8-pin plastic DIP |
| CLC410AJE | -40°C to +85°C | 8-pin plastic SOIC |
| CLC410ALC | -40°C to +85°C | dice |
| CLC410AMC | -55°C to +125°C | dice qualified to Method 5008, MIL-STD-883, Level B |
| CLC410A8B | -55°C to +125°C | 8-pin hermetic CERDIP, MIL-STD-883, Level B |

DESC SMD number: 5962-90600

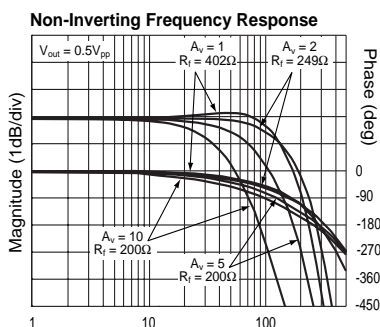
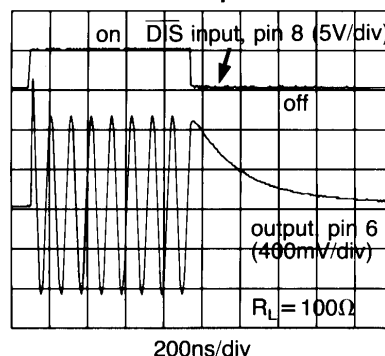
Features

- -3dB bandwidth of 200MHz
- 0.05% settling in 12ns
- Low power, 160mW (40mW disabled)
- Low distortion, -60dBc at 20MHz
- Fast disable (200ns)
- Differential gain/phase: 0.01%/0.01°
- ± 1 to ± 8 closed-loop gain range

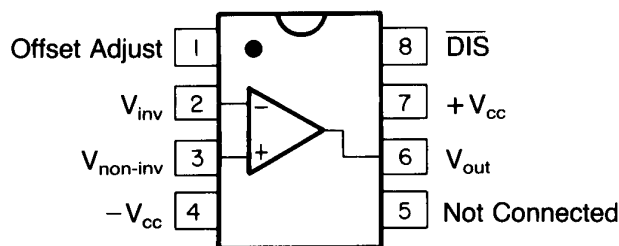
Applications

- Video switching and distribution
- Analog bus driving (with disable)
- Low power “standby” using disable
- Fast, precision A/D conversion
- D/A current-to-voltage conversion
- IF processors
- High-speed communications

Enable/Disable Response



Pinout DIP & SOIC



CLC410 Electrical Characteristics ($A_V = +2$, $V_{CC} = \pm 5V$, $R_L = 100\Omega$, $R_f = 250\Omega$; unless specified)

| PARAMETER | CONDITIONS | TYP | MAX & MIN RATINGS | | | | UNITS | SYMBOL |
|---|-------------------------------|-----------|-------------------|-------------|-------------|------------------|-------|--------|
| | | | -40°C | +25°C | +85°C | | | |
| Ambient Temperature | CLC410AJ | +25°C | -40°C | +25°C | +85°C | | | |
| FREQUENCY DOMAIN RESPONSE | | | | | | | | |
| -3dB bandwidth | $V_{out} < 0.5V_{pp}$ | 200 | >150 | >150 | >120 | MHz | SSBW | |
| | $V_{out} < 5V_{pp}, A_V = +5$ | 50 | >35 | >35 | >35 | MHz | LSBW | |
| gain flatness | $V_{out} < 0.5V_{pp}$ | | | | | | | |
| peaking | DC to 40MHz | 0 | <0.4 | <0.3 | <0.4 | dB | GFPL | |
| peaking | >40MHz | 0 | <0.7 | <0.5 | <0.7 | dB | GFPH | |
| rolloff | DC to 75MHz | 0.6 | <1 | <1 | <1.3 | dB | GFR | |
| linear phase deviation | DC to 75MHz | 0.2 | <1 | <1 | <1.2 | ° | LPD | |
| TIME DOMAIN RESPONSE | | | | | | | | |
| rise and fall time | 0.5V step | 1.6 | <2.4 | <2.4 | <2.4 | ns | TRS | |
| | 5V step | 6.5 | <10 | <10 | <10 | ns | TRL | |
| settling time to $\pm 0.1\%$ | 2V step | 10 | <13 | <13 | <13 | ns | TSP | |
| $\pm 0.05\%$ | 2V step | 12 | <15 | <15 | <15 | ns | TS | |
| overshoot | 0.5V step | 0 | <15 | <10 | <10 | % | OS | |
| slew rate $A_V = +2$ | | 700 | >430 | >430 | >430 | V/ μs | SR | |
| $A_V = -2$ | | 1600 | — | — | — | V/ μs | SR1 | |
| DISTORTION AND NOISE RESPONSE | | | | | | | | |
| 2nd harmonic distortion | $2V_{pp}, 20MHz$ | -60 | <-40 | <-45 | <-45 | dBc | HD2 | |
| 3rd harmonic distortion | $2V_{pp}, 20MHz$ | -60 | <-50 | <-50 | <-50 | dBc | HD3 | |
| equivalent input noise | | | | | | | | |
| noise floor | >1MHz ¹ | -157 | <-154 | <-154 | <-153 | dBm(1Hz) | SNF | |
| integrated noise | 1MHz to 200MHz ¹ | 40 | <54 | <57 | <63 | μV | INV | |
| differential gain ² | (see plots) | 0.01 | 0.05 | 0.04 | 0.04 | % | DG | |
| differential phase ² | (see plots) | 0.01 | 0.1 | 0.02 | 0.02 | ° | DP | |
| DISABLE/ENABLE PERFORMANCE | | | | | | | | |
| disable time to >50dB attenuation at 10MHz | | 200 | <1000 | <1000 | <1000 | ns | TOFF | |
| enable time | | 100 | <200 | <200 | <200 | ns | TON | |
| DIS voltage | | | | | | | | |
| to disable | | 1.0 | 0.5 | 0.5 | 0.5 | V | VDIS | |
| to enable | | 2.6 | 2.3 | 3.2 | 4.0 | V | VEN | |
| DIS current (sourced from CLC410, see figure 4) | | | | | | | | |
| to disable | | 200 | 250 | 250 | 250 | μA | IDIS | |
| to enable | | 80 | 60 | 60 | 60 | μA | IEN | |
| off isolation | at 10MHz | 59 | >55 | >55 | >55 | dB | OSD | |
| STATIC, DC PERFORMANCE | | | | | | | | |
| *input offset voltage | | 2 | < ± 8.2 | < ± 5.0 | < ± 9.0 | mV | VIO | |
| average temperature coefficient | | 20 | < ± 40 | — | < ± 40 | $\mu V/^\circ C$ | DVIO | |
| *input bias current | non-inverting | 10 | < ± 36 | < ± 20 | < ± 20 | μA | IBN | |
| average temperature coefficient | | 100 | < ± 200 | — | < ± 100 | nA/ $^\circ C$ | DIBN | |
| *input bias current | inverting | 10 | < ± 36 | < ± 20 | < ± 30 | μA | IBI | |
| average temperature coefficient | | 50 | < ± 200 | — | < ± 100 | nA/ $^\circ C$ | DIBI | |
| power supply rejection ratio | | 50 | >45 | >45 | >45 | dB | PSRR | |
| common mode rejection ratio | | 50 | >45 | >45 | >45 | dB | CMRR | |
| *supply current | no load, quiescent | 16 | <18 | <18 | <18 | mA | ICC | |
| supply current, disabled | no load, quiescent | 4 | <6 | <6 | <6 | mA | ISD | |
| MISCELLANEOUS PERFORMANCE | | | | | | | | |
| non-inverting input | resistance | 200 | >50 | >100 | >100 | kohm | RIN | |
| | capacitance | 0.5 | <2 | <2 | <2 | pF | CIN | |
| output impedance | at DC | 0.1 | <0.2 | <0.2 | <0.2 | ohm | RO | |
| output impedance, disabled | resistance, at DC | 200 | >100 | >100 | >100 | kohm | ROD | |
| | capacitance, at DC | 0.5 | <2 | <2 | <2 | pF | COD | |
| output voltage range | no load | ± 3.5 | > ± 3 | > ± 3.2 | > ± 3.2 | V | VO | |
| common mode input range for rated performance | | ± 2.1 | > ± 1.2 | > ± 2 | > ± 2 | V | CMIR | |
| output current | -40°C to +85°C | ± 70 | > ± 35 | > ± 50 | > ± 50 | mA | IO | |
| | -55°C to +125°C | ± 60 | > ± 30 | > ± 50 | > ± 50 | mA | IO | |

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

| | |
|--|--|
| V_{cc} | $\pm 7V$ |
| I_{out} | output is short circuit protected to ground, however, maximum reliability is obtained if I_{out} does not exceed... 60mA |
| common mode input voltage | $\pm V_{cc}$ |
| differential input voltage | 5V |
| disable input voltage (pin 8) | $+V_{cc}, -1V$ |
| applied output voltage when disabled | $\pm V_{cc}$ |
| junction temperature | $+150^{\circ}C$ |
| operating temperature range | AJ: $-40^{\circ}C$ to $+85^{\circ}C$ |
| storage temperature range | $-65^{\circ}C$ to $+150^{\circ}C$ |
| lead solder duration ($+300^{\circ}C$) | 10 sec |
| ESD rating (human body model) | 500V |

Miscellaneous Ratings

| | |
|------------------------|--|
| recommended gain range | ± 1 to ± 8 |
| Notes: | |
| * | AJ 100% tested at $+25^{\circ}C$. |
| note 1: | Noise tests are performed from 5MHz to 200MHz. |
| note 2: | Differential gain and phase measured at: $A_v = +2$, $R_f = 250\Omega$, $R_g = 150\Omega$ $1V_{pp}$ equivalent video signal, 0-100 IRE, 40IRE _{pp} , 3.58 MHz, 0IRE = 0 volts, at 75Ω load. See text. |

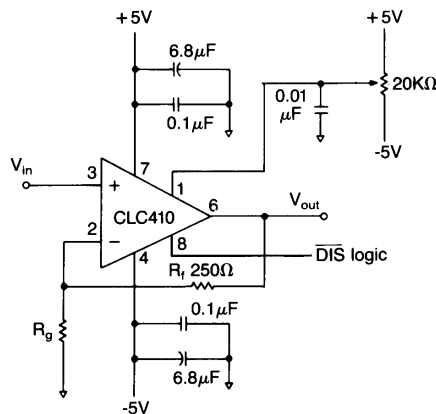
Reliability Information

| | |
|------------------|----|
| Transistor count | 29 |
|------------------|----|

Package Thermal Resistance

| Package | θ_{JC} | θ_{JA} |
|---------|---------------|---------------|
| AJP | 65°C/W | 120°C/W |
| AJE | 60°C/W | 140°C/W |
| CERDIP | 35°C/W | 125°C/W |

Figure 1:
recommended
non-inverting gain
circuit



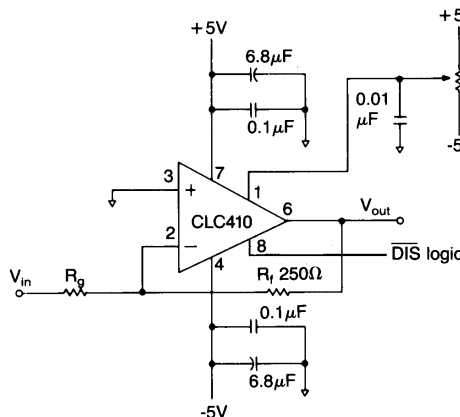
offset voltage adjustment circuit (optional – except for capacitor, which improves fine scale settling time)

$$A_v = 1 + \frac{R_f}{R_g}$$

For optimum performance, R_f and R_g should be low-inductance, low-capacitance resistors.

(Pin designations are for DIP versions.)

Figure 2:
recommended
inverting gain
circuit



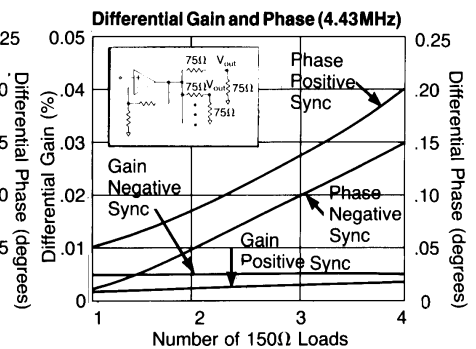
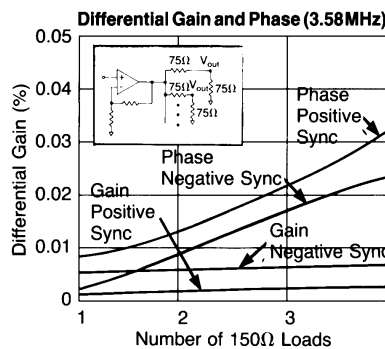
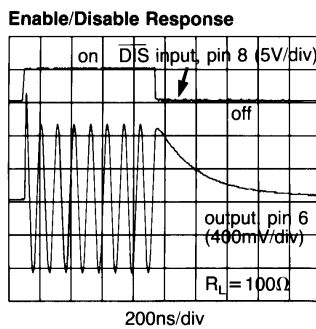
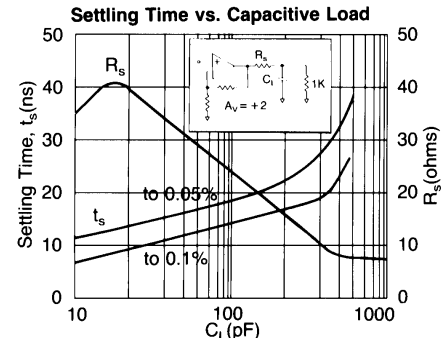
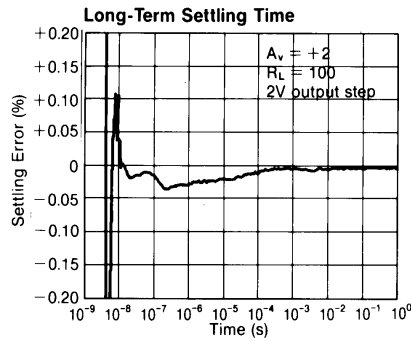
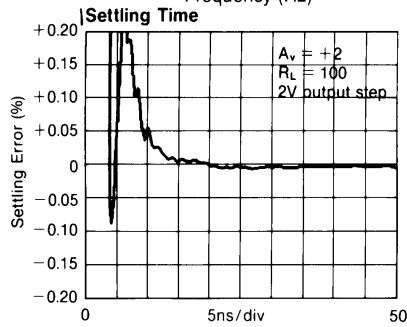
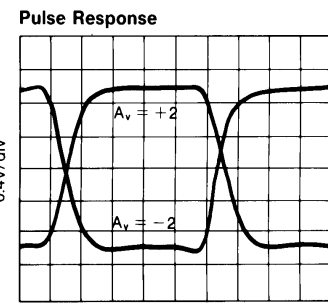
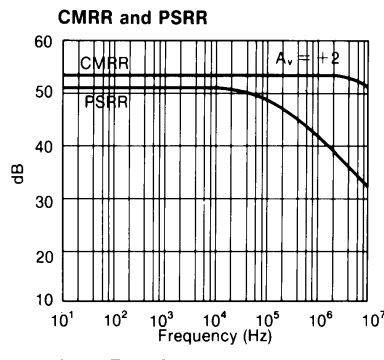
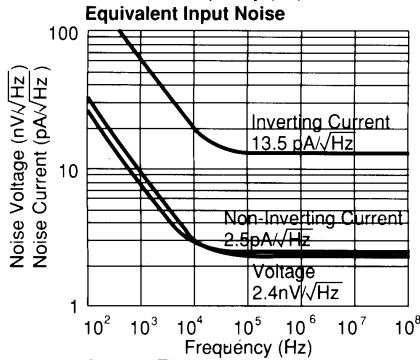
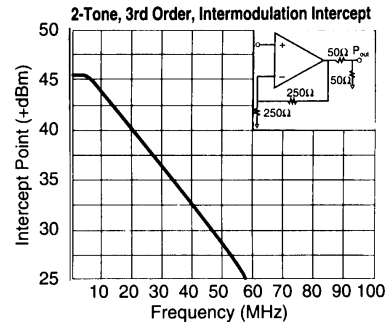
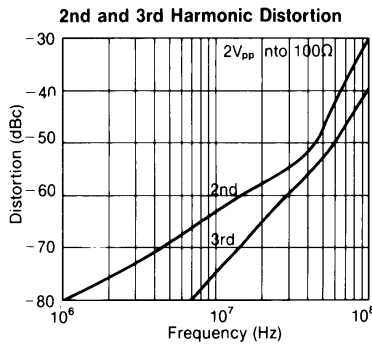
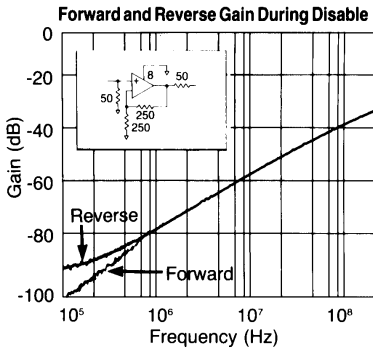
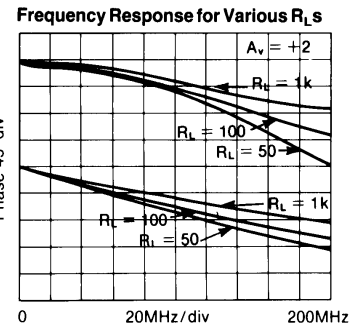
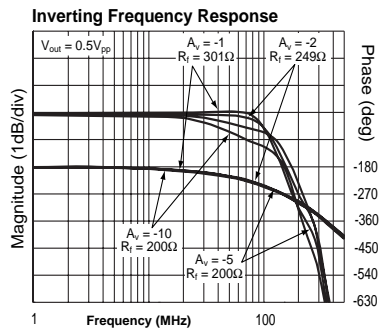
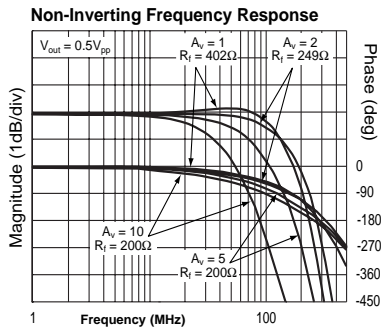
offset voltage adjustment circuit (optional – except for capacitor, which improves fine scale settling time)

$$A_v = -\frac{R_f}{R_g}$$

For optimum performance, R_f and R_g should be low-inductance, low-capacitance resistors.

(Pin designations are for DIP versions.)

CLC410 Typical Performance Characteristics ($T_A = 25^\circ$, $A_V = +2$, $V_{CC} = \pm 5V$, $R_L = 100\Omega$; unless specified)



Enable/Disable Operation

The CLC410 has an enable/disable feature that is useful for conserving power and for multiplexing the outputs of several amplifiers onto an analog bus (figure 3A). Disabling an amplifier while not in use reduces power supply current and the output and inverting input pins become a high impedance.

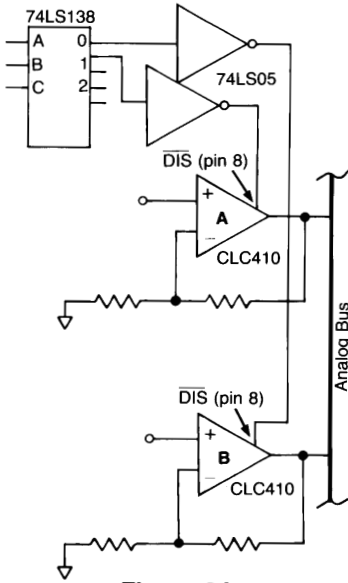


Figure 3A

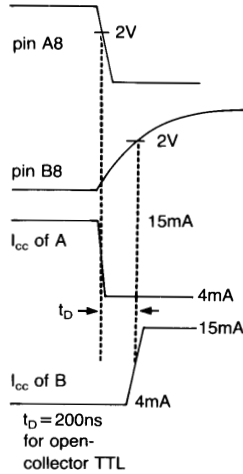


Figure 3B

Pin 8, the $\overline{\text{DIS}}$ pin, can be driven from either open-collector TTL or from 5V CMOS. A logic low disables the amplifier and an internal 15K Ω pull-up resistor ensures that the amplifier is enabled if pin 8 is not connected (figure 4). Both TTL and 5V CMOS logic are guaranteed to drive a high enough high-level output voltage (V_{OH}) to ensure that the CLC410 is enabled. Whichever type used, "break-before-make" operation should be established when outputs of several amplifiers are connected together. This is important for avoiding large, transient currents flowing between amplifiers when two or more are simultaneously enabled. Typically, proper operation is ensured if all the amplifiers are driven from the same decoder integrated circuit because logic output rise times tend to be longer than fall times. As a result, the amplifier being disabled will reach the 2V threshold sooner than the amplifier being enabled (see t_D of figure 3B timing diagram).

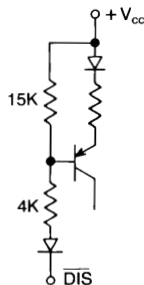


Figure 4: equivalent of $\overline{\text{DIS}}$ input

During disable, supply current drops to approximately 4mA and the inverting input and output pin impedances become 200K Ω || 0.5pF each. The total impedance that a disabled amplifier and its associated feedback network presents to the analog bus is determined from figure 5. For example,

at a non-inverting gain of 1, the output impedance at video frequencies is 100K Ω || 1pF since the 250 Ω feedback resistor is a negligible impedance. Similarly, output impedance is 500 Ω || 0.5pF at a non-inverting gain of 2 (with $R_F = R_G = 250\Omega$).

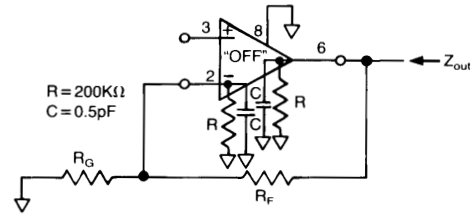


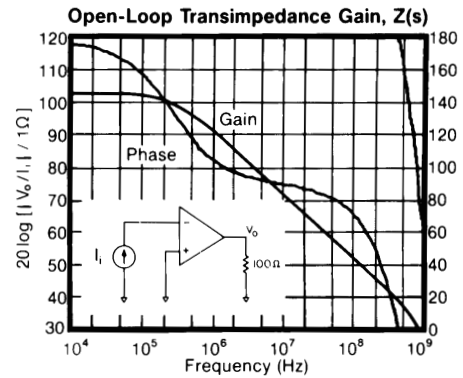
Figure 5

Differential Gain and Phase

Plots on the preceding page illustrate the differential gain and phase performance of the CLC410 at both 3.58 and 4.43MHz. Application Note OA-08 presents a measurement technique for measuring the very low differential gain and phase of the CLC410. Observe that the gain and phase errors remain low even as the output loading increases, making the device attractive for driving multiple video outputs.

Understanding the Loop Gain

The CLC410 is a current-feedback op amp. Referring to the equivalent circuit of figure 6, any current flowing in the inverting input is amplified to a voltage at the output through the transimpedance gain shown below. This $Z(s)$ is analogous to the open-loop gain of a voltage feedback amplifier.



Developing the non-inverting frequency response for the topology of Figure 3 yields:

$$\frac{V_o}{V_i} = \frac{1 + R_f / R_g}{1 - 1 / \text{LG}} \quad \text{eq. (1)}$$

where LG is the loop gain defined by,

$$\text{LG} = \frac{Z(s)}{R_f} \times \frac{1}{1 + Z_i / (R_f || R_g)} \quad \text{eq. (2)}$$

Equation 1 has a form identical to that for a voltage feedback amplifier with the differences occurring in the LG expression, eq. 2. For an idealized treatment, set $Z_i = 0$ which results in a very simple $\text{LG} = Z(s) / R_f$ (Derivation of the transfer function for the case where $Z_i = 0$ is given in

Application Note AN300-1.) Using the $Z(s)$ (open-loop transimpedance gain) plot shown on the previous page and dividing by the recommended $R_f = 250\Omega$, yields a large loop gain at DC. As a result, equation 1 shows that the closed-loop gain at DC is very close to $(1 + R_f/R_g)$.

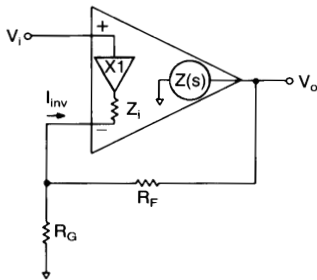


Figure 6: current feedback topology

At higher frequencies, the roll-off of $Z(s)$ determines the closed-loop frequency response which, ideally, is dependent only on R_f . **The specifications reported on the previous pages are therefore valid only for the specified $R_f = 250\Omega$.** Increasing R_f from 250Ω will decrease the loop gain and bandwidth, while decreasing it will increase the loop gain possibly leading to inadequate phase margin and closed-loop peaking. Conversely, fixing R_f will hold the frequency response constant while the closed-loop gain can be adjusted using R_g .

The CLC410 departs from this idealized analysis to the extent that the inverting input impedance is finite. With the low quiescent power of the CLC410, $Z_i \approx 50\Omega$ leading to a drop in loop gain and bandwidth at high gain settings, as given by equation 2. The second term in equation 2 accounts for the division in feedback current that occurs between Z_i and $R_f \parallel R_g$ at the inverting node of the CLC410. This decrease in bandwidth can be circumvented as described in "Increasing Bandwidth at High Gains." Also see "Current Feedback Amplifiers" in the Comlinear Databook for a thorough discussion of current feedback op amps.

Increasing Bandwidth At High Gains

Bandwidth may be increased at high closed-loop gains by adjusting R_f and R_g to make up for the losses in loop gain that occur at these high gain settings due to current division at the inverting input. An approximate relationship may be obtained by holding the LG expression constant as the gain is changed from the design point used in the specifications (that is, $R_f = 250\Omega$ and $R_g = 250\Omega$). For the CLC410 this gives,

$$R_f = 350 - 50A_v \text{ and } R_g = \frac{350 - 50A_v}{A_v - 1} \quad \text{eq. (3)}$$

where A_v is the non-inverting gain. Note that with $A_v = +2$ we get the specified $R_f = 250\Omega$, while at higher gains, a lower value gives stable performance with improved bandwidth.

DC Accuracy and Noise

Since the two inputs for the CLC410 are quite dissimilar, the noise and offset error performance differs somewhat from that of a standard differential input amplifier. Specifically, the inverting input current noise is much larger than the non-inverting current noise. Also the two input

bias currents are physically unrelated rendering bias current cancellation through matching of the inverting and non-inverting pin resistors ineffective.

In equation 4, the output offset is the algebraic sum of the equivalent input voltage and current sources that influence DC operation. Output noise is determined similarly except that a root-sum-of-squares replaces the algebraic sum. R_s is the non-inverting pin resistance.

$$\text{Output Offset } V_o = \pm IBN \times R_s(1 + R_f/R_g) \pm VIO(1 + R_f/R_g) \pm IBI \times R_f \quad \text{eq. (4)}$$

An important observation is that for fixed R_f , offsets as referred to the input improve as the gain is increased (divide all terms by $1 + R_f/R_g$). A similar result is obtained for noise where noise figure improves as gain increases.

The input noise plot shown in the CLC400 datasheet applies equally as well to the CLC410.

Capacitive Feedback

Capacitive feedback should not be used with the CLC410 because of the potential for loop instability. See Application Note OA-7 for active filter realizations with the CLC410.

Offset Adjustment Pin

Pin 1 can be connected to a potentiometer as shown in Fig. 1 and used to adjust the input offset of the CLC410. Full range adjustment of $\pm 5V$ on pin 1 will yield a $\pm 10mV$ input offset adjustment range. Pin 1 should always be bypassed to ground with a ceramic capacitor located close to the package for best settling performance.

Printed Circuit Layout

As with any high frequency device, a good PCB layout will enhance performance. Ground plane construction and good power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal coupling to the ground plane. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

Parasitic or load capacitance directly on the output will introduce additional phase shift in the loop degrading the loop phase margin and leading to frequency response peaking. A small series resistor before the capacitance effectively decouples this effect. The graphs on the preceding page illustrate the required resistor value and resulting performance vs. capacitance.

Precision buffered resistors (PRP8351 series from Precision Resistive Products) with low parasitic reactances were used to develop the data sheet specifications. Precision carbon composition resistors will also yield excellent results. Standard spirally-trimmed RN55D metal film resistors will work with a slight decrease in bandwidth due to their reactive nature at high frequencies.

Evaluation PC boards (part numbers CLC730013 for through-hole and CLC730027 for SOIC) for the CLC404 are available.

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