National Semiconductor

June 1999

CLC502
Clamping, Low-Gain Op Amp with Fast 14-bit Settling

General Description

The CLC502 is an operational amplifier designed for low-gain applications requiring output voltage clamping. This feature allows the designer to set maximum positive and negative output voltage levels for the amplifier – thus allowing the CLC502 to protect downstream circuitry, such as delicate converter systems, from destructive transients or signals which would otherwise cause saturation. The overload recovery time of only 8ns permits systems to resume operation quickly after overdrive.

High-accuracy systems will also benefit from the CLC502's fast, accurate settling. Settling to 0.0025% in 25ns (32ns guaranteed over temperature), the CLC502 is ideal as the input amplifier in high-accuracy (12 bits and above) A/D systems. Unlike most other high-speed op amps, the CLC502 is free of settling tails. And, as the settling plots show, settling to 0.01% accuracy is an even faster 18ns typical.

The CLC502 is also useful in other applications which require low-gain amplification (± 1 to ± 8) and the clamping or overload recovery features. For example, even low-resolution imaging circuits, which often have to cope with overloading signal levels, can benefit from clamping and overload recovery.

The CLC502 is available in several versions to meet a variety of requirements. A three-letter suffix determines the version:

CLC502AJP	-40°C to +85°C	8-pin plastic DIP
CLC502AJE	-40°C to +85°C	8-pin plastic SOIC

DESC SMD number: 5962-91743

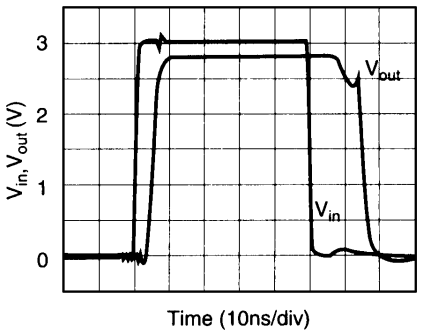
Features

- Output clamping with fast recovery
- 0.0025% settling in 25ns (32ns max.)
- Low power, 170mW
- Low distortion. -50dBc at 20MHz

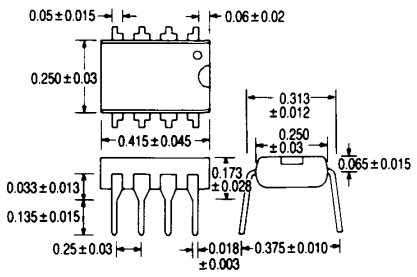
Applications

- Output clamping applications
- High-accuracy A/D systems (12-14 bits)
- High-accuracy D/A converters
- Pulse amplitude modulation systems

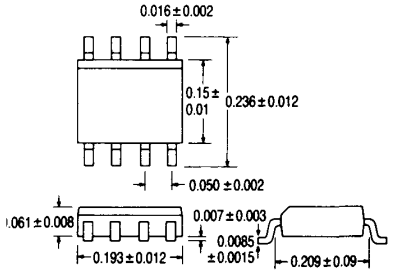
Clamped Pulse Response (8x Overdrive)



Package Dimensions



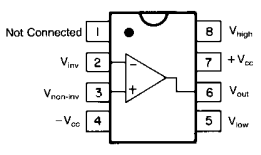
8-pin plastic DIP



8-pin plastic SOIC

Pinout

DIP & SOIC



CLC502 Electrical Characteristics (A_V = +2, V_{cc} = ±5V, R_L = 100Ω, R_f = 250Ω, V_H = +3V, V_L = -3V)

PARAMETER	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC502AJ	+25°C	−40°C	+25°C	+ 85°C		
FREQUENCY DOMAIN PERFORMANCE							
-3dB bandwidth	V_{out} <0.5V_{pp}	150	>100	>110	>100	MHz	SSBW
	V_{out} <5V_{pp}	65	>40	>40	>40	MHz	LSBW
gain flatness	V_{out} <0.5V_{pp}						
peaking	DC to 25MHz	0	<0.4	<0.3	<0.4	dB	GFPL
peaking	>25MHz	0	<0.7	<0.5	<0.7	dB	GFPH
rolloff[2]	DC to 50MHZ	0.5	<1.0	<1.0	<1.0	dB	GFR
linear phase deviation	DC to 50MHZ	0.4	<1.2	<1.0	<1.2	°	LPD
TIME DOMAIN PERFORMANCE							
rise and fall time	0.5V step	2.7	<3.5	<3.2	<3.5	ns	TRS
	5V step	5.0	<8	<8	<8	ns	TRL
settling time to ±0.0025%	2Vstep	25	<32	<32	<32	ns	TS14
±0.01%	2V step	18	<25	<25	<25	ns	TSP
±0.1%	2V step	10	<15	<15	<15	ns	TSS
overshoot	0.5V step	0	<10	<10	<10	%	OS
slew rate		800	>500	>500	>500	V/μs	SR
DISTORTION AND NOISE PERFORMANCE							
2nd harmonic distortion	$2V_{pp}$, 20MHz	−50	<−38	<−43	<−43	dBc	HD2
3rd harmonic distortion	$2V_{pp}$, 20MHz	−60	<−53	<−53	<−53	dBc	HD3
equivalent input noise							
noise floor	>1MHz	−157	<−155	<−155	<−155	dBm(1Hz)	SNF
integrated noise	1MHz to 150MHz	40	<49	<49	<49	μV	INV
differential gain[1]		0.01	—	—	—	%	DG
differential phase[1]		0.05	—	—	—	°	DP
CLAMP PERFORMANCE							
overshoot in clamp	2x overdrive	5	—	<10	—	%	OVC
overload recovery from clamp	2x overdrive	8	<15	<15	<15	ns	TSO
*clamp accuracy	2x overdrive	±0.2	<±0.3	<±0.3	<±0.3	V	VOC
input bias current on V_h, V_l		20	<75	<35	<35	μA	ICL
−3dB bandwidth	V_l or V_h = $2V_{pp}$	50	—	—	—	MHz	CBW
clamp voltage range	V_h or V_l		<± 3.0	<± 3.3	<± 3.3	V	CMC
STATIC, DC PERFORMANCE							
* input offset voltage		0.5	<2.6	<1.6	<2.8	mV	VIO
average temperature coefficient		3	<12	—	<12	μV/°C	DVIO
* input bias current	noninverting	10	<45	<25	<35	μA	IBN
average temperature coefficient		100	<250	—	<100	nA/°C	DIBN
* input bias current	inverting	10	<50	<30	<40	μA	IBI
average temperature coefficient		100	<250	—	<100	nA/°C	DIBI
†power supply rejection ratio		68	>55	>60	>60	dB	PSRR
common mode rejection ratio		65	>55	>60	>60	dB	CMRR
*supply current	no load	17	<23	<23	<23	mA	ICC
MISCELLANEOUS PERFORMANCE							
noninverting input	resistance	150	>50	>85	>85	kΩ	RIN
	capacitance	3.5	<5.5	<5.5	<5.5	pF	CIN
output impedance	at DC	0.1	<0.2	<0.2	<0.2	Ω	RO
common mode input range		3.0	>2.0	>2.5	>2.5	V	CMIR
output voltage range	no load	±3.5V	>±3.0	>±3.2	>±3.2	V	VO
output current		±55	>±25	>±45	>±45	mA	IO

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

V_{cc}	± 7V
I_{out} output is short circuit protected to ground, but maximum reliability will be maintained if I_{out} does not exceed...	60mA
common mode input voltage	± V_{cc}
junction temperature	+ 150°C
operating temperature range	
AJ:	− 40°C to + 85°C
storage temperature range	− 65°C to + 150°C
lead solder duration (+ 300°C)	10 sec
ESD (human body model)	1000V

Miscellaneous Ratings

recommended gain range: ± 1 to ± 8

NOTES:

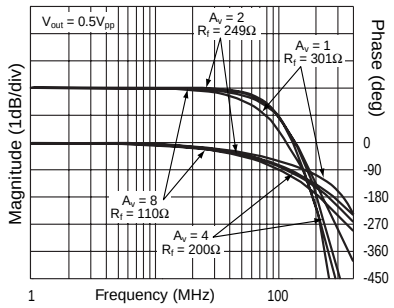
* AJ 100% tested at + 25°C.

note 1: Differential gain and phase measured at A_v = +2V, R = 250Ω.

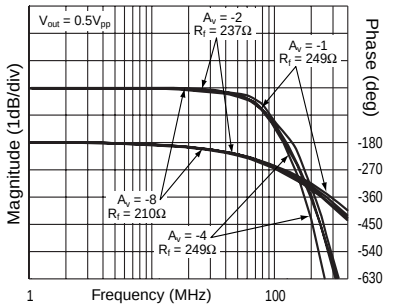
R_L = 150Ω, 1V_{pp} equivalent video signal, 0-100 IRE, 40 IRE_{pp}, 0 IRE = 0 volts, at 75Ω load and 3.58 MHz.

Typical Performance Characteristics (T_A = 25°, A_V = +2, V_{CC} = ±5V, R_L = 100Ω, R_f = 250Ω, V_H = +3V, V_L = -3V)

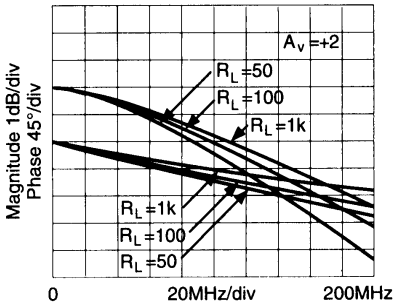
Non-Inverting Frequency Response



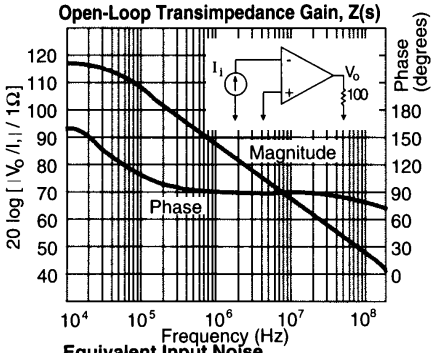
Inverting Frequency Response



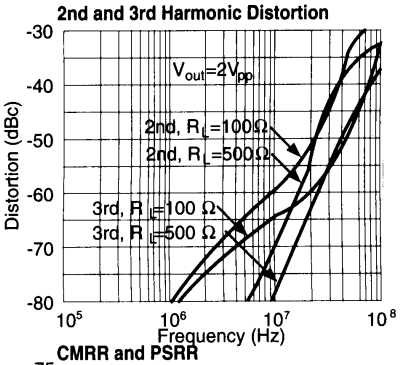
Frequency Response for Various R_Ls



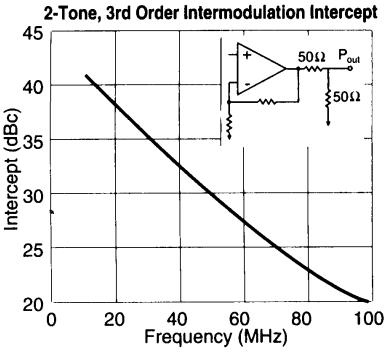
Open-Loop Transimpedance Gain, Z(s)



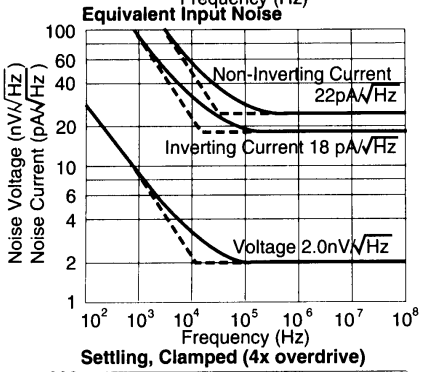
2nd and 3rd Harmonic Distortion



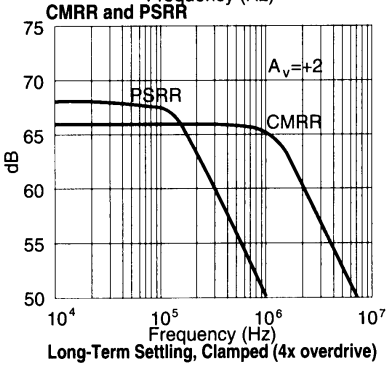
2-Tone, 3rd Order Intermodulation Intercept



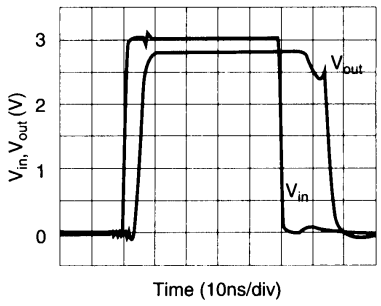
Equivalent Input Noise



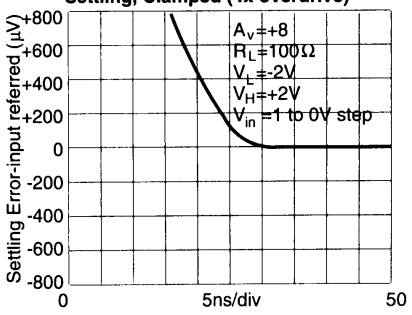
CMRR and PSRR



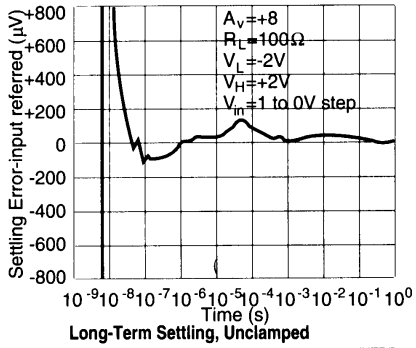
Clamped Pulse Response (8x Overdrive)



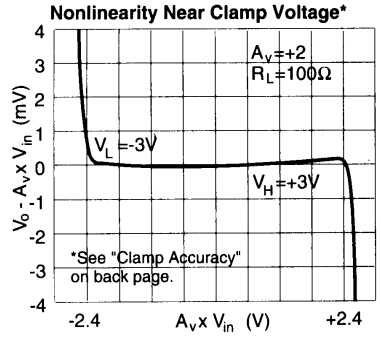
Settling, Clamped (4x overdrive)



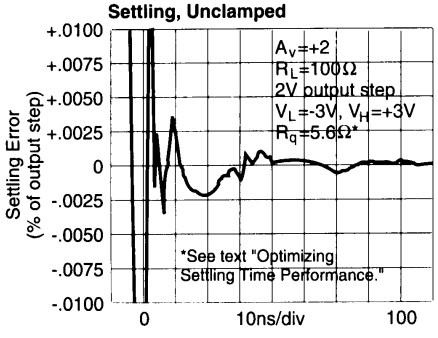
Long-Term Settling, Clamped (4x overdrive)



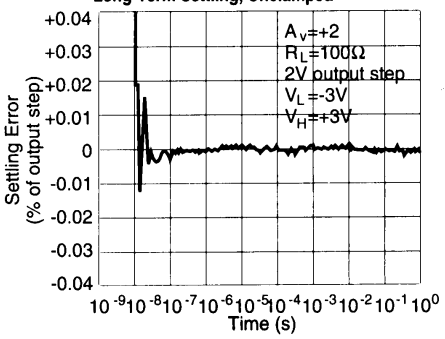
Nonlinearity Near Clamp Voltage*



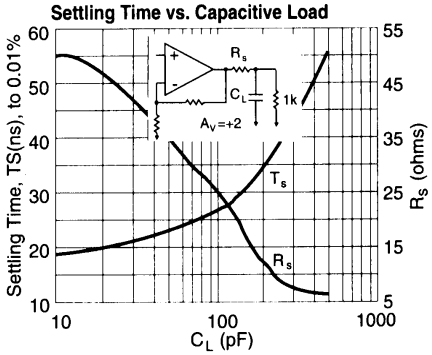
Settling, Unclamped



Long-Term Settling, Unclamped



Settling Time vs. Capacitive Load



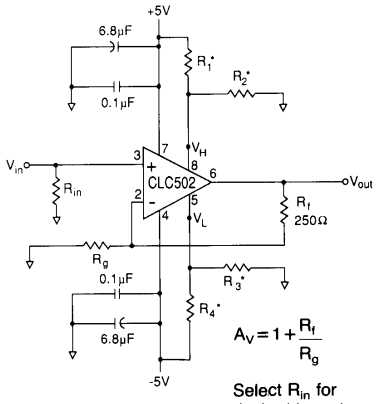


Figure 1:
recommended non-inverting gain circuit

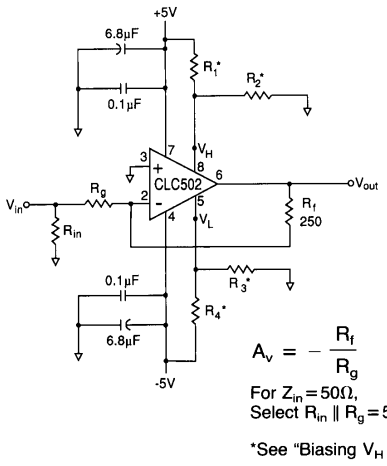


Figure 2:
recommended inverting gain circuit

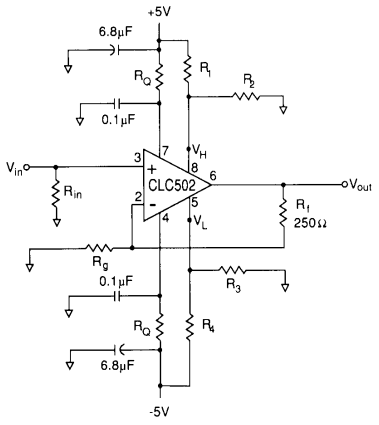


Figure 3:
location of damping resistors (R_Q)

Clamp Operation

The maximum positive or negative excursion of the output voltage is determined by voltages applied to the clamping pins, V_H and V_L. V_H determines the positive clamping level; V_L determines the negative level. For example, if V_H is set at +2V and V_L is set at −0.5V the output voltage is restricted within this −0.5V to +2V range. When the output voltage tries to exceed this level, the amplifier goes into "clamp mode" and the output voltage limits at the clamp voltage.

Clamp Accuracy and Amplifier Linearity

Ideally, the clamped output voltage and the clamp voltage should be identical. In practice, however, there are two sources of clamp inaccuracy: the inherent clamp accuracy (which is shown in the specification page) and resistor divider action of open-loop output resistance of 10Ω and the load resistor. Or, in equation form,

$$V_{out,\ clamp} = (V_{H\ or\ L} \pm 300mV)\frac{R_L}{R_L + 10\Omega.}$$

When setting the clamp voltages, the designer should also recognize that within about 200mV of the clamp voltage, amplifier linearity begins to deteriorate. (See plot on previous page.)

Biasing V_H and V_L

Each of the clamping pins is buffered internally so simple resistive voltage divider circuits work well in providing the clamp voltages. V_L and V_H can be set by choosing the divider resistors using:

$$V_H = (5V)\left(\frac{R_2}{R_1 + R_2}\right) \qquad V_L = (-5V)\left(\frac{R_3}{R_3 + R_4}\right)$$

As a general guideline, let $R_1 + R_2 \cong R_3 + R_4 \cong 5k\Omega$.

V_H should be biased more positively than V_L. V_H may be biased below 0V; however, with this biasing, the output voltage will actually clamp at 0V unless a simple pull down circuit is added to the op amp output (when clamped against V_H, the output cannot sink current). An analogous situation and design solution exists for V_L when it is biased above 0V, but in this case, a pull up circuit is used to *source* current when the amplifier is clamped against V_L.

The clamp voltage range rating is that for normal operation. Problems in overdriven linearity may occur if the clamps are set outside this range so this is not suggested under any conditions. If the clamping capability is not required, the CLC402 (low-gain op amp with fast 14-bit settling) may be the more appropriate part.

The clamps, which have a bandwidth of about 50MHz, may be driven by a high-frequency signal source. This allows the clamping level to be modulated, which is useful in many applications such as pulse amplitude modulation. The source resistance of the signal source should be less than 500Ω to ensure stability.

Clamp-Mode Dynamics

As can be seen in the clamped pulse response plot on the previous page, clamping is virtually instantaneous. Note, however, that there can be a small amount of overshoot, as indicated on the specification page. The output voltage stays at the clamp voltage level as long as the product of the input voltage and the gain setting exceeds the clamp voltage. When the input voltage decreases, it will eventually reach a point where it is no longer trying to drive the output voltage above the clamp voltage. When this occurs, there is typically a 5-10ns "overload recovery from clamp," which is the time it takes for the op amp to resume linear operation. The normal op amp parameters, such as the rise time, apply when the op amp is in linear operation.

Optimizing Settling Time Performance

To obtain the best possible settling time performance for the CLC502, some additional design criteria must be considered, particularly when driving loads of less than 500Ω. When driving a 100Ω load, a step of a few volts on the output will create a large step of current in the power supplies. In some cases, this step will cause a small ringing on the power supply due to the bypass capacitor (.1µF) oscillating with the inductance in the power supply trace. The critical trace is the power supply trace between the two capacitors (a trace inductance of 20nH will be enough to degrade settling time performance). The frequency of the ring can be determined by

$$f = \frac{1}{2\pi\sqrt{C \cdot L_{Trace}}}$$

and any reduction in this frequency will improve performance due to better power supply rejection at lower frequencies. To obtain the best performance, a small resistor, R_Q, may be added in the trace to dampen the circuit (See Figure 3). An R_Q of 5-10Ω will result in excellent settling performance and will have only minor impact on other performance characteristics. No provision for R_Q has been made on the evaluation board available from Comlinear as part #730013. It can, however, be easily added by cutting a trace and adding a 5-10Ω resistor, as shown in Figure 3, for both supplies.

DC Accuracy and Noise

Since the two inputs for the CLC502 are quite dissimilar, the noise and offset error performance differs somewhat from that of a standard differential input amplifier. The two input bias currents are physically unrelated rendering bias current cancellation through matching of the inverting and non-inverting source resistance ineffective.

In Equation 3, the output offset is the algebraic sum of the equivalent input voltage and current sources that influence DC operation. Output noise is determined similarly except that a root-sum-of-squares replaces the algebraic sum. R_s is the non-inverting pin source resistance.

$$\text{Output Offset } V_O = \pm IBN \times R_S(1 + R_f/R_g) \pm VIO\ (1 + R_f/R_g) \pm IBI \times R_f \qquad \text{Eq. (3)}$$

Printed Circuit Layout

As with any high frequency device, a good PCB layout will enhance performance. Ground plane construction and good power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal coupling to the ground plane. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

The device is also very sensitive to parasitic capacitance on the output pin. The plots include a suggested series R_s to de-couple this effect. Evaluation boards (part number 730013 for through-hole and 730027 for SOIC) for the CLC502 are available.

Package Thermal Resistance

Package	θ_{JC}	θ_{JA}
AJP	65°C/W	120°C/W
AJE	60°C/W	140°C/W

Reliability Information

Transistor Count	46

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