June 1999

National Semiconductor

CLC532
High-Speed 2:1 Analog Multiplexer

General Description

The CLC532 is a high-speed 2:1 multiplexer with active input and output stages. The CLC532 also employs a closed-loop design which dramatically improves accuracy. This monolithic device is constructed using an advanced high-performance bipolar process.

The CLC532 has been specifically designed to provide settling times of 17ns to 0.01%. This, coupled with the adjustable noise-bandwidth, makes the CLC532 an ideal choice for infrared and CCD imaging systems. Channel-to-channel isolation is better than 80dB @ 10MHz. Low distortion (80dBc) and spurious signal levels make the CLC532 a very suitable choice for both I/Q processors and receivers.

The CLC532 is offered over both the industrial and military temperature ranges. The Industrial versions, CLC532AJP\AJE\AID, are specified from -40°C to +85°C and are packaged in 14-pin plastic DIP's, 14-pin SOIC's and 14-pin Side-Brazed packages. The extended temperature versions, CLC532A8B/A8D/A8L-2, are specified from -55°C to +125°C and are packaged in a 14-pin hermetic DIP and 20-terminal LCC packages. (Contact factory for LCC and CERDIP availability.)

Ordering Information ...

CLC532AJP	-40ºC to +85ºC	14-pin plastic DIP
CLC532AJE	-40ºC to +85ºC	14-pin plastic SOIC
CLC532ALC	-40ºC to +85ºC	dice
CLC532AMC	-55ºC to +125ºC	dice, MIL-STD-833
CLC532A8B	-55ºC to +125ºC	14-pin CERDIP; MIL-STD-883
CLC532A8L-2A	-55ºC to +125ºC	20-terminal LCC; MIL-STD-883

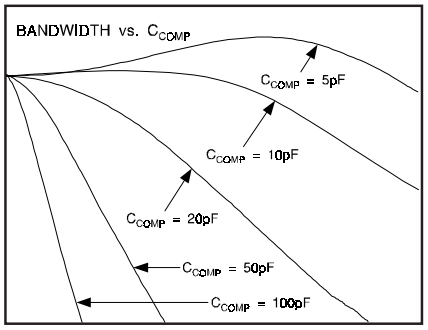
Contact factory for other packages and DESC SMD number.

Features

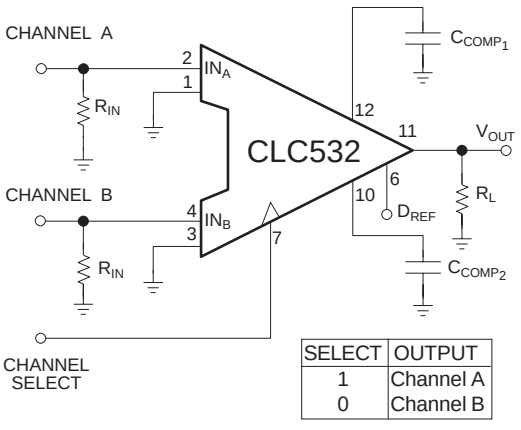
- 12-bit settling (0.01%) - 17ns
- Low noise - 32µVrms
- High isolation - 80dB @ 10MHz
- Low distortion - 80dBc @ 5MHz
- Adjustable bandwidth - 190MHz (max)

Applications

- Infrared system multiplexing
- CCD sensor signals
- Radar I/Q switching
- High definition video HDTV
- Test and calibration

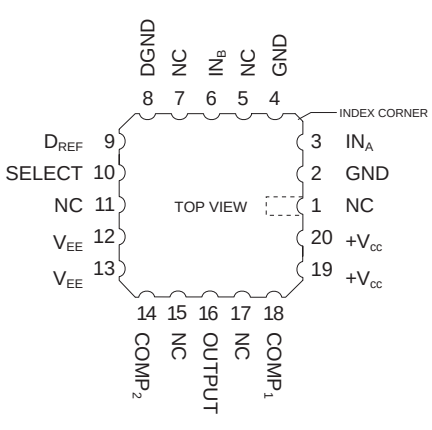


Typical Application

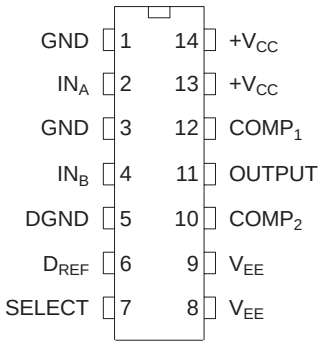


SELECT	OUTPUT
1	Channel A
0	Channel B

20-Terminal LCC



Pinout
DIP & SOIC



Electrical Characteristics ($+V_{CC}$=+5.0V; $-V_{EE}$=-5.2V; R_{IN}=50Ω; R_L=500Ω; C_{COMP}=10pF; ECL Mode, pin 6 = NC)

PARAMETER[1]	CONDITIONS	TYP	MAX/MIN RATINGS[2]			UNITS	SYMBOL
Case Temperature	CLC532AJP/AJE/AIB	+25°C	-40°C	+25°C	+85°C		
FREQUENCY DOMAIN PERFORMANCE							
-3dB bandwidth	V_{OUT}<0.1Vpp	190	140	140	110	MHz	SSBW
-3dB bandwidth	V_{OUT}=2Vpp	45	35	35	30	MHz	LSBW
gain flatness	V_{OUT}<0.1Vpp						
peaking	0.1MHz to 200MHz	0.2	0.7	0.7	0.8	dB	GFP
rolloff	0.1MHz to 100MHz	1.0	1.8	1.8	2.6	dB	GFR
linear phase deviation	dc to 100MHz	2.0				deg	LPD
differential gain	C_{COMP} = 5pF; R_L=150Ω	0.05				%	DG
differential phase	C_{COMP} = 5pF; R_L=150Ω	0.01				deg	DP
crosstalk rejection	2Vpp, 10MHz	80	75	75	74	dB	CT10
	2Vpp, 20MHz	74	69	69	68	dB	CT20
	2Vpp, 30MHz	68	63	63	62	dB	CT30
TIME DOMAIN PERFORMANCE							
rise and fall time	0.5V step	2.7	3.3	3.3	3.8	ns	TRS
	2V step	10	12.5	12.5	14.5	ns	TRL
settling time 2V step; from 50% V_{OUT}	±0.0025%	35				ns	TS14
	±0.01%	17	24	24	27	ns	TSP
	±0.1%	13	18	18	21	ns	TSS
overshoot	2.0V step	2	5	5	6	%	OS
slew rate		160	130	130	110	V/µs	SR
SWITCH PERFORMANCE							
channel to channel switching time	50% SELECT to 10%V_{OUT}	5	7	7	8	ns	SWT10
(2V step at output)	50% SELECT to 90%V_{OUT}	15	20	20	23	ns	SWT90
switching transient		30				mV	ST
DISTORTION AND NOISE PERFORMANCE							
2nd harmonic distortion	2Vpp, 5MHz	80	67	67	67	dBc	HD2
3rd harmonic distortion	2Vpp, 5MHz	86	68	68	68	dBc	HD3
equivalent input noise							
spot noise voltage	>1MHz	3.1				nV/√Hz	SNF
integrated noise	1MHz to 100MHz	32	42	42	46	µVrms	INV
spot noise current		3				pA/√Hz	SNC
STATIC AND DC PERFORMANCE							
* analog output offset voltage		1	6.5	3.5	5.5	mV	VOS
temperature coefficient		15	90		20	µV/°C	DVIO
analog output offset voltage matching		TBD				mV	VOSM
* analog input bias current		50	250	120	120	µA	IBN
temperature coefficient		0.3	2.0		0.8	µA/°C	DIBN
analog input bias current matching		TBD				µA	IBNM
analog input resistance		200	90	120	120	kΩ	RIN
analog input capacitance		2	3.0	2.5	2.5	pF	CIN
* gain accuracy	±2V	0.998	0.988	0.988	0.988	V/V	GA
gain matching	±2V	TBD				V/V	GAM
integral endpoint non-linearity	±1V (full scale)	0.02	0.05	0.03	0.03	%FS	ILIN
output voltage	no load	±3.4	2.4	2.8	2.8	V	VO
output current		45	20	30	30	mA	IO
output resistance	dc	1.5	4.0	2.5	2.5	Ω	RO
DIGITAL INPUT PERFORMANCE							
ECL mode (pin 6 floating)							
input voltage logic HIGH			-1.1	-1.1	-1.1	V	VIH1
input voltage logic LOW			-1.5	-1.5	-1.5	V	VIL1
input current logic HIGH		14	50	30	30	µA	IIH1
input current logic LOW		50	270	110	110	µA	IIL1
TTL mode (pin 6 = +5V)							
input voltage logic HIGH			2.0	2.0	2.0	V	VIH2
input voltage logic LOW			0.8	0.8	0.8	V	VIL2
input current logic HIGH		14	50	30	30	µA	IIH2
input current logic LOW		50	270	110	110	µA	IIL2
POWER REQUIREMENTS							
* supply current ($+V_{CC}$ = +5.0V)	no load	23	30	28	25	mA	ICC
* supply current ($-V_{EE}$ = -5.2V)	no load	24	31	30	26	mA	IEE
nominal power dissipation	no load	240				mW	PD
* power supply rejection ratio		73	60	64	64	dB	PSRR

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Recommended Operating Conditions

positive supply voltage ($+V_{CC}$)	+5V
negative supply voltage ($-V_{EE}$)	-5.2V or -5.0V
differential voltage between any two GND's	10mV
analog input voltage range	±2V
SELECT input voltage range (TTL mode)	0.0V to +3.0V
SELECT input voltage range (ECL mode)	-2.0V to 0.0V
C_{COMP} range[2]	0pF to 100pF

thermal data	θ_{JC}(°C/W)	θ_{JA}(°C/W)
14-pin plastic	55	100
14-pin Cerdip	35	85
14-pin SOIC	35	105
20-terminal LCC	35	50

Absolute Maximum Ratings[3]

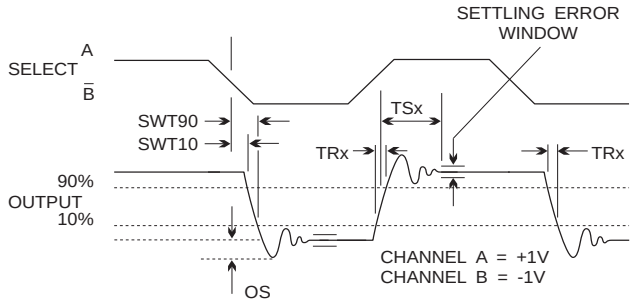
positive supply voltage ($+V_{CC}$)	-0.5V to +7.0V
negative supply voltage ($-V_{EE}$)	+0.5V to -7.0V
differential voltage between any two GND's	200mV
analog input voltage range	$-V_{EE}$ to $+V_{CC}$
digital input voltage range	$-V_{EE}$ to $+V_{CC}$
output short circuit duration (output shorted to GND)	Infinite
junction temperature	+150°C
operating temperature range	
CLC532AJP/AJE/AIB	-40°C to +85°C
storage temperature range	-65°C to +150°C
lead solder duration (+300°C)	10 sec
ESD rating	<500V
transistor count	74

Note 1: Test levels are as follows:
* AJ : 100% tested at +25°C.

Note 2: The CLC532 does not require external C_{COMP} capacitors for proper operation.

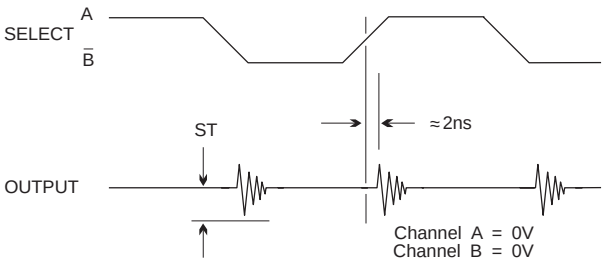
Note 3: Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to maximum ratings for extended periods may affect device reliability.

System Timing Diagram



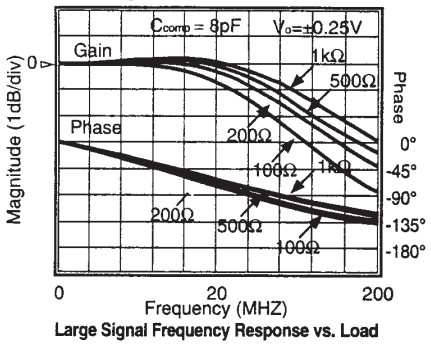
... where TSx is TS14 or TSP or TSS, and TRx is TRS ro TSL.

Switching Transient Timing Diagram

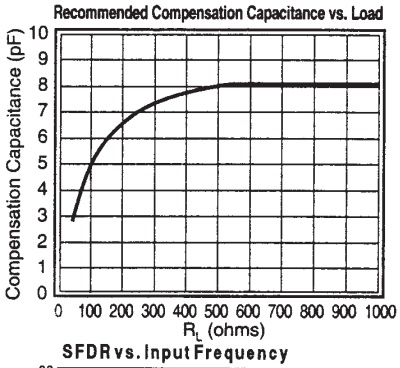


CLC532 Electrical Characteristics (+25°C unless specified)

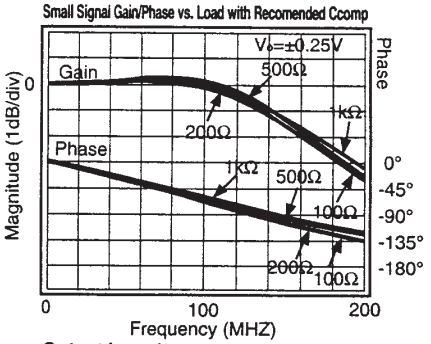
Small Signal Gain/Phase vs. Load



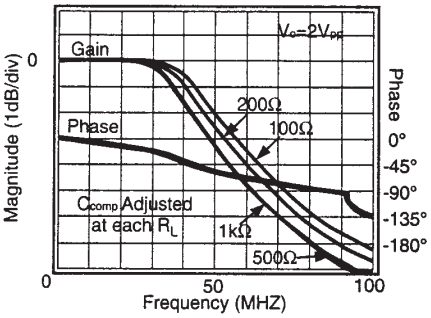
Recommended Compensation Capacitance vs. Load



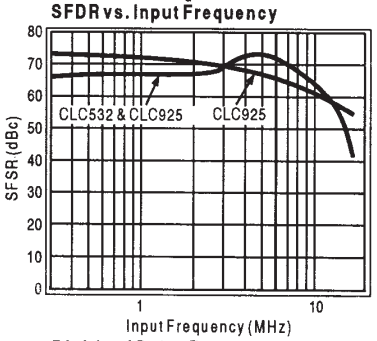
Small Signal Gain/Phase vs. Load with Recomended Ccomp



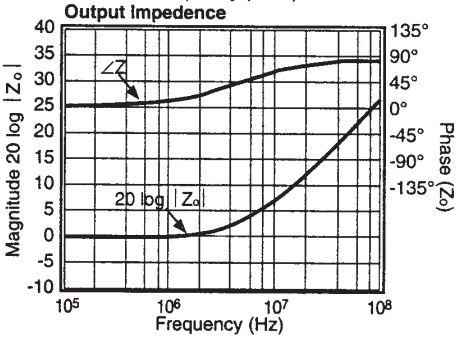
Large Signal Frequency Response vs. Load



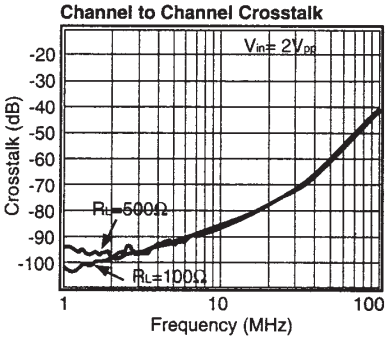
SFDR vs. Input Frequency



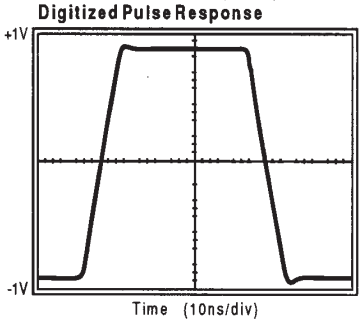
Output Impedence



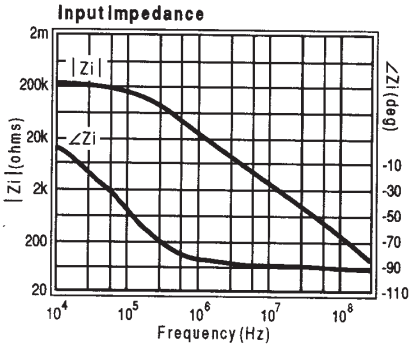
Channel to Channel Crosstalk



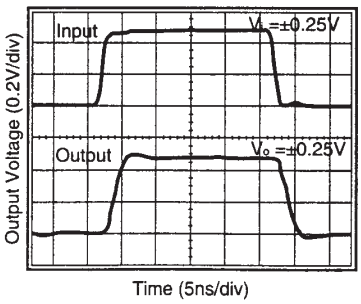
Digitized Pulse Response



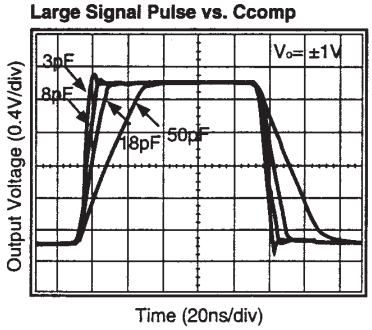
Input Impedance



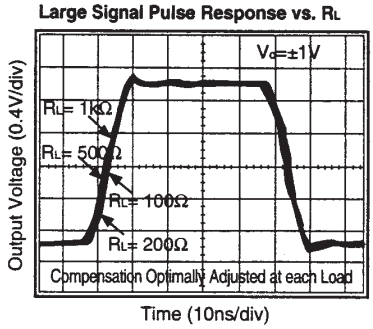
Small Signal Pulse Response



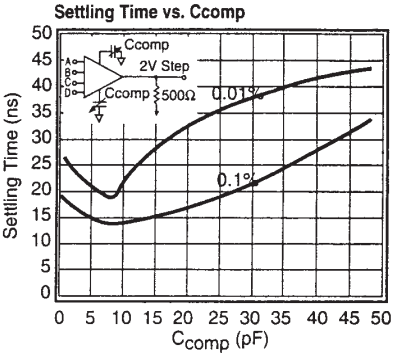
Large Signal Pulse vs. Ccomp



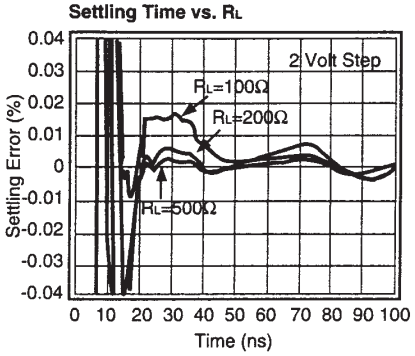
Large Signal Pulse Response vs. RL



Settling Time vs. Ccomp

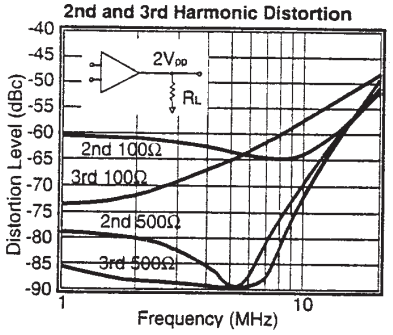


Settling Time vs. RL

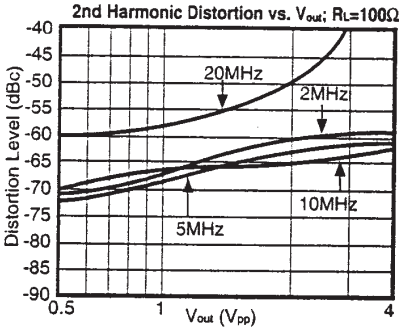


CLC532 Electrical Characteristics (+25°C unless specified)

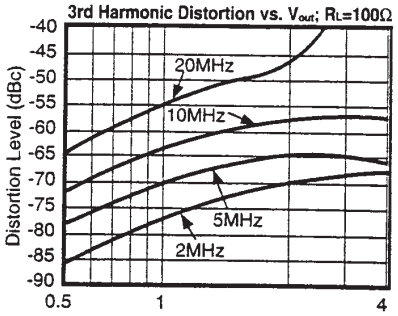
2nd and 3rd Harmonic Distortion



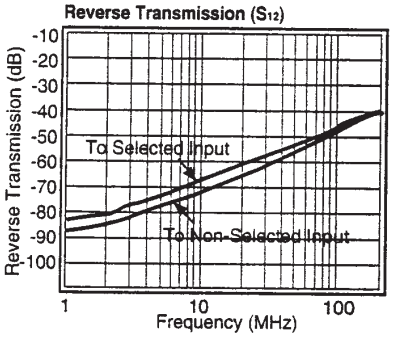
2nd Harmonic Distortion vs. V_{out}; R_L=100Ω



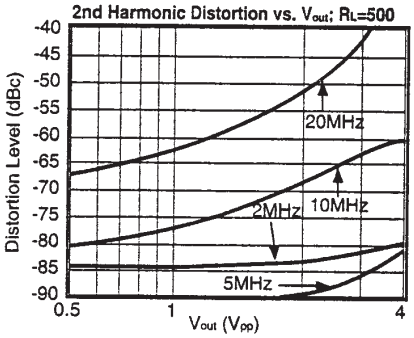
3rd Harmonic Distortion vs. V_{out}; R_L=100Ω



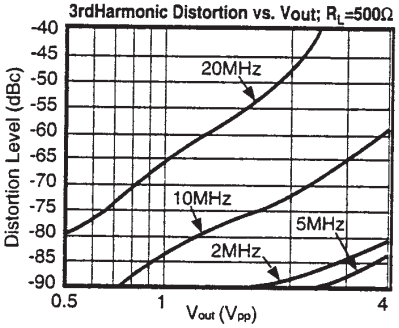
Reverse Transmission (S_{12})



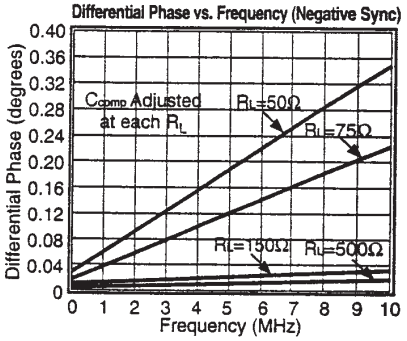
2nd Harmonic Distortion vs. V_{out}; R_L=500



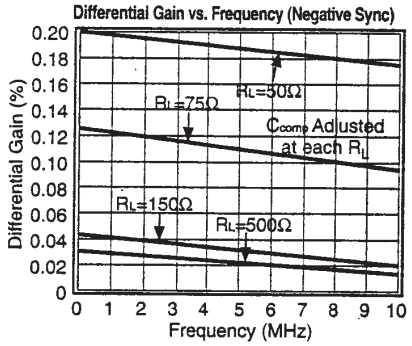
3rdHarmonic Distortion vs. Vout; R_L=500Ω



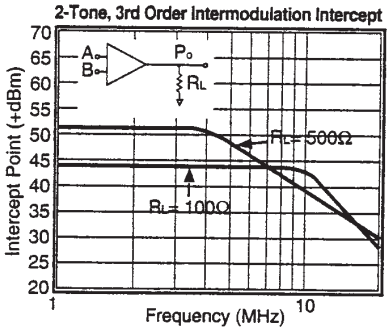
Differential Phase vs. Frequency (Negative Sync)



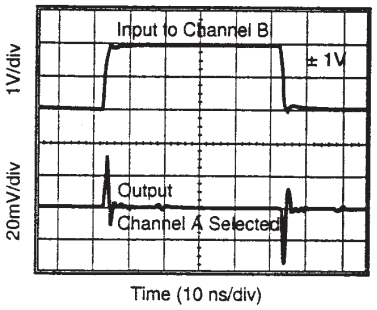
Differential Gain vs. Frequency (Negative Sync)



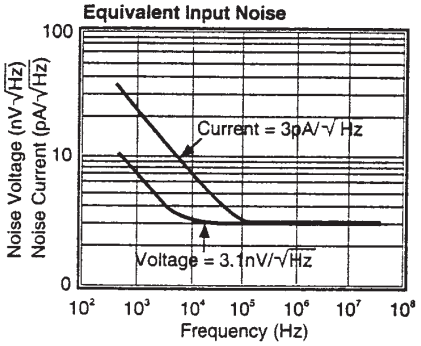
2-Tone, 3rd Order Intermodulation Intercept



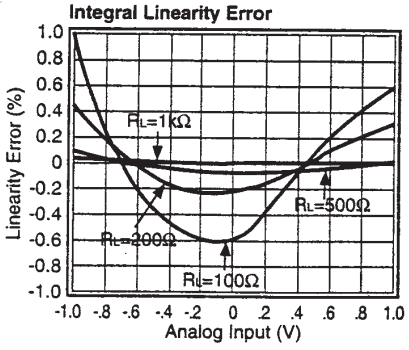
Transient Isolation



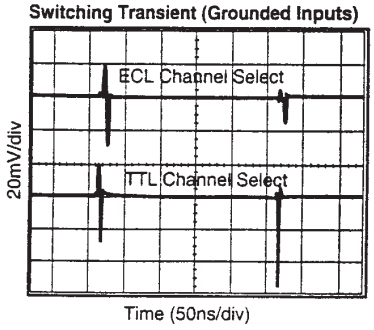
Equivalent Input Noise



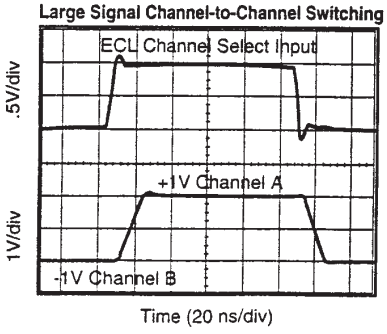
Integral Linearity Error



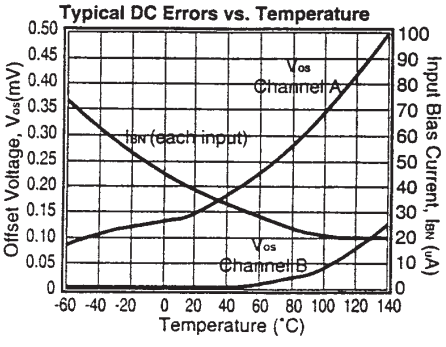
Switching Transient (Grounded Inputs)



Large Signal Channel-to-Channel Switching



Typical DC Errors vs. Temperature



Applications Information

Operation

The CLC532 is a 2:1 analog multiplexer with high-impedance buffered inputs, and a low-impedance, low-distortion, output stage. The CLC532 employs a closed-loop design, which dramatically improves accuracy. The channel SELECT control (Figure 1) determines which of the two inputs (IN_A or IN_B) is present at the OUTPUT. Beyond the basic multiplexer function, the CLC532 offers compatibility with either TTL or ECL logic families, as well as adjustable bandwidth.

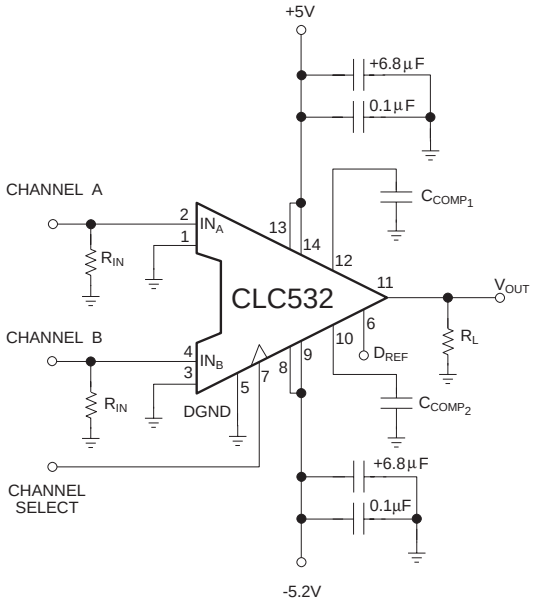


Figure 1: Standard CLC532 Circuit Configuration

Digital Interface and Channel SELECT

The CLC532 functions with ECL, TTL and CMOS logic families. D_{REF} controls logic compatibility. In normal operation, D_{REF} is left floating, and the channel SELECT responds to ECL level signals, Figure 2. For TTL or CMOS level SELECT inputs (Figure 3), D_{REF} should be tied to +5V (the CLC532 incorporates an internal 2300Ω series isolation resistor for the D_{REF} input). For TTL or CMOS operation, the channel SELECT requires a resistor input network to prevent saturation of the channel select circuitry. Without this input network, channel SELECT logic levels above 3V will cause internal junction saturation and slow switching speeds.

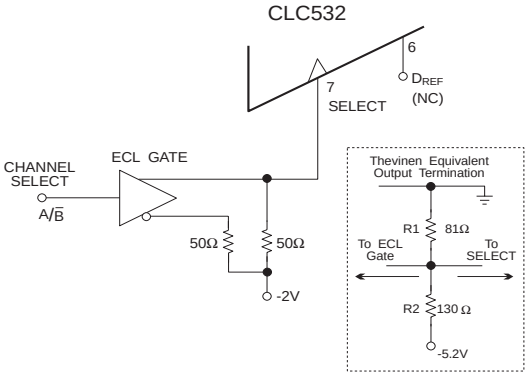


Figure 2: ECL Level Channel SELECT Configuration

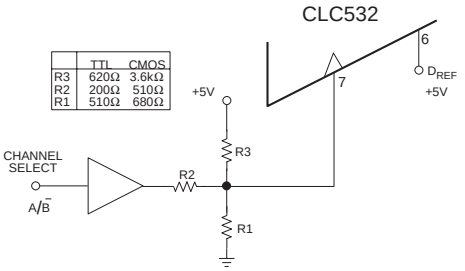


Figure 3: TTL/CMOS Level Channel SELECT Configuration

Compensation

The CLC532 incorporates compensation nodes that allow both its bandwidth and its settling time/slew rate to be adjusted. Bandwidth and settling time/slew adjustments are linked, meaning that lowering the bandwidth also lowers slew rate and lengthens settling time. Proper adjustment (compensation) is necessary to optimize system performance. Time Domain applications should generally be optimized for lowest RMS noise at the CLC532 output, while maintaining settling time and slew rates at adequate levels to meet system needs. Frequency Domain applications should generally be optimized for maximally flat frequency response.

Figure 4 below describes the basic relationship between bandwidth and R_S for various values of load capacitance, C_L, where C_{COMP} = 10pF.

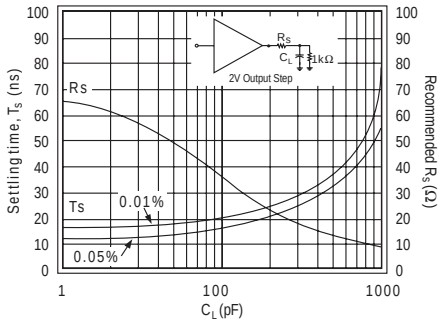


Figure 4: Settling Time and R_S vs. C_L

Figure 5 shows the resulting changes in bandwidth and slew rate for increasing values of C_{COMP} . The RMS noise at the CLC532 output can be approximated as:

$$OUTPUT_{NOISE_{RMS}} = (n_V)(\sqrt{1.57*BW_{-3dB}})$$

where... n_V = input spot noise voltage;
BW_{-3dB} = Bandwidth is from figure 5.

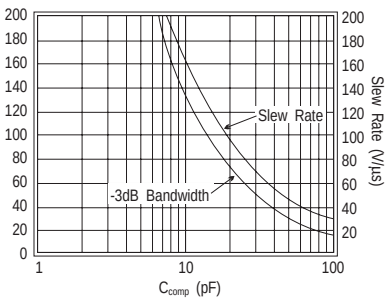


Figure 5: C_{COMP} for Maximally Flat Frequency Response

Power Supplies and Grounding

Proper power supply bypassing and grounding is essential to the CLC532's operation. A 0.1µF to 0.01mF ceramic chip capacitor should be located as close as possible to the individual power supply pins. Larger +6.8µF tantalum capacitors should be used within a few inches of the CLC532. The ground connections for these larger by-pass capacitors should be very symmetrically located relative the CLC532 output load ground connection. Harmonic distortion can be heavily influenced by non-symmetric decoupling capacitor grounding. The smaller chip capacitors located directly at the power supply pins are not particularly susceptible to this effect.

Separation of analog and digital ground planes is not recommended. In most cases, a single low-impedance ground plane will provide the best performance. In those special cases requiring separate ground planes, the following table indicates the signal and supply ground connections.

Pin	Functions	Ground Return
1,3	Shield /Supply Returns	Supplies and Inputs
5	D_{REF} Ground	D_{REF} Currents Only

Input Shielding

The CLC532 has been designed for use in high-speed wide-dynamic range systems. Guard-ring traces and the use of the ground pins separating the analog inputs are recommended to maintain high isolation (Figure 6). Likely sources of noise and interference that may couple onto the inputs, are the logic signals and power supplies to the CLC532. Other types of clock and signal traces should not be overlooked, however.

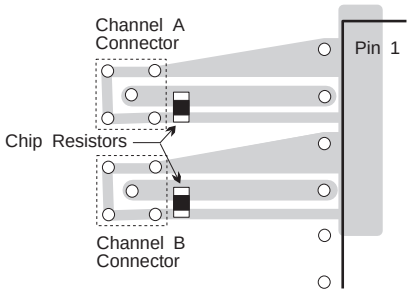


Figure 6: Alternate Layout Using Guard Ring

The general rule in maintaining isolation has two facets, minimize the primary return ground current path impedances back to the respective signal sources, while maximizing the impedance associated with common or secondary ground current return paths. Success or failure to optimize input signal isolation can be measured directly as the isolation between the input channels with the CLC532 removed from circuit. The channel-to-channel isolation of the CLC532 can never be better than the isolation level present at its inputs.

Special attention must be paid to input termination resistors. Minimizing the return current path that is common to both of the input termination resistors is essential. In the event that a ground return current from one input termination resistor is able to find a secondary path back to its signal source (which also happens to be common with either the primary or secondary return path for the second input termination resistor), a small voltage can appear across the second input termination resistor. The small voltage seen across the second input termination resistor will be highly correlated with the signal generating the initial return currents. This situation will severely degrade channel-to-channel isolation at the input of the CLC532, even if the CLC532 were removed from circuit. Poor isolation at the input will be transmitted directly to the output.

Use of "small" value input termination resistors will also improve channel-to-channel isolation. However, extremely low values (<25Ω) tend to stress the driving source's ability to provide a high-quality input signal to the CLC532. Higher values tend to aggravate any layout dependent crosstalk. 75Ω to 50Ω is a reasonable target, but the lower the better.

Combining Two Signals in ADC Applications

The CLC532 is applicable in a wide range of circuits and applications. A classic example of this flexibility is combining two or more signals for digitization by an analog-to-digital converter (ADC). A clear understanding of both the multiplexer and the ADC's operation is needed to optimize this configuration.

To obtain the best performance from the combination, the output of the CLC532 must be an accurate representation of the selected input during the ADC conversion cycle. The time at which the ADC samples the input varies with the type of ADC that is being used.

Subranging ADCs usually have a Track-and-Hold (T/H) at their input. For a successful combination of the multiplexer and the ADC, the multiplexer timing and the T/H timing must be compatible. When the ADC is given a convert command, the T/H transitions from Track mode to Hold mode. The delay between the convert command and this transition is usually specified as Aperture Delay or as Sampling Time Offset.

To maximize the time that the multiplexer output has to settle, and that the T/H has to acquire the signal, the multiplexer should begin its transition from one input to the other immediately after the T/H transition into HOLD mode. Unfortunately it is during the initial portion of the HOLD period that a subranging ADC performs analog processing of the sampled signal. High slew rate transitions on the input during this time may have a detrimental effect on the conversion accuracy.

To minimize the effects of high input slew rates, two strategies that can employed. Strategy one applies when the sample rate of the system is below the rated speed of the ADC. Here the CLC532 SELECT timing is delayed until after the multiplexer transition takes place, and after the A/D has completed one conversion cycle and is waiting for the next convert command. As an example, if a CLC935 (15MSPS) ADC is being used at 10MSPS, the conversion takes place in the first 67ns after the CONVERT command. The next 33ns are spent waiting for the next CONVERT command, and would be an ideal place to switch the multiplexer from one channel to the next.

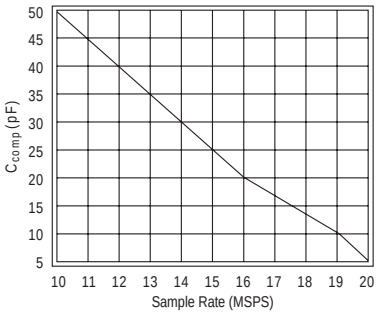


Figure 7: Recommended C_{COMP} vs. ADC Sample Rate

The second optimization strategy involves lowering the slew rate at the input of the ADC so that fewer high frequency components are available to feed through to the hold capacitor during HOLD

mode. The CLC532 output signal can be slew limited by using its compensation capacitors. This approach also has the advantage of limiting the excess noise passed through the CLC532 and on to the ADC. Figure 7 shows the recommended C_{COMP} values as a function of ADC Sample rate. Since the optimal values will change from one ADC to the next, this graph should be used as a starting point for C_{COMP} selection. Both C_{COMP} capacitors should be the same value to maintain output symmetry.

Flash ADCs are similar to subranging ADCs in that the sampling period is very brief. The primary difference is that the acquisition time of a flash converter is much shorter than that of a subranging ADC. With a flash ADC, the transition of the CLC532 output should be after the sampling instant ("Aperture Delay" after the CONVERT command). It is only during this period that a flash converter is susceptible to interference from a rapidly changing analog input signal.

Gain Selection for an ADC

In many applications, such as RADAR, the dynamic range requirements may exceed the accuracy requirements. Since wide dynamic range ADCs are also typically highly accurate ADCs, this often leads the designer into selecting an ADC which is a technical overkill and a budget buster. By using the CLC532 as a selectable-gain stage, a less expensive ADC can be used. As an example, if an application calls for 80dB of dynamic Range and 0.05% accuracy, rather than using a 14-bit converter, a 12-bit converter combined with the circuit in figure 8 will meet the same objective. The CLC532 is used to select between the analog input signal and a version of the input signal attenuated by 12dB. This circuit affords 14-bit dynamic range, 12-bit accuracy and 12-bit ease of implementation.

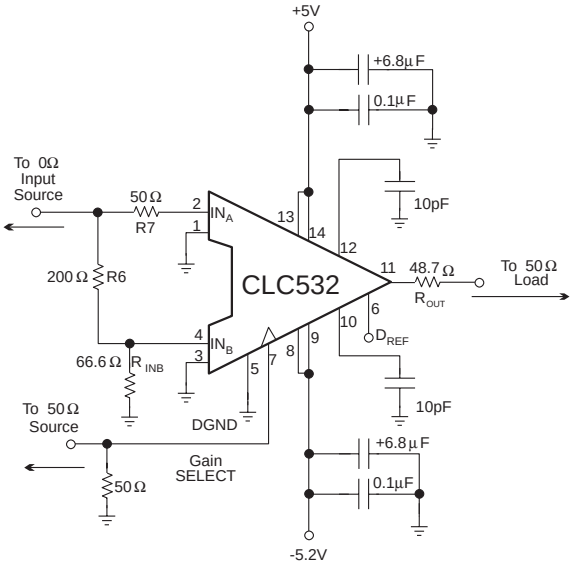


Figure 8: Selectable Gain Stage Improves ADC Dynamic Range

Full Wave Rectifier Circuit

The use of a diode rectifier provides significant distortion for signals that are small compared to the forward bias voltage. Accordingly, when low distortion performance is needed, standard diode based circuits do not work well. The CLC532 can be configured to provide a very low distortion full wave rectifier. The circuit in figure 9 is used to select between an analog input signal and an inverted version of the input signal. The resulting output exhibits very little distortion for small scale signals up to several hundred kilohertz.

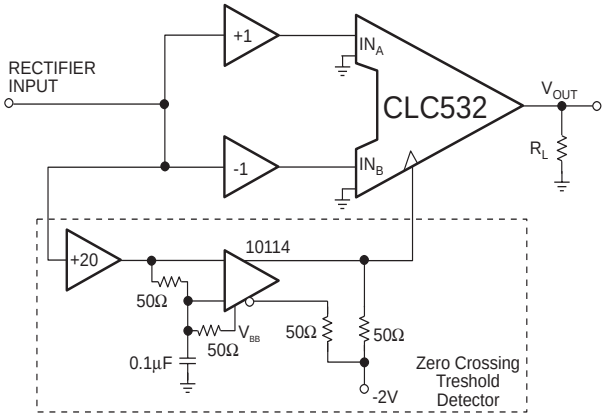


Figure 9: Low Distortion Full Wave Rectifier

Use of the CLC532 as a Mixer.

A double balanced mixer, such as is shown in figure 10, operates by multiplying the RF input by the LO input. This is done by using the LO to select one of two paths through a diode bridge depending upon the LO sign. The result is an output where IF=RF when LO>0 and IF=-RF if LO<0. This same result can be obtained with the circuit shown in figure 11. The CLC532 based circuit uses a digital LO making system design easier in those cases where the LO is digitally derived. One advantage of the CLC532 based approach is excellent isolation between all three ports. Also see the *RF design awards* article by Thomas Hack in the January 1993 issue of *RF Design*.

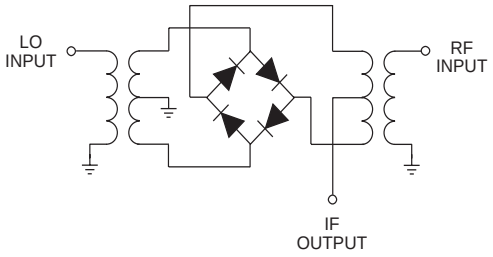


Figure 10: Typical Double-Balanced Mixer

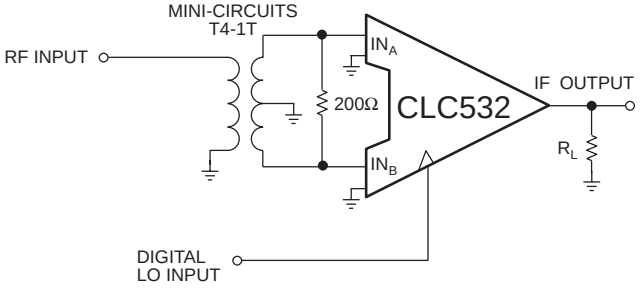


Figure 11: High-Isolation Mixer Implementation

Evaluation Board

An evaluation board (part number CLC730028) for the CLC532 is available. This board can be used for fast, trouble-free, evaluation and characterization of the CLC532. Additionally, this board serves as a template for layout and fabrication information. The CLC532 evaluation board data sheet is available.

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