

CLC5623

Triple, High Output, Video Amplifier

General Description

The CLC5623 has a new output stage that delivers high output drive current (130mA), but consumes minimal quiescent supply current (3.0mA/ch) from a single 5V supply. Its current feedback architecture, fabricated in an advanced complementary bipolar process, maintains consistent performance over a wide range of gains and signal levels, and has a linear-phase response up to one half of the -3dB frequency.

The CLC5623 offers 0.1dB gain flatness to 15MHz and differential gain and phase errors of 0.06% and 0.06°. These features are ideal for professional and consumer video applications.

The CLC5623 offers superior dynamic performance with a 148MHz small-signal bandwidth, 370V/ μ s slew rate and 4.4ns rise/fall times ($2V_{step}$). The combination of low quiescent power, high output current drive, and high-speed performance make the CLC5623 well suited for many battery-powered personal communication/computing systems.

The ability to drive low-impedance, highly capacitive loads, with minimum distortion, makes the CLC5623 ideal for cable applications. The CLC5623 will drive a 100 Ω load with only -78/-94dBc second/third harmonic distortion ($A_v = +2$, $V_{out} = 2V_{pp}$, $f = 1\text{MHz}$). With a 25 Ω load, and the same conditions, it produces only -82/-96dBc second/third harmonic distortion.

The CLC5623 can also be used for driving differential-input step-up transformers for applications such as Asynchronous Digital Subscriber Lines (ADSL) or High-Bit-Rate Digital Subscriber Lines (HDSL).

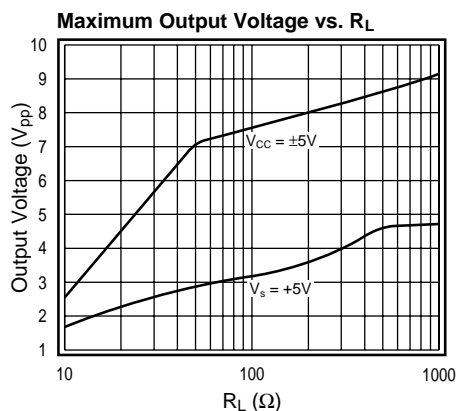
When driving the input of high-resolution A/D converters, the CLC5623 provides excellent -86/-96dBc second/third harmonic distortion ($A_v = +2$, $V_{out} = 2V_{pp}$, $f = 1\text{MHz}$, $R_L = 1\text{k}\Omega$) and fast settling time.

Features

- 130mA output current
- 0.06%, 0.06° differential gain, phase
- 3.0mA/ch supply current
- 148MHz bandwidth ($A_v = +2$)
- -86/-96dBc HD2/HD3 (1MHz)
- 18ns settling to 0.05%
- 370V/ μ s slew rate
- Stable for capacitive loads up to 1000pf
- Single 5V or $\pm 5\text{V}$ supplies

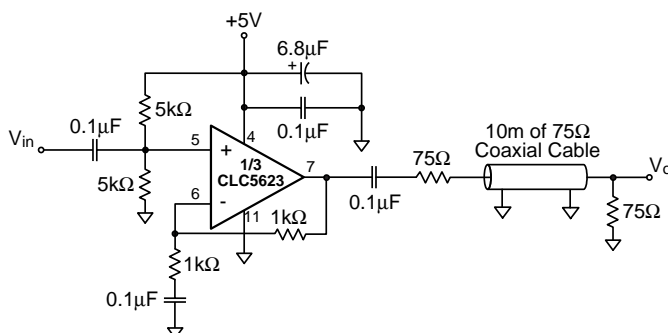
Applications

- Video line driver
- ADSL/HDSL driver
- Coaxial cable driver
- UTP differential line driver
- Transformer/coil driver
- High capacitive load driver
- Portable/battery-powered applications
- Differential A/D driver



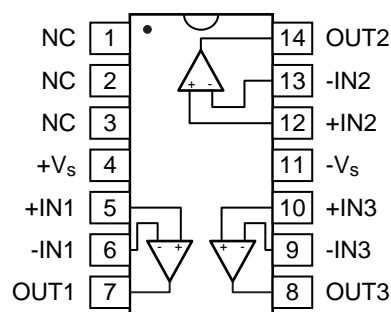
Typical Application

Single Supply Cable Driver



Pinout

DIP & SOIC



+5V Characteristics ($A_v = +2$, $R_f = 750\Omega$, $R_i = 1k\Omega$ (PDIP), $R_i = 750\Omega$ (SOIC), $V_s = +5V^1$, $V_{cm} = V_{EE} + (V_s/2)$, R_L tied to V_{cm} , unless specified)

PARAMETERS	CONDITIONS	TYP	MIN/MAX RATINGS				UNITS	NOTES
Ambient Temperature	CLC5623IN	+25°C	+25°C	0 to 70°C	-40 to 85°C			
FREQUENCY DOMAIN RESPONSE								
-3dB bandwidth	$V_o = 1.5V_{pp}$	107	85	75	75		MHz	
-0.1dB bandwidth	$V_o = 0.5V_{pp}$	14	13	10	10		MHz	
gain peaking	<200MHz, $V_o = 0.5V_{pp}$	0	0.5	0.9	0.9		dB	
gain rolloff	<30MHz, $V_o = 0.5V_{pp}$	0.3	0.7	0.8	0.8		dB	
linear phase deviation	<30MHz, $V_o = 0.5V_{pp}$	1.0	2.0	2.4	2.4		deg	
differential gain	NTSC, $R_L = 150\Omega$ to -1V	0.03	—	—	—		%	
differential phase	NTSC, $R_L = 150\Omega$ to -1V	0.08	—	—	—		deg	
TIME DOMAIN RESPONSE								
rise and fall time	2V step	4.5	6.0	6.4	6.8		ns	
settling time to 0.05%	1V step	17	25	40	60		ns	
overshoot	2V step	11	15	18	18		%	
slew rate	2V step	280	195	165	150		V/ μ s	
DISTORTION AND NOISE RESPONSE								
2 nd harmonic distortion	$2V_{pp}$, 1MHz	-76	—	—	—		dBc	
	$2V_{pp}$, 1MHz; $R_L = 1k\Omega$	-85	—	—	—		dBc	
	$2V_{pp}$, 5MHz	-63	-58	-56	-56		dBc	
	$2V_{pp}$, 1MHz	-88	—	—	—		dBc	
	$2V_{pp}$, 1MHz; $R_L = 1k\Omega$	-96	—	—	—		dBc	
3 rd harmonic distortion	$2V_{pp}$, 5MHz	-65	-62	-60	-60		dBc	
equivalent input noise								
voltage (e_{ni})	>1MHz	4.9	5.9	6.4	6.4		nV/ \sqrt{Hz}	
non-inverting current (i_{bn})	>1MHz	6.6	8.5	9.3	9.3		pA/ \sqrt{Hz}	
inverting current (i_{bi})	>1MHz	11.1	14.7	15.8	15.8		pA/ \sqrt{Hz}	
crosstalk (input referred)	10MHz, $1V_{pp}$	-51	—	—	—		dB	
crosstalk, all hostile (input referred)	10MHz, $1V_{pp}$	-49	—	—	—		dB	
STATIC DC PERFORMANCE								
input offset voltage		1	4	6	6		mV	A
average drift		8	—	—	—		μ V/ $^{\circ}$ C	
input bias current (non-inverting)		6	18	22	24		μ A	A
average drift		40	—	—	—		nA/ $^{\circ}$ C	
input bias current (inverting)		6	14	16	17		μ A	A
average drift		25	—	—	—		nA/ $^{\circ}$ C	
power supply rejection ratio	DC	48	45	43	43		dB	
common-mode rejection ratio	DC	45	43	41	41		dB	
supply current per channel	$R_L = \infty$	3.0	3.4	3.6	3.6		mA	A
MISCELLANEOUS PERFORMANCE								
input resistance (non-inverting)		0.86	0.50	0.45	0.45		M Ω	
input capacitance (non-inverting)		1.8	2.75	2.75	2.75		pF	
input voltage range, High		4.2	4.1	4.1	4.0		V	
input voltage range, Low		0.8	0.9	0.9	1.0		V	
output voltage range, High	$R_L = 100\Omega$	4.0	3.9	3.9	3.8		V	
output voltage range, Low	$R_L = 100\Omega$	1.0	1.1	1.1	1.2		V	
output voltage range, High	$R_L = \infty$	4.1	4.0	4.0	3.9		V	
output voltage range, Low	$R_L = \infty$	0.9	1.0	1.0	1.1		V	
output current		100	80	65	40		mA	B
output resistance, closed loop	DC	70	105	105	140		m Ω	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Notes

- A) J-level: spec is 100% tested at +25°C.
 B) The short circuit current can exceed the maximum safe output current.
 1) $V_s = V_{CC} - V_{EE}$

Absolute Maximum Ratings

supply voltage ($V_{CC} - V_{EE}$)	+14V
output current (see note C)	140mA
common-mode input voltage	V_{EE} to V_{CC}
maximum junction temperature	+150°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C

Reliability Information

Transistor Count

147

±5V Characteristics (A_v = +2, R_f = 1kΩ (PDIP), R_f = 750Ω (SOIC), R_L = 100Ω, V_{CC} = ±5V, unless specified)

PARAMETERS	CONDITIONS	TYP	GUARANTEED MIN/MAX			UNITS	NOTES
Ambient Temperature	CLC5623IN	+25°C	+25°C	0 to 70°C	-40 to 85°C		
FREQUENCY DOMAIN RESPONSE							
-3dB bandwidth	V _o = 1.5V _{pp}	148	110	105	85	MHz	
	V _o = 4.0V _{pp}	72	55	52	52	MHz	
-0.1dB bandwidth	V _o = 1.0V _{pp}	15	12	9	9	MHz	
gain peaking	<200MHz, V _o = 1.0V _{pp}	0	0.5	0.9	1.3	dB	
gain rolloff	<30MHz, V _o = 1.0V _{pp}	0.1	0.3	0.5	0.5	dB	
linear phase deviation	<30MHz, V _o = 1.0V _{pp}	0.08	1.6	2.0	2.0	deg	
differential gain	NTSC, R _L =150Ω	0.06	0.12	—	—	%	
differential phase	NTSC, R _L =150Ω	0.06	0.1	—	—	deg	
TIME DOMAIN RESPONSE							
rise and fall time	2V step	4.4	5.8	6.2	6.8	ns	
settling time to 0.05%	2V step	18	25	40	60	ns	
overshoot	2V step	19	21	23	24	%	
slew rate	2V step	370	280	260	240	V/μs	
DISTORTION AND NOISE RESPONSE							
2 nd harmonic distortion	2V _{pp} , 1MHz	-78	—	—	—	dBc	
	2V _{pp} , 1MHz; R _L = 1kΩ	-86	—	—	—	dBc	
	2V _{pp} , 5MHz	-65	-60	-58	-58	dBc	
3 rd harmonic distortion	2V _{pp} , 1MHz	-94	—	—	—	dBc	
	2V _{pp} , 1MHz; R _L = 1kΩ	-96	—	—	—	dBc	
	2V _{pp} , 5MHz	-73	-60	-58	-58	dBc	
equivalent input noise							
voltage (e _{ni})	>1MHz	4.9	5.9	6.4	6.4	nV/√Hz	
non-inverting current (i _{bn})	>1MHz	6.6	8.5	9.3	9.3	pA/√Hz	
inverting current (i _{bi})	>1MHz	11.1	14.7	15.8	15.8	pA/√Hz	
crosstalk (input referred)	10MHz, 1V _{pp}	-51	—	—	—	dB	
crosstalk, all hostile (input referred)	10MHz, 1V _{pp}	-49	—	—	—	dB	
STATIC DC PERFORMANCE							
input offset voltage		1	6	7	8	mV	
average drift		10	—	—	—	μV/°C	
input bias current (non-inverting)		8	18	23	25	μA	
average drift		40	—	—	—	nA/°C	
input bias current (inverting)		9	24	28	28	μA	
average drift		30	—	—	—	nA/°C	
power supply rejection ratio	DC	48	45	43	43	dB	
common-mode rejection ratio	DC	47	43	41	41	dB	
supply current (per channel)	R _L = ∞	3.2	3.8	4.0	4.0	mA	
MISCELLANEOUS PERFORMANCE							
input resistance (non-inverting)		0.88	0.52	0.47	0.47	MΩ	
input capacitance (non-inverting)		1.45	2.15	2.15	2.15	pF	
common-mode input range		±4.2	±4.1	±4.1	±4.0	V	
output voltage range	R _L = 100Ω	±3.8	±3.6	±3.6	±3.5	V	
output voltage range	R _L = ∞	±4.0	±3.8	±3.8	±3.7	V	
output current		130	100	80	50	mA	B
output resistance, closed loop	DC	60	90	90	120	mΩ	

Notes

B) The short circuit current can exceed the maximum safe output current.

Package Thermal Resistance

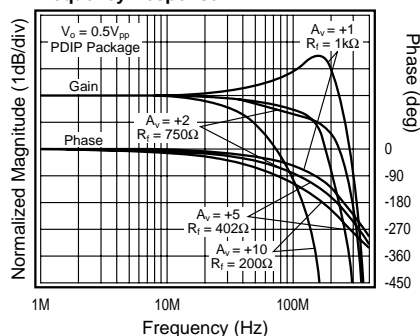
Package	θ _{JC}	θ _{JA}
Plastic (IN)	60°C/W	110°C/W
Surface Mount (IM)	55°C/W	125°C/W

Ordering Information

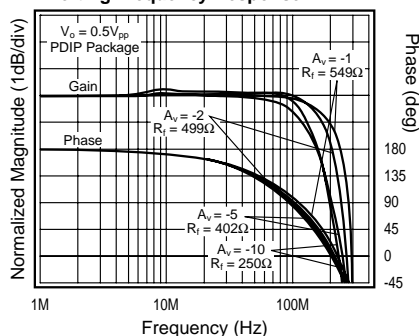
Model	Temperature Range	Description
CLC5623IN	-40°C to +85°C	8-pin PDIP
CLC5623IM	-40°C to +85°C	8-pin SOIC
CLC5623IMX	-40°C to +85°C	8-pin SOIC tape and reel

+5V Typ. Perform. ($A_v = +2$, $R_f = 1\text{k}\Omega$ (PDIP), $R_f = 750\Omega$ (SOIC), $R_L = 100\Omega$, $V_s = +5\text{V}^1$, $V_{cm} = V_{EE} + (V_s/2)$, R_L tied to V_{cm} , unless specified)

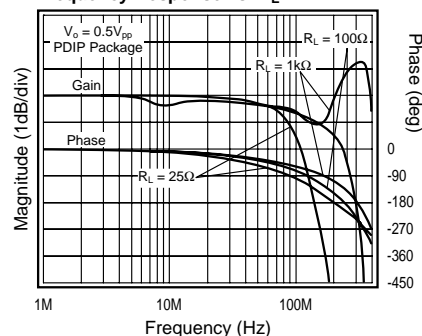
Frequency Response



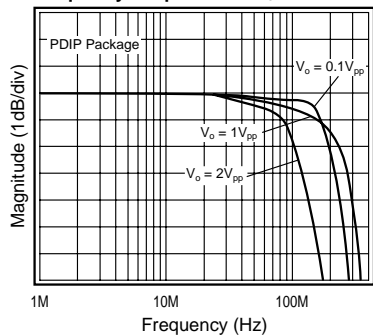
Inverting Frequency Response



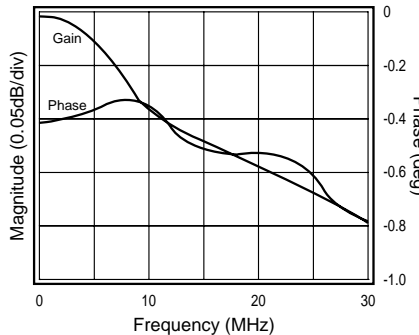
Frequency Response vs. R_L



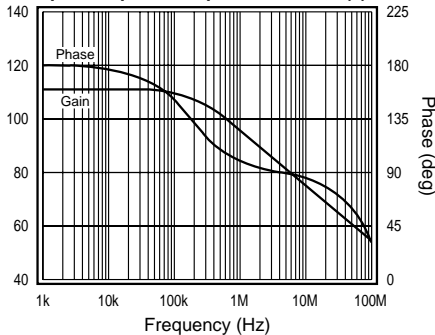
Frequency Response vs. V_o



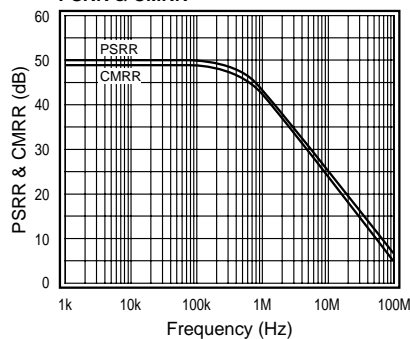
Gain Flatness & Linear Phase



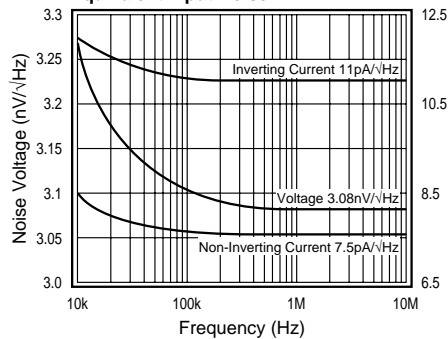
Open Loop Transimpedance Gain, $Z(s)$



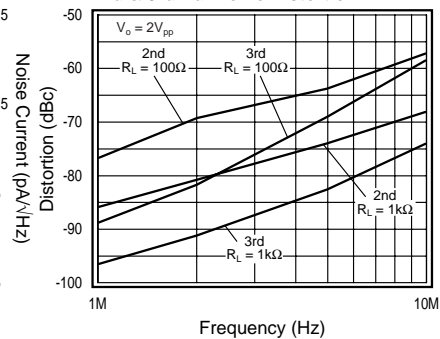
PSRR & CMRR



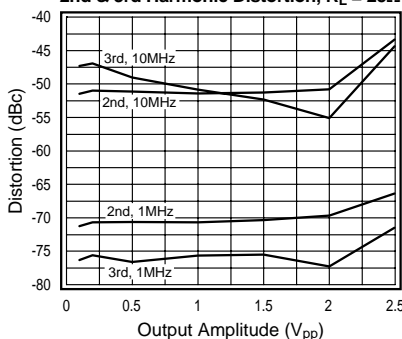
Equivalent Input Noise



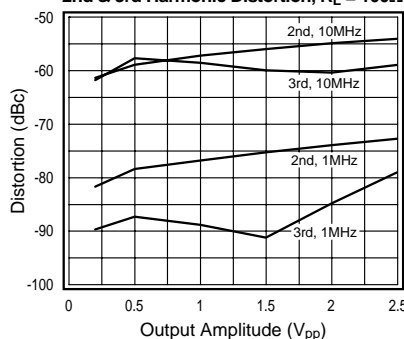
2nd & 3rd Harmonic Distortion



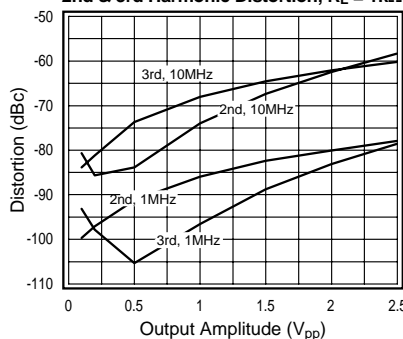
2nd & 3rd Harmonic Distortion, $R_L = 25\Omega$



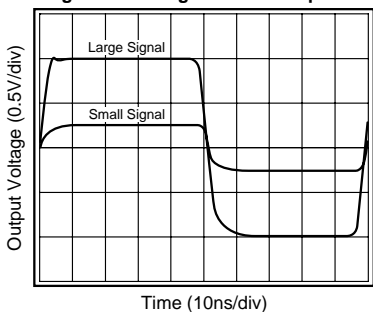
2nd & 3rd Harmonic Distortion, $R_L = 100\Omega$



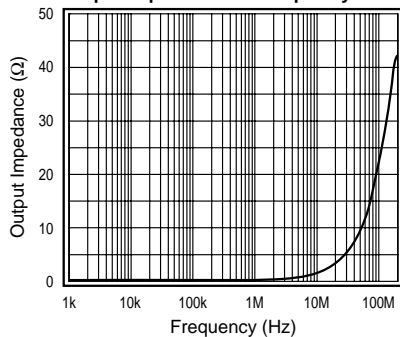
2nd & 3rd Harmonic Distortion, $R_L = 1\text{k}\Omega$



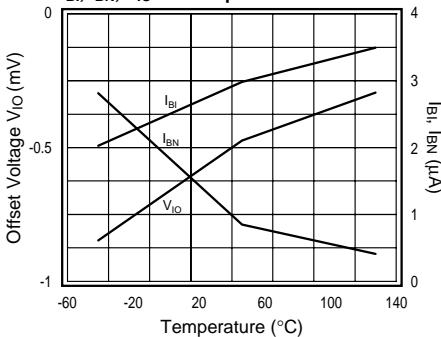
Large & Small Signal Pulse Response



Output Impedance vs. Frequency

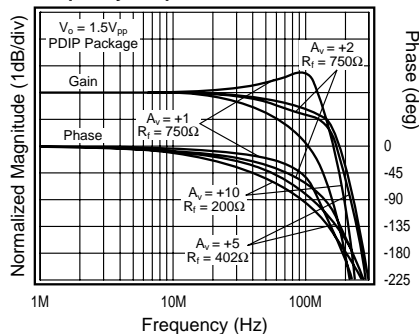


I_{BI} , I_{BN} , V_{IO} vs. Temperature

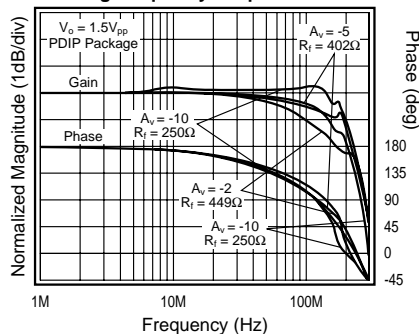


±5V Typical Performance ($A_v = +2$, $R_f = 1\text{k}\Omega$ (PDIP), $R_L = 100\Omega$, $V_{CC} = \pm 5\text{V}$, unless specified)

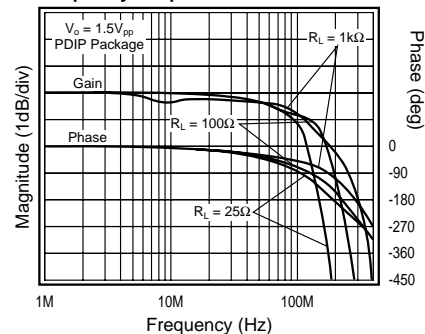
Frequency Response



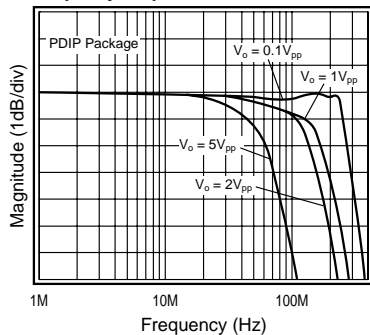
Inverting Frequency Response



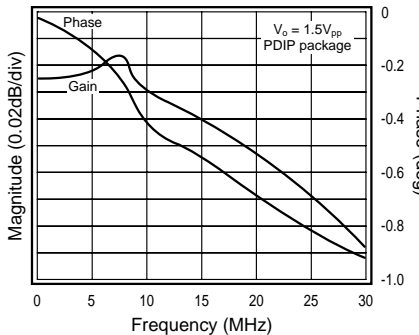
Frequency Response vs. R_L



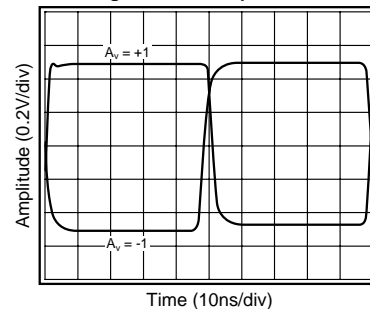
Frequency Response vs. V_o



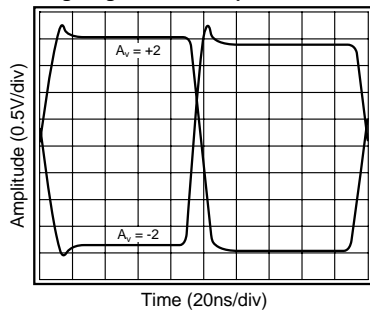
Gain Flatness & Linear Phase



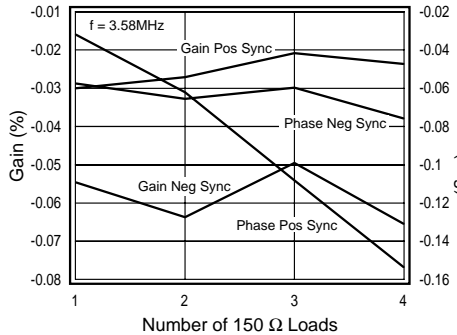
Small Signal Pulse Response



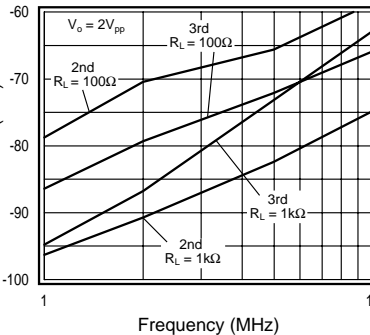
Large Signal Pulse Response



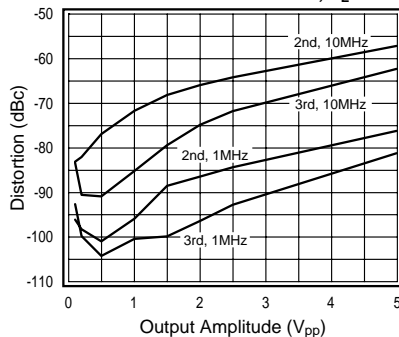
Differential Gain & Phase



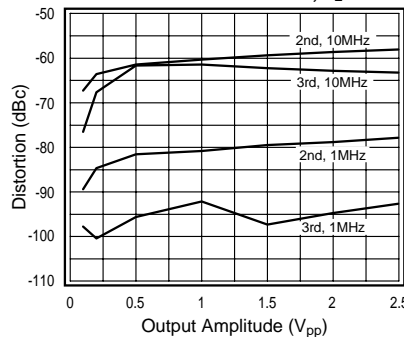
2nd & 3rd Harmonic Distortion



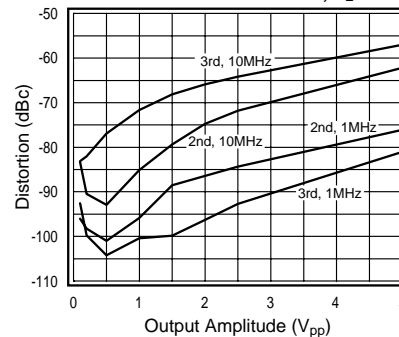
2nd & 3rd Harmonic Distortion, $R_L = 25\Omega$



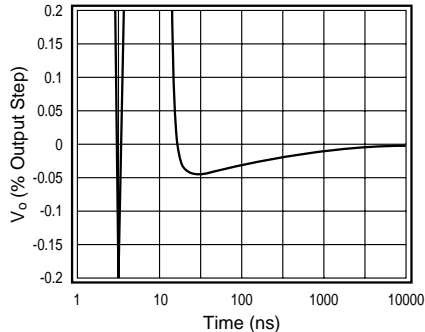
2nd & 3rd Harmonic Distortion, $R_L = 100\Omega$



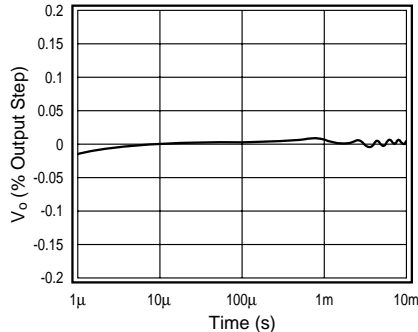
2nd & 3rd Harmonic Distortion, $R_L = 1\text{k}\Omega$



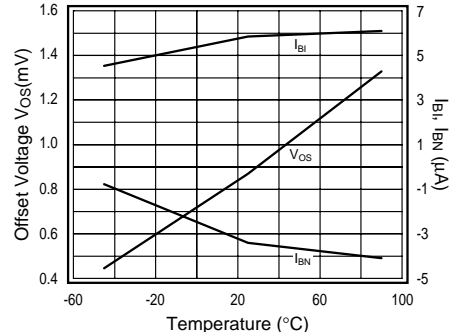
Short Term Settling Time



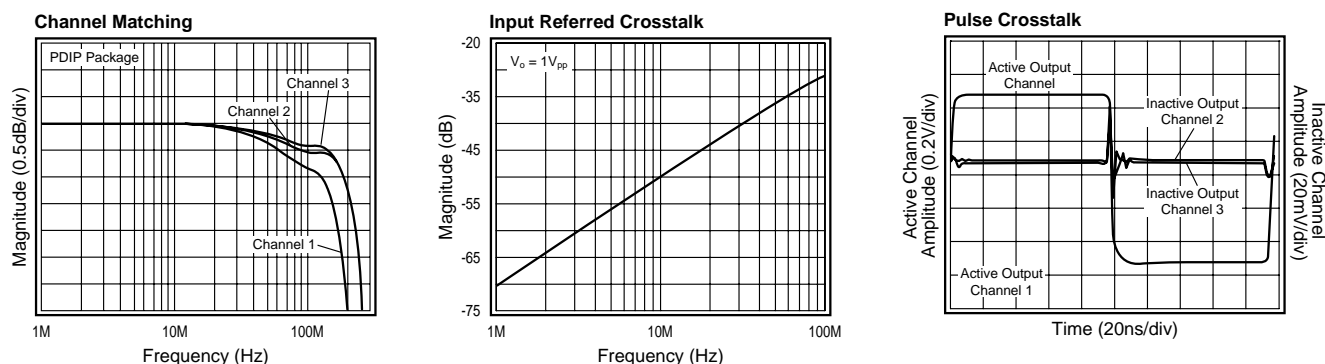
Long Term Settling Time



I_{BI} , I_{BN} , V_{OS} vs. Temperature



±5V Typical Channel Matching Performance ($A_v = +2$, $R_f = 1k\Omega$ (PDIP), $R_L = 100\Omega$, $V_{CC} = \pm 5V$, unless specified)



CLC5623 OPERATION

The CLC5623 is a current feedback amplifier built in an advanced complementary bipolar process. The CLC5623 operates from a single 5V supply or dual $\pm 5V$ supplies. Operating from a single supply, the CLC5623 has the following features:

- Provides 100mA of output current while consuming 15mW of power
- Offers low -85/-96dB 2nd and 3rd harmonic distortion
- Provides BW > 100MHz and 1MHz distortion < -70dBc at $V_o = 2V_{pp}$

The CLC5623 performance is further enhanced in $\pm 5V$ supply applications as indicated in the **±5V Electrical Characteristics** table and **±5V Typical Performance** plots.

Current Feedback Amplifiers

Some of the key features of current feedback technology are:

- Independence of AC bandwidth and voltage gain
- Inherently stable at unity gain
- Adjustable frequency response with feedback resistor
- High slew rate
- Fast settling

Current feedback operation can be described using a simple equation. The voltage gain for a non-inverting or inverting current feedback amplifier is approximated by Equation 1.

$$\frac{V_o}{V_{in}} = \frac{A_v}{1 + \frac{R_f}{Z(j\omega)}} \quad \text{Equation 1}$$

where:

- A_v is the closed loop DC voltage gain
- R_f is the feedback resistor
- $Z(j\omega)$ is the CLC5623's open loop transimpedance gain
- $\frac{Z(j\omega)}{R_f}$ is the loop gain

The denominator of Equation 1 is approximately equal to 1 at low frequencies. Near the -3dB corner frequency, the interaction between R_f and $Z(j\omega)$ dominates the circuit performance. The value of the feedback resistor has a large affect on the circuits performance. Increasing R_f has the following affects:

- Decreases loop gain
- Decreases bandwidth
- Reduces gain peaking
- Lowers pulse response overshoot
- Affects frequency response phase linearity

Refer to the **Feedback Resistor Selection** section for more details on selecting a feedback resistor value.

CLC5623 DESIGN INFORMATION

Single Supply Operation ($V_{CC} = +5V$, $V_{EE} = \text{GND}$)

The specifications given in the **±5V Electrical Characteristics** table for single supply operation are measured with a common mode voltage (V_{cm}) of 2.5V. V_{cm} is the voltage around which the inputs are applied and the output voltages are specified.

Operating from a single +5V supply, the Common Mode Input Range (CMIR) of the CLC5623 is typically +0.8V to

+4.2V. The typical output range with $R_L = 100\Omega$ is +1.0V to +4.0V.

For single supply DC coupled operation, keep input signal levels above 0.8V DC. For input signals that drop below 0.8V DC, AC coupling and level shifting the signal are recommended. The non-inverting and inverting configurations for both input conditions are illustrated in the following 2 sections.

DC Coupled Single Supply Operation

Figures 1 and 2 show the recommended non-inverting and inverting configurations for input signals that remain above 0.8V DC.

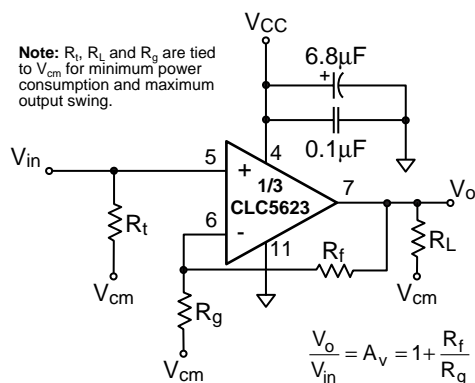


Figure 1: Non-Inverting Configuration

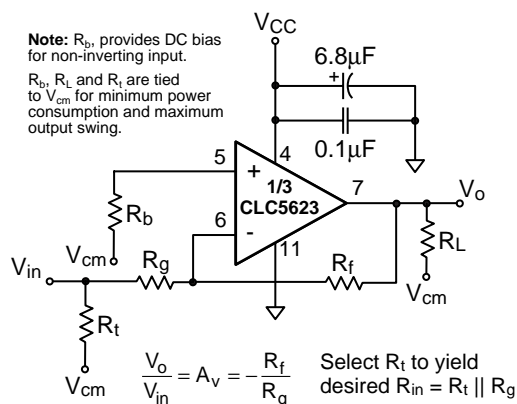


Figure 2: Inverting Configuration

AC Coupled Single Supply Operation

Figures 3 and 4 show possible non-inverting and inverting configurations for input signals that go below 0.8V DC. The input is AC coupled to prevent the need for level shifting the input signal at the source. The resistive voltage divider biases the non-inverting input to $V_{CC} \div 2 = 2.5V$ (For $V_{CC} = +5V$).

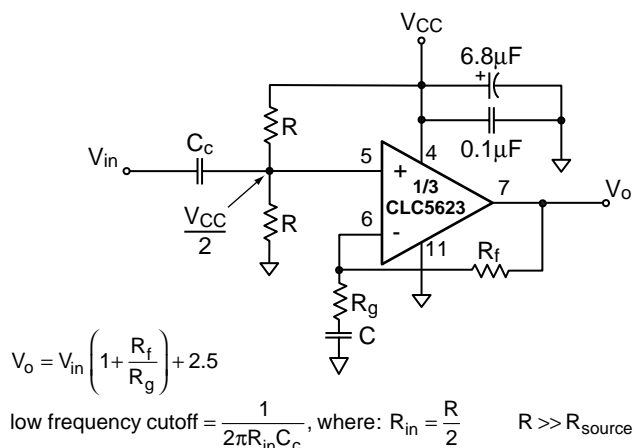


Figure 3: AC Coupled Non-Inverting Configuration

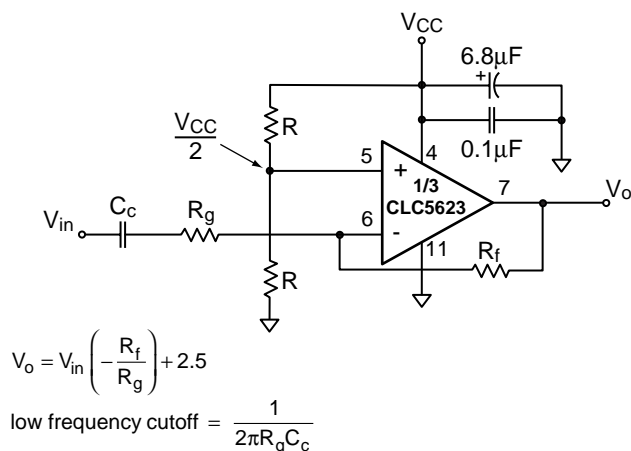


Figure 4: AC Coupled Inverting Configuration

Dual Supply Operation

The CLC5623 operates on dual supplies as well as single supplies. The non-inverting and inverting configurations are shown in Figures 5 and 6.

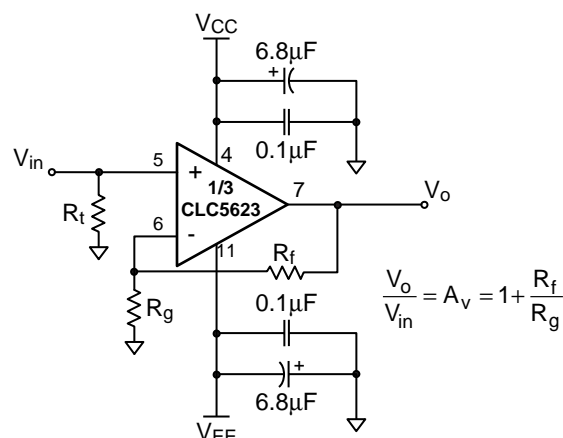


Figure 5: Dual Supply Non-Inverting Configuration

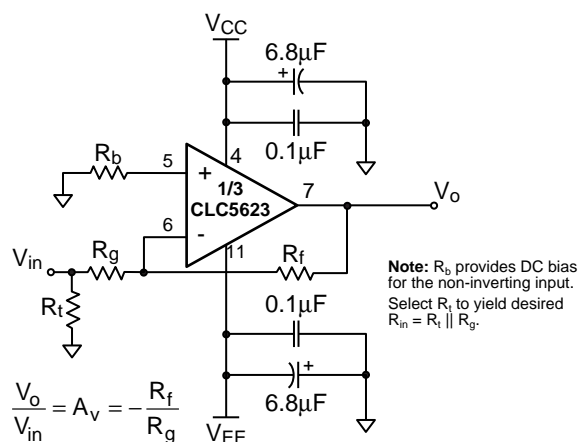


Figure 6: Dual Supply Inverting Configuration

Feedback Resistor Selection

The feedback resistor, R_f , affects the loop gain and frequency response of a current feedback amplifier. Optimum performance of the CLC5623, at a gain of +2V/V, is achieved with R_f equal to 750 Ω for the SOIC package and 1k Ω for the PDIP package. The frequency response plots in the **Typical Performance** sections illustrate the recommended R_f for several gains. These recommended values of R_f provide the maximum bandwidth with minimal peaking. Within limits, R_f can be adjusted to optimize the frequency response.

- Decrease R_f to peak frequency response and extend bandwidth
- Increase R_f to roll off frequency response and compress bandwidth

As a rule of thumb, if the recommended R_f is doubled, then the bandwidth will be cut in half.

Unity Gain Operation

The recommended R_f for unity gain (+1V/V) operation is 750 Ω (for the PDIP package). R_g is left open. Parasitic capacitance at the inverting node may require a slight increase in R_f to maintain a flat frequency response.

Load Termination

The CLC5623 can source and sink near equal amounts of current. For optimum performance, the load should be tied to V_{cm} .

Additional parasitics and limitations on decoupling in the CLC5623IN combine to provide a lower level of performance than the CLC5623IM. The specifications in the Electrical Characteristics tables are based on the performance of the DIP package (CLC5623IN). For optimum performance, use the CLC5623IM (SOIC package). Proper supply decoupling and board layout are critical factors for obtaining optimum performance of the CLC5623IN. Board layout is less critical for the SOIC package. Use the evaluation boards as a guide to proper layout.

Figure 7 illustrates the frequency response versus output amplitude for the CLC5623IM. Compare the **Frequency Response vs. V_o** plot, in the **$\pm 5V$ Typical Performance** section, with Figure 7. Notice that gain flatness and bandwidth improve when the SOIC package is used.

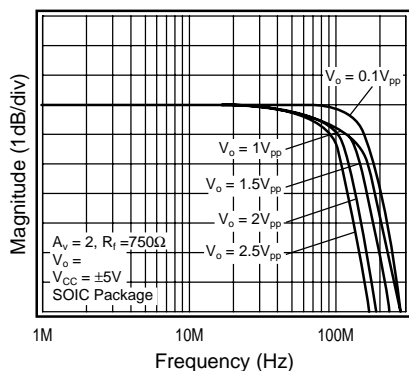


Figure 7: Frequency Response vs. V_o

Figure 8 illustrates the channel matching performance of the surface mount version of the CLC5623. Once again, the surface mount package performs better. If optimum performance is desired, use the surface mount version of the CLC5623.

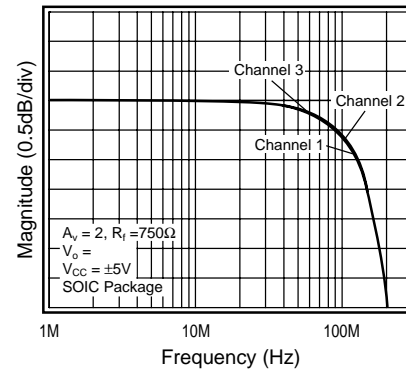


Figure 8: Channel Matching Performance

Driving Cables and Capacitive Loads

When driving cables, double termination is used to prevent reflections. For capacitive load applications, a small series resistor at the output of the CLC5623 will improve stability and settling performance. The **Frequency Response vs. C_L** plot, shown below in Figure 9, gives the recommended series resistance value for optimum flatness at various capacitive loads.

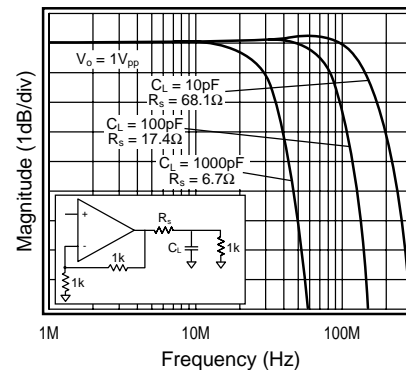


Figure 9: Frequency Response vs. C_L

Transmission Line Matching

One method for matching the characteristic impedance (Z_o) of a transmission line or cable is to place the appropriate resistor at the input or output of the amplifier. Figure 10 shows typical inverting and non-inverting circuit configurations for matching transmission lines.

Non-inverting gain applications:

- Connect R_g directly to ground.
- Make R_1 , R_2 , R_6 , and R_7 equal to Z_o .
- Use R_3 to isolate the amplifier from reactive loading caused by the transmission line, or by parasitics.

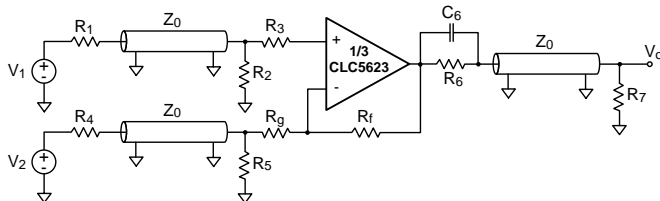


Figure 10: Transmission Line Matching

Inverting gain applications:

- Connect R_3 directly to ground.
- Make the resistors R_4 , R_6 , and R_7 equal to Z_0 .
- Make $R_5 \parallel R_g = Z_0$.

The input and output matching resistors attenuate the signal by a factor of 2, therefore additional gain is needed. Use C_6 to match the output transmission line over a greater frequency range. C_6 compensates for the increase of the amplifier's output impedance with frequency.

Power Dissipation

Follow these steps to determine the power consumption of the CLC5623:

1. Calculate the quiescent (no-load) power:

$$P_{amp} = I_{CC} (V_{CC} - V_{EE})$$
2. Calculate the RMS power at the output stage:

$$P_o = (V_{CC} - V_{load}) (I_{load})$$
, where V_{load} and I_{load} are the RMS voltage and current across the external load.
3. Calculate the total RMS power:

$$P_t = P_{amp} + P_o$$

The maximum power that the DIP and SOIC packages can dissipate at a given temperature is illustrated in Figure 11. The power derating curve for any CLC5623 package can be derived by utilizing the following equation:

$$\frac{(175^\circ - T_{amb})}{\theta_{JA}}$$

where

T_{amb} = Ambient temperature ($^\circ\text{C}$)

θ_{JA} = Thermal resistance, from junction to ambient, for a given package ($^\circ\text{C}/\text{W}$)

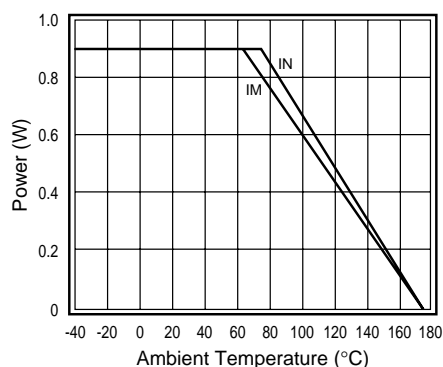


Figure 11: Power Derating Curves

Layout Considerations

A proper printed circuit layout is essential for achieving high frequency performance. National provides evaluation boards for the CLC5623 (CLC730075-DIP, CLC730074-SOIC) and suggests their use as a guide for high frequency layout and as an aid for device testing and characterization.

General layout and supply bypassing play major roles in high frequency performance. Follow the steps below as a basis for high frequency layout:

- Include 6.8 μF tantalum and 0.1 μF ceramic capacitors on both supplies.
- Place the 6.8 μF capacitors within 0.75 inches of the power pins.
- Place the 0.1 μF capacitors less than 0.1 inches from the power pins.
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance.
- Minimize all trace lengths to reduce series inductances.
- Use flush-mount printed circuit board pins for prototyping, never use high profile DIP sockets.

Evaluation Board Information

A data sheet is available for the CLC730075/ CLC730074 evaluation boards. The evaluation board data sheet provides:

- Evaluation board schematics
- Evaluation board layouts
- General information about the boards

The evaluation boards are designed to accommodate dual supplies. The boards can be modified to provide single supply operation. For best performance; 1) do not connect the unused supply, 2) ground the unused supply pin.

SPICE Models

SPICE models provide a means to evaluate amplifier designs. Free SPICE models are available for National's monolithic amplifiers that:

- Support Berkeley SPICE 2G and its many derivatives
- Reproduce typical DC, AC, Transient, and Noise performance
- Support room temperature simulations

The **readme** file that accompanies the diskette lists released models, and provides a list of modeled parameters. The application note OA-18, Simulation SPICE Models for National's Op Amps, contains schematics and a reproduction of the readme file.

Application Circuits

Single Supply Cable Driver

The typical application shown below shows one of the CLC5623 amplifiers driving 10m of 75Ω coaxial cable. The CLC5623 is set for a gain of +2V/V to compensate for the divide-by-two voltage drop at V_o .

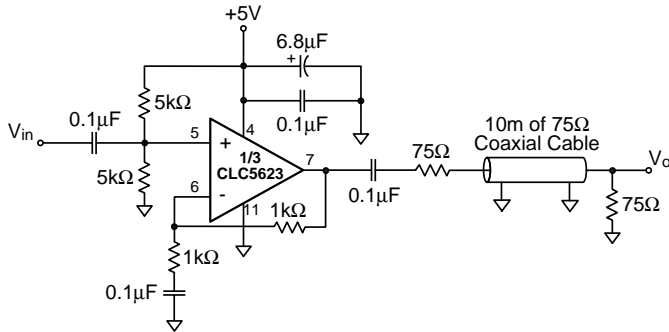


Figure 12: Single Supply Cable Driver

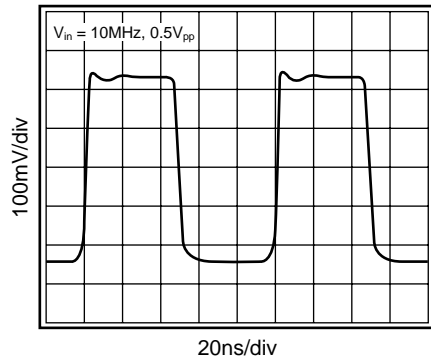


Figure 13: Response After 10m of Cable

Single Supply Lowpass Filter

Figures 14 and 15 illustrate a lowpass filter and design equations. The circuit operates from a single supply of +5V. The voltage divider biases the non-inverting input to 2.5V. And the input is AC coupled to prevent the need for level shifting the input signal at the source. Use the design equations to determine R_1 , R_2 , C_1 , and C_2 based on the desired Q and corner frequency.

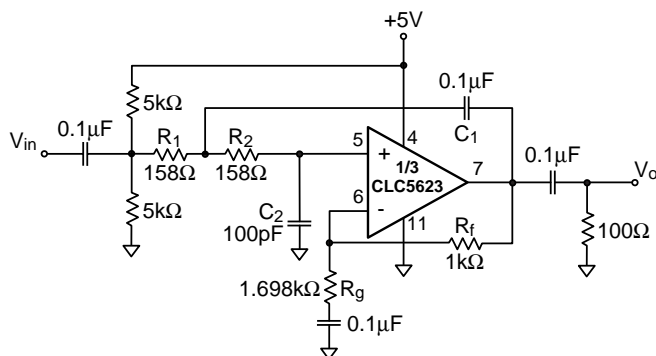


Figure 14: Lowpass Filter Topology

$$\text{Gain} = K = 1 + \frac{R_f}{R_g}$$

$$\text{Corner frequency} = \omega_c = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}}$$

$$Q = \frac{1}{\sqrt{\frac{R_2 C_2}{R_1 C_1}} + \sqrt{\frac{R_1 C_2}{R_2 C_1}} + (1-K) \sqrt{\frac{R_1 C_1}{R_2 C_2}}}$$

For $R_1 = R_2 = R$ and $C_1 = C_2 = C$

$$\omega_c = \frac{1}{RC}$$

$$Q = \frac{1}{(3-K)}$$

Figure 15: Design Equations

This example illustrates a lowpass filter with $Q = 0.707$ and corner frequency $f_c = 10\text{MHz}$. A Q of 0.707 was chosen to achieve a maximally flat, Butterworth response. Figure 16 indicates the filter response.

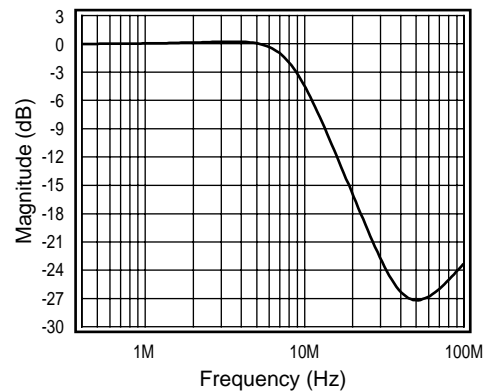


Figure 16: Lowpass Response

Differential Line Driver With Load Impedance Conversion

The circuit shown in the *Typical Application* schematic on the front page and in Figure 17, operates as a differential line driver. The transformer converts the load impedance to a value that best matches the CLC5623's output capabilities. The single-ended input signal is converted to a differential signal by the CLC5623. The line's characteristic impedance is matched at both the input and the output. The schematic shows Unshielded Twisted Pair for the transmission line; other types of lines can also be driven.

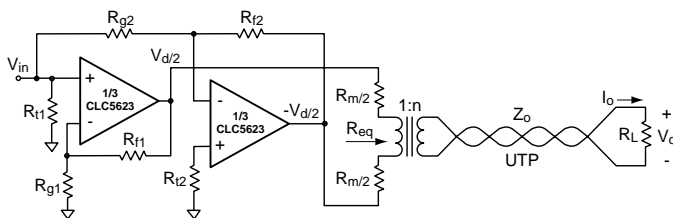


Figure 17: Differential Line Driver with Load Impedance Conversion

Set up the CLC5623 as a difference amplifier:

$$\frac{V_d}{V_{in}} = 2 \cdot \left(1 + \frac{R_{f1}}{R_{g1}} \right) = 2 \cdot \frac{R_{f2}}{R_{g2}}$$

Make the best use of the CLC5623's output drive capability as follows:

$$R_m + R_{eq} = \frac{2 \cdot V_{max}}{I_{max}}$$

where R_{eq} is the transformed value of the load impedance, V_{max} is the Output Voltage Range, and I_{max} is the maximum Output Current.

Match the line's characteristic impedance:

$$\begin{aligned} R_L &= Z_0 \\ R_m &= R_{eq} \\ n &= \sqrt{\frac{R_L}{R_{eq}}} \end{aligned}$$

Select the transformer so that it loads the line with a value very near Z_0 over frequency range. The output impedance of the CLC5623 also affects the match. With an ideal transformer we obtain:

$$\text{Return Loss} = -20 \cdot \log_{10} \left| \frac{n^2 \cdot Z_{o(5623)}(j\omega)}{Z_0} \right|, \text{dB}$$

where $Z_{o(5623)}(j\omega)$ is the output impedance of the CLC5623 and $|Z_{o(5623)}(j\omega)| \ll R_m$.

The load voltage and current will fall in the ranges:

$$\begin{aligned} |V_o| &\leq n \cdot V_{max} \\ |I_o| &\leq \frac{I_{max}}{n} \end{aligned}$$

The CLC5623's high output drive current and low distortion make it a good choice for this application.

Bandpass Filter

Figure 18 illustrates a low-sensitivity bandpass filter and design equations. This topology utilizes the CLC5623's closely matched amplifiers to obtain low op-amp sensitivity at high frequencies. The third CLC5623 is used as a buffer to obtain low output impedance. The overall circuit gain is unity. For additional gain, the third CLC5623 can be configured as a non-inverting amplifier.

To design the filter, choose C and then determine values for R and R_1 based on the desired resonant frequency (f_r) and Q factor.

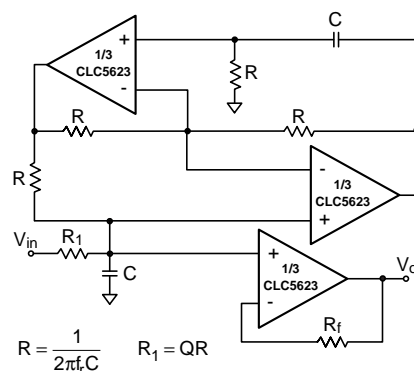


Figure 18: Bandpass Filter Topology

Instrumentation Amplifier

An instrumentation circuit is shown on the front page and reproduced in Figure 19. The DC CMRR can be fine tuned by adjusting R_1 .

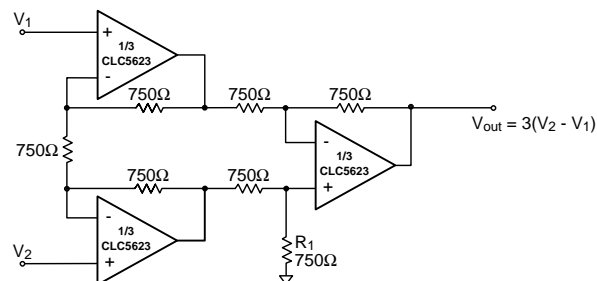


Figure 19: Instrumentation Amplifier

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