June 1999

National Semiconductor

# CLC5654
# Very High-Speed, Low-Cost, Quad Operational Amplifier

## General Description

The CLC5654 is a quad, current feedback operational amplifier that is perfect for many cost-sensitive applications that require high performance. This device also offers excellent economy in board space and power, consuming only 5mA per amplifier while providing 70mA of output current capability. Applications requiring significant density of high speed devices such as video routers, matrix switches and high-order active filters will benefit from the configuration of the CLC5654 and the low channel-to-channel crosstalk of 70dB at 5MHz.

The CLC5654 provides excellent performance for video applications. Differential gain and phase of 0.03% and 0.03° makes this device well suited for many professional composite video systems, but consumer applications will also be able to take advantage of these features due to the device's low cost. The CLC5654 offers superior dynamic performance with a small signal bandwidth of 450MHz and slew rate of 2000V/µs. These attributes are well suited for many component video applications such as driving RGB signals down significant lengths of cable. These and many other application can also take advantage of the 0.1dB flatness to 40MHz.

Combining wide bandwidth with low cost makes the the CLC5654 an attractive option for active filters. SAW filters are often used in IF filters in the 10's of MHz range, but higher order filters designed around a quad operational amplifier may offer an economical alternative to the typical SAW approach and offer greater freedom in the selection of filter parameters. National Semiconductor's Comlinear Products Group has published a wide array of liturature on active filters and a list of these publications can be found on the last page of this datasheet.

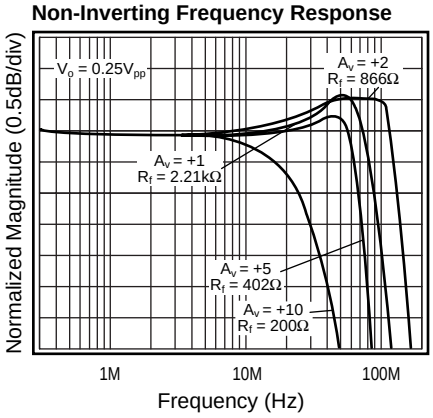
## Features

- 450MHz small signal bandwidth
- 2000 V/µs slew rate
- 5mA / channel supply current
- -71/-82dBc HD2/HD3 (5MHz)
- 0.03%, 0.03° differential gain, phase
- 70mA output current
- 12ns settling to 0.1%

## Applications

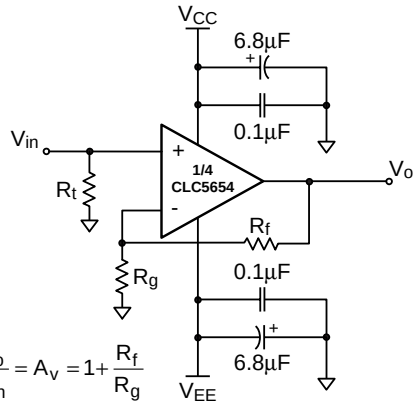
- High performance RGB video
- Video switchers & routers
- Video line driver
- Active filters
- IF amplifier
- Twisted pair driver/receiver

**Non-Inverting Frequency Response**

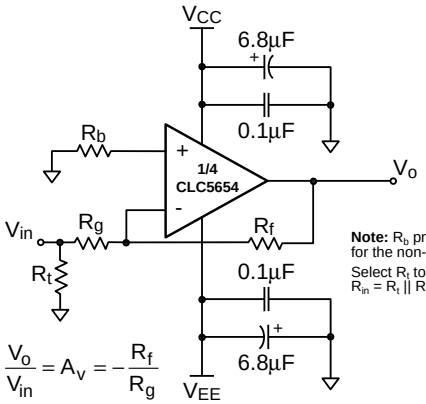



## Typical Configurations

**Non-Inverting Gain**

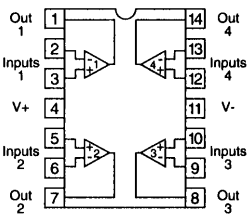



**Inverting Gain**




**Note:** $R_b$ provides DC bias for the non-inverting input. Select $R_t$ to yield desired $R_{in} = R_t \parallel R_g$.

**Pinout**
DIP & SOIC

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## CLC5654 Electrical Characteristics ($A_v$ = +2, $R_f$ = 866Ω, $R_L$ = 100Ω, $V_s$ = ±5V, unless specified)

| PARAMETERS | CONDITIONS | TYP | MIN/MAX RATINGS | | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Ambient Temperature | CLC5654I | +25°C | +25°C | -40 to 85°C | | |
| **FREQUENCY DOMAIN RESPONSE** | | | | | | |
| -3dB bandwidth | $A_v$ = 1 | 450 | – | – | MHz | |
| | $V_o$ < 0.5$V_{pp}$ | 350 | – | – | MHz | |
| | $V_o$ < 5$V_{pp}$ | 100 | – | – | MHz | |
| 0.1dB bandwidth | | 40 | – | – | MHz | |
| differential gain | NTSC, $R_L$ = 150Ω | 0.03 | – | – | dB | |
| differential phase | NTSC, $R_L$ = 150Ω | 0.03 | – | – | dB | |
| **TIME DOMAIN RESPONSE** | | | | | | |
| rise and fall time | 0.5V step | 1.2 | – | – | ns | |
| | 5V step | 2.7 | – | – | ns | |
| settling time to 0.1% | 2V step | 12 | – | – | ns | |
| overshoot | 0.5V step | 7 | – | – | % | |
| slew rate | | 2000 | – | – | V/µs | |
| **DISTORTION AND NOISE RESPONSE** | | | | | | |
| 2nd harmonic distortion | 2$V_{pp}$, 5MHz | -71 | – | – | dBc | |
| 3rd harmonic distortion | 2$V_{pp}$, 5MHz | -82 | – | – | dBc | |
| equivalent input noise | | | | | | |
| voltage ($e_{ni}$) | >1MHz | 3.3 | – | – | nV/√Hz | |
| non-inverting current ($i_{bn}$) | >1MHz | 2.5 | – | – | pA/√Hz | |
| inverting current ($i_{bi}$) | >1MHz | 12 | – | – | pA/√Hz | |
| crosstalk (input inferred) | 10MHz | 76 | – | – | dBc | |
| **STATIC DC PERFORMANCE** | | | | | | |
| input offset voltage | | 2.5 | 6 | 11 | mV | A |
| average drift | | 18 | – | 55 | µV/°C | |
| input bias current (non-inverting) | | 6 | 15 | 28 | µA | A |
| average drift | | 40 | – | 160 | nA/°C | |
| input bias current (inverting) | | 5 | 12 | 20 | µA | A |
| average drift | | 25 | – | 120 | nA/°C | |
| power supply rejection ratio | DC | 55 | 47 | 45 | dB | |
| common-mode rejection ratio | DC | 50 | 45 | 43 | dB | |
| supply current (per channel) | $R_L$= ∞ | 5 | 6.7 | 7 | mA | A |
| **MISCELLANEOUS PERFORMANCE** | | | | | | |
| input resistance (non-inverting) | | 1 | 0.5 | 0.25 | MΩ | |
| input capacitance (non-inverting) | | 1 | 2 | 2 | pF | |
| common-mode input range | | ±2.2 | ±2.0 | ±1.4 | V | |
| output voltage range | $R_L$ = 150Ω | ±2.6 | ±2.5 | ±2.3 | V | |
| output current | | 70 | 50 | 40 | mA | |
| output resistance, closed loop | DC | 0.2 | 0.3 | 0.6 | mΩ | |

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

## Notes

A) J-level: spec is 100% tested at +25°C.

## Reliability Information

| | |
|---|---|
| Transistor Count | 152 |
| MTBF (based on limited test data) | 12.5Mhr |

## Package Thermal Resistance

| Package | $\theta_{JC}$ | $\theta_{JA}$ |
|---|---|---|
| Plastic (IN) | 60°C/W | 110°C/W |
| Surface Mount (IM) | 55°C/W | 125°C/W |

## Absolute Maximum Ratings

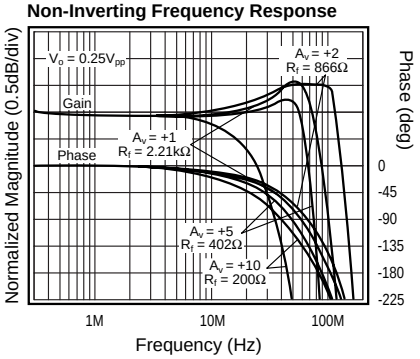
| | |
|---|---|
| supply voltage ($V_{CC}$ - $V_{EE}$) | +14V |
| output current | 95mA |
| common-mode input voltage | $V_{EE}$ to $V_{CC}$ |
| maximum junction temperature | +150°C |
| storage temperature range | -65°C to +150°C |
| lead temperature (soldering 10 sec) | +300°C |

## Ordering Information

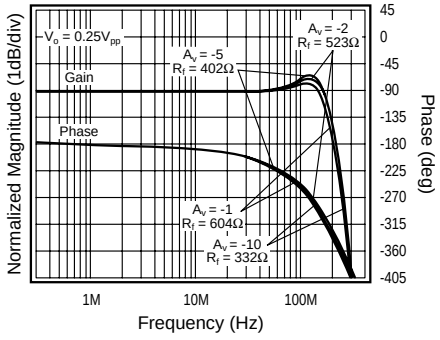
| Model | Temperature Range | Description |
|---|---|---|
| CLC5654IN | -40°C to +85°C | 14-pin PDIP |
| CLC5654IM | -40°C to +85°C | 14-pin SOIC |
| CLC5654IMX | -40°C to +85°C | 14-pin tape and reel |

# CLC5654 Typical Performance ($A_V$ = +2, $R_f$ = 866Ω, $R_L$ = 100Ω, $V_S$ = ±5V, unless specified)

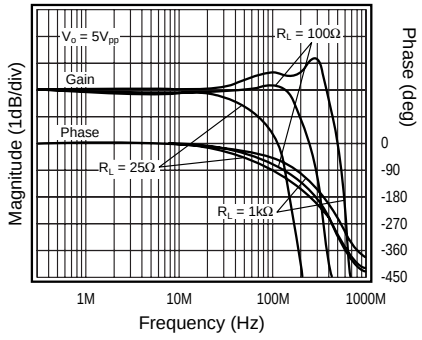
**Non-Inverting Frequency Response**



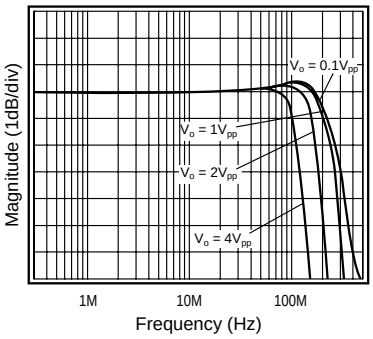

**Inverting Frequency Response**



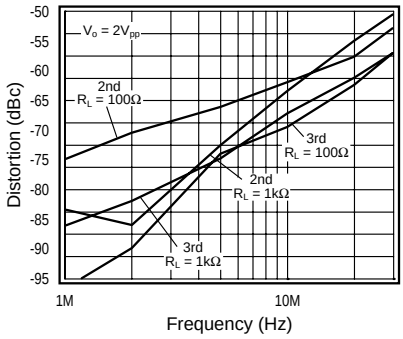

**Frequency Response vs. $R_L$**



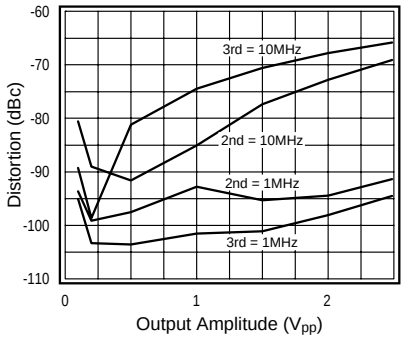

**Frequency Response vs. $V_o$**



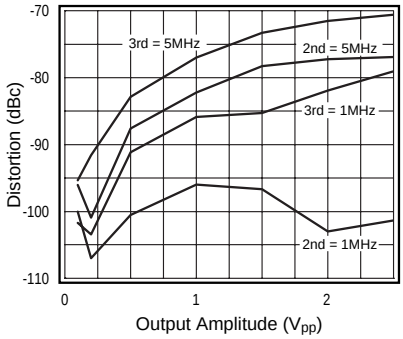

**2nd & 3rd Harmonic Distortion**



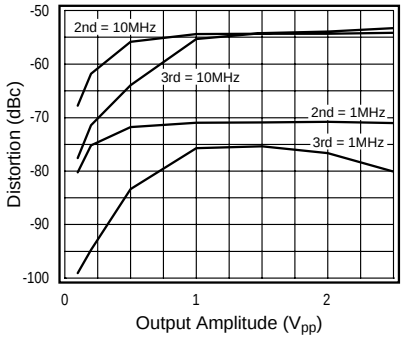

**2nd & 3rd Harmonic Distortion, $R_L$ = 1kΩ**



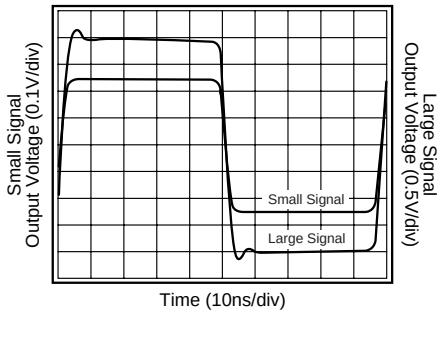

**2nd & 3rd Harmonic Distortion, $R_L$ = 100Ω**



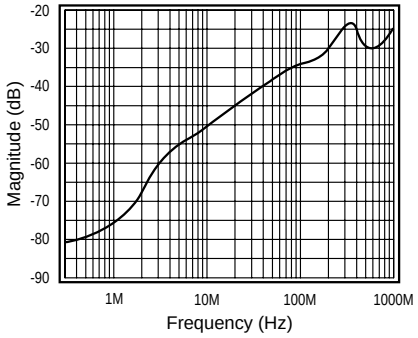

**2nd & 3rd Harmonic Distortion, $R_L$ = 25Ω**



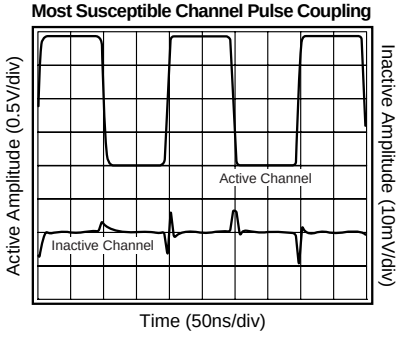

**Large & Small Signal Pulse Response**



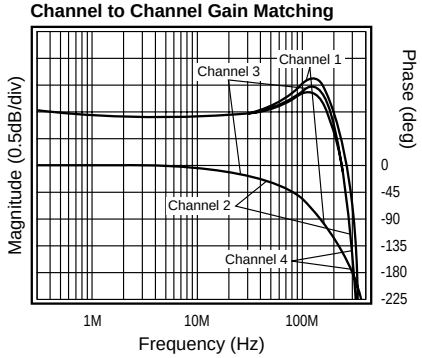

**All Hostile Crosstalk**



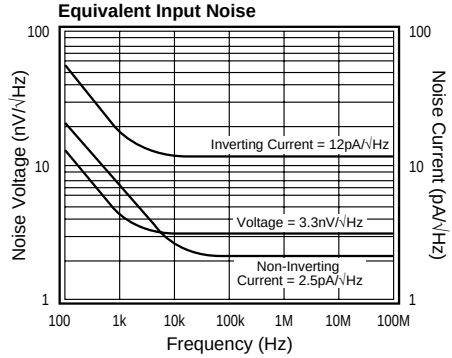

**Most Susceptible Channel Pulse Coupling**



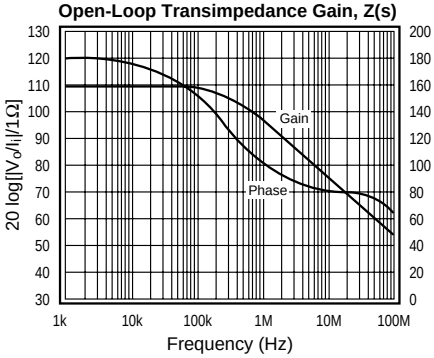

**Channel to Channel Gain Matching**



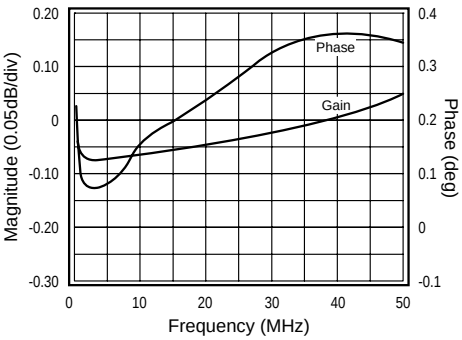

**Equivalent Input Noise**




**Open-Loop Transimpedance Gain, Z(s)**




**Gain Flatness & Linear Phase**



### Current Feedback Amplifiers

Some of the key features of current feedback technology are:

- Independence of AC bandwidth and voltage gain
- Inherently stable at unity gain
- Adjustable frequency response with $R_f$
- High slew rate
- Fast settling

Current feedback operation can be described using a simple equation. The voltage gain for a non-inverting or inverting current feedback amplifier is approximated by Equation 1.

$$\frac{V_o}{V_i} = \frac{A_v}{1 + \frac{R_f}{Z(j\omega)}} \qquad \text{Equation 1}$$

where:

$A_v$ is the closed loop DC voltage gain
$R_f$ is the feedback resistor
$Z(j\omega)$ is the open loop transimpedance gain

The denominator of Equation 1 is approximately equal to 1 at low frequencies. Near the -3dB corner frequency, the interaction between $R_f$ and $Z(j\omega)$ dominates the circuit performance. The value of the feedback resistor has a large affect on the circuits performance. Increasing $R_f$ has the following affects:

- Decreases loop gain
- Decreases bandwidth
- Reduces gain peaking
- Lowers pulse response overshoot
- Affects frequency response phase linearity

### Layout Considerations

A proper printed circuit layout is essential for achieving high frequency performance. National provides evaluation boards for the CLC5654 (CLC730024 - DIP, CLC730031 - SOIC) and suggests their use as a guide for high frequency layout and as an aid for device testing and characterization. General layout and supply bypassing play major roles in high frequency performance. Follow the steps below as a basis for high frequency layout:

- Include 6.8µF tantalum and 0.1µF ceramic capacitors on both supplies.
- Place the 6.8µF capacitors within 0.75 inches of the power pins.
- Place the 0.1µF capacitors less than 0.1 inches from the power pins.
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance.
- Minimize all trace lengths to reduce series inductances.
- Use flush-mount printed circuit board pins for prototyping, never use high profile DIP sockets.

### Active Filter Application Notes

OA-21 Simplified Component Pre-Distortion for High Speed Active Filters
OA-26 Designing High-Speed Active Filters
OA-27 Low-Sensitivity, Lowpass Filter Design
OA-28 Low-Sensitivity, Bandpass Filter Design with Tuning Method
OA-29 Low-Sensitivity, Highpass Filter Design with Parasitic Compensation

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