National Semiconductor

May 1995

DP83910A CMOS SNI Serial Network Interface

General Description

The DP83910A CMOS Serial Network Interface (SNI) is a direct-pin equivalent of the bipolar DP8391 SNI and provides the Manchester data encoding and decoding functions for IEEE 802.3 Ethernet/Thin-Ethernet type local area networks. The SNI interfaces the DP8390 Network Interface Controller (NIC) to the DP8392 CTI or an Ethernet transceiver cable. When transmitting, the SNI converts non-return-to-zero (NRZ) data from the controller into Manchester data and sends the converted data differentially to the transceiver. Conversely, when receiving, a Phase Lock Loop decodes the 10 Mbit/s data from the transceiver into NRZ data for the controller.

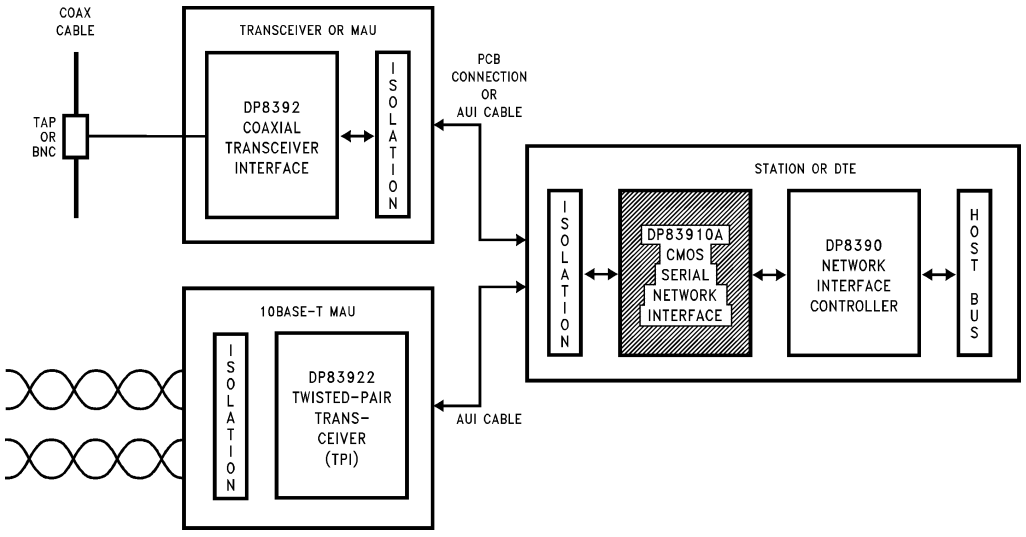
The DP83910A operates in conjunction with the DP8392 Coaxial Transceiver Interface (CTI) and the DP8390 Network Interface Controller (NIC) to form a three-chip set that implements a complete IEEE 802.3 compatible network as shown below. The DP83910A is a functionally complete Manchester encoder/decoder including a balanced driver and receiver, on-board crystal oscillator, collision signal translator, and a diagnostic loopback feature. The DP83910A, fabricated CMOS, typically consumes less than 70 mA of current. However, as a result of being CMOS, the DP83910A's differential signals must be isolated in both Ethernet and thin wire Ethernet.

Features

- Compatible with Ethernet I, IEEE 802.3; 10BASE5, 10BASE2, and 10BASE-T
- Designed to interface with 10BASE-T transceivers
- Functional and pin-out duplicate of the DP8391
- 10 Mbits/s Manchester encoding/decoding with receive clock recovery
- Requires no precision components
- Loopback capability for diagnostics
- Externally selectable half or full step modes of operation at transmit output
- Squelch circuitry at the receive and collision inputs to reject noise
- TTL/MOS compatible controller interface

1.0 System Diagram

IEEE 802.3 Compatible Ethernet/Thin-Ethernet/10 BaseT Local Area Network Chip Set



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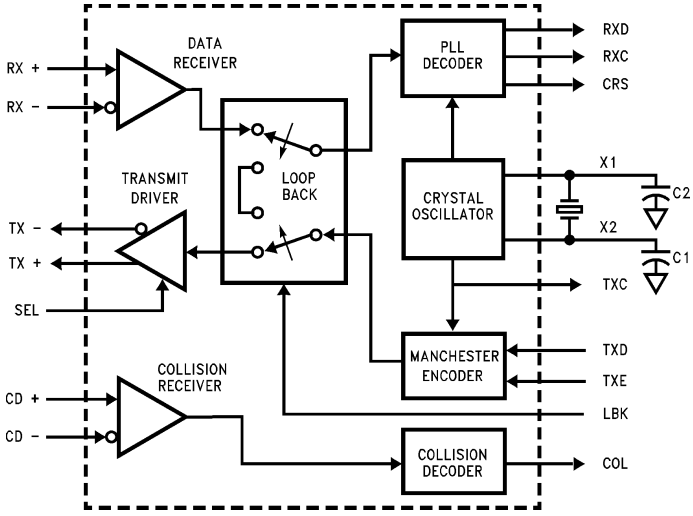
2.0 Block Diagram



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3.0 Functional Description

The DP83910A consists of five main logical blocks:

a) The oscillator generates the 10 MHz transmit clock signal for system timing.

b) The Manchester encoder accepts NRZ data from the controller, encodes the data to Manchester, and transmits it differentially to the transceiver, through the differential transmit driver.

c) The Manchester decoder receives Manchester data from the transceiver, converts it to NRZ data and clock pulses, and sends it to the controller.

d) The collision translator indicates to the controller the presence of a valid 10 MHz collision signal to the PLL.

e) The loopback circuitry, when asserted, routes the data from the Manchester encoder back to the PLL decoder.

3.1 OSCILLATOR

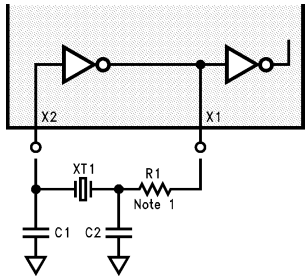
The oscillator is controlled by a 20 MHz parallel resonant crystal connected between X1 and X2 or by an external clock on X1. The 20 MHz output of the oscillator is divided by 2 to generate the 10 MHz transmit clock for the controller. The oscillator also provides internal clock signals to the encoding and decoding circuits.

If a crystal is connected to the DP83910A, it is recommended that the circuit shown in *Figure 1* be used and that the components used meet the following:

Crystal XT1: AT cut parallel resonant crystal
Series Resistance: $\leq 10\Omega$
Specified Load Capacitance: 13.5 pF
Accuracy: 0.005% (50 ppm)

C1, C2: Load Capacitor, 27 pF.

The resistor, R1, in *Figure 1* may be required in order to minimize frequency drift due to changes in the V_{CC} supply voltage. If R1 is required, it's value must be carefully selected. R1 decreases the loop gain. Thus, if R1 is made too large, the loop gain will be greatly reduced and the crystal will not oscillate. If R1 is made too small, normal variations in the V_{CC} may cause the oscillation frequency to drift out of specification. As the first rule of thumb, the value of R1 should be made equal to five times the motional resistance of the crystal.



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Note 1: The resistor R1 may be required in order to minimize frequency drift due to changes in the V_{CC}. See text description.

FIGURE 1. Crystal Connection to DP83910A
(see text for component values)

The motional resistance of 20 MHz crystals is usually in the range of 10Ω to 30Ω. This implies that a reasonable value for R1 should be in the range of $50\Omega - 150\Omega$.

The decision of whether or not to include R1 should be based upon measured variations of crystal frequency as each of the circuit parameters is varied.

According to the IEEE 802.3 standard, the entire oscillator circuit (crytsal and amplifier) must be accurate to 0.01%. When using a crystal, the X1 pin is not guaranteed to provide a TTL compatible logic output, and should not be used to drive external standard logic. If additional logic needs to be driven, then an external oscillator should be used, as described in the following.

3.2 OSCILLATOR MODULE OPERATION

If the designer wishes to use a crystal clock oscillator, one that provides the following should be employed:
1) TTL or CMOS output with a 0.01% frequency tolerance
2) 40%–60% duty cycle
3) ≥ 2 TTL load output drive (I_{OL} = 3.2 mA)

3.0 Functional Description (Continued)

The circuit is shown in *Figure 2*. (Additional output drive may be necessary if the oscillator must also drive other components.) When using a clock oscillator it is still recommended that the designer connect the oscillator output to the X1 pin and tie the X2 pin to ground.

3.3 MANCHESTER ENCODER AND DIFFERENTIAL DRIVER

The encoder begins operation when the Transmit Enable input (TXE) goes high and converts clock and NRZ data to Manchester data for the transceiver. For the duration of TXE remaining high, the Transmitted Data (TXD) is encoded for the transmit-driver pair (TX±). TXD must be valid on the rising edge of Transmit Clock (TXC). Transmission ends when TXE goes low. The last transition is always positive; it occurs at the center of the bit cell if the last bit is a one, or at the end of the bit cell if the last bit is a zero.

The differential transmit pair from the secondary of the isolation transformer drives up to 50 meters of twisted pair AUI cable. These outputs are source followers which require two 270Ω pull-down resistors to ground.

The DP83910A allows both half-step and full-step to be compatible with Ethernet I and IEEE 802.3. With the SEL pin low (for Ethernet I), transmit+ is positive with respect to transmit− during idle; with SEL high (for IEEE 802.3), transmit+ and transmit− are equal in the idle state. This provides zero differential voltage to operate with transformer coupled loads.

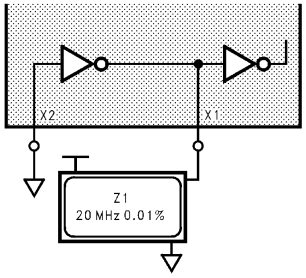

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FIGURE 2. DP83910A Connection for Oscillator Module

3.4 MANCHESTER DECODER

The decoder consists of a differential receiver and a PLL to separate Manchester encoded data stream into clock signals and NRZ data. The differential input must be externally terminated with two 39Ω resistors connected in series if the standard 78Ω transceiver drop cable is used; in Thin-Ethernet applications, these resistors are optional. To prevent noise from falsely triggering the decoder, a squelch circuit at the input rejects signals with levels less than −175 mV. Once the input exceeds the squelch requirements, Carrier Sense (CRS) is asserted. Receive data (RXD) and receive clock (RXC) become valid typically within 6 bit times. The DP83910A may tolerate bit jitter up to 18 ns in the received data.

The decoder detects the end of a frame when no more midbit transitions are detected. Within one and a half bit times after the last bit, carrier sense is de-asserted. Receive clock stays active for five more bit times after CRS goes low to guarantee the receive timings of the DP8390 NIC.

3.5 COLLISION TRANSLATOR

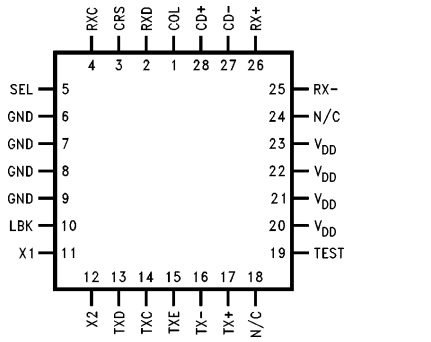
When the Ethernet transceiver (DP8392 CTI) detects a collision, it generates a 10 MHz signal to the differential collision inputs (CD±) of the DP83910A. When these inputs are detected active, the DP83910A translates the 10 MHz signal to an active high level for the controller. The controller uses this signal to back off its current transmission and reschedule another one.

The collision differential inputs are terminated the same way as the differential receive inputs. The squelch circuitry is also similar, rejecting pulses with levels less than −175 mV.

3.6 LOOPBACK FUNCTIONS

When the Loopback input (LBK) is asserted high, the DP83910A redirects its transmitted data back into its receive path. This feature provides a convenient method for testing both chip and system level integrity. The transmit driver and receive input circuitry are disabled in loopback mode.

4.0 Connection Diagrams



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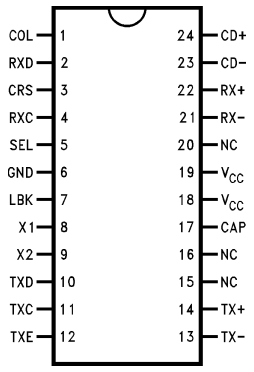
Top View

Order Number DP83910AV
See NS Package Number V28A



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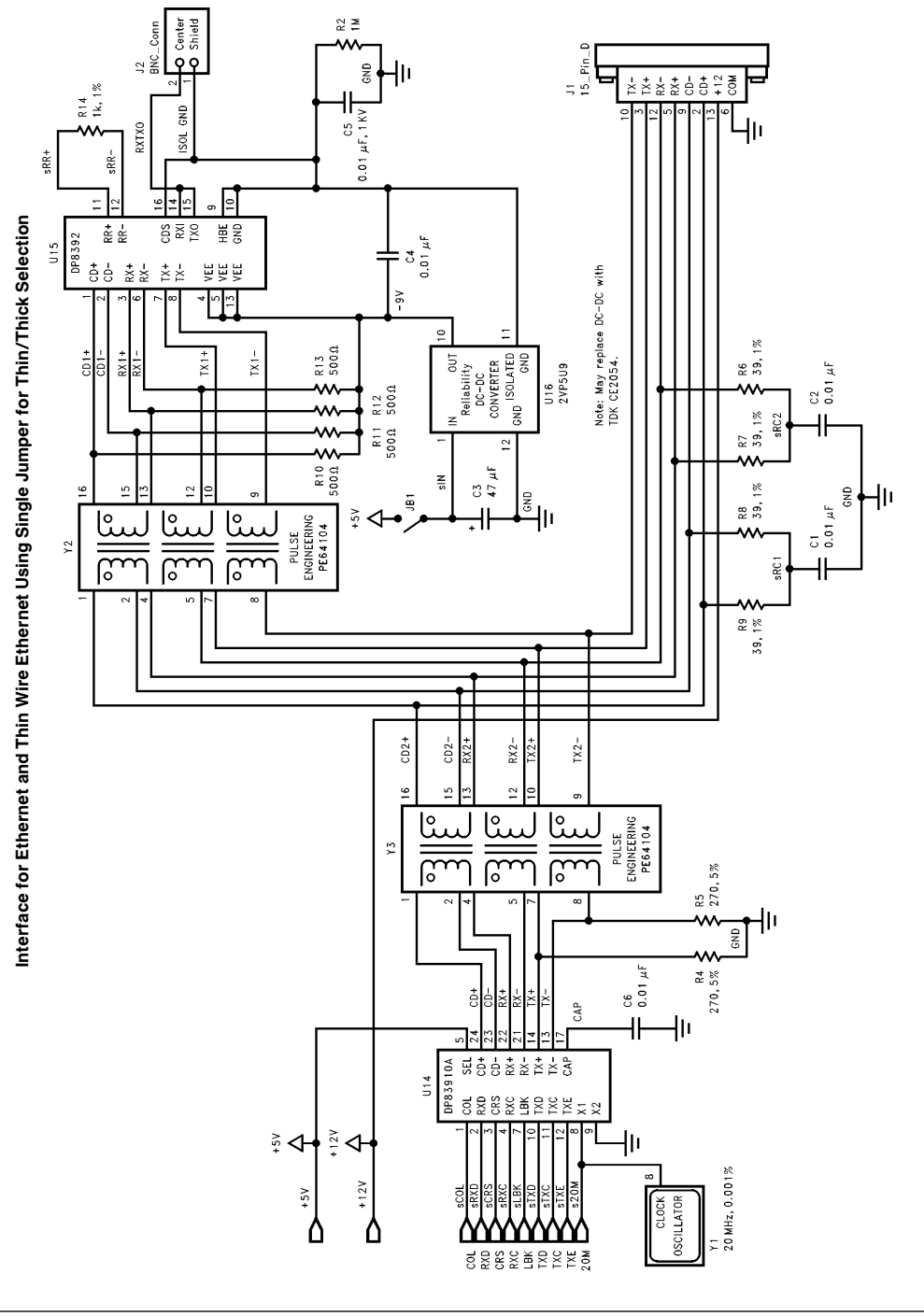
Top View

Order Number DP83910AN
See NS Package Number N24C

5.0 Typical Application



6.0 Pin Descriptions

24-Pin DIP	28-Pin PCC	Name	I/O	Description
1	1	COL	O	**COLLISION DETECT OUTPUT:** Generates an active high signal when 10 MHz collision signal is detected.
2	2	RXD	O	**RECEIVE DATA OUTPUT:** NRZ data output from the PLL. This signal must be sampled on the rising edge of receive clock.
3	3	CRS	O	**CARRIER SENSE:** Asserted on the first valid high-to-low transition on the RX± pair. Remains active until 1.5 bit times after the last bit in data.
4	4	RXC	O	**RECEIVE CLOCK:** The receive clock from the Manchester data after the PLL has locked. Remains active 5 bit times after deasserting CRS.
5	5	SEL	I	**MODE SELECT:** When high, transmit+ and transmit− are the same voltage in the idle state. When low, transmit+ is positive with respect to transmit− in the idle state, at the transformer's primary.
6	7 8 9	V_{SS} V_{SS} V_{SS}		**GROUND PIN**
7	10	LBK	I	**LOOPBACK:** When high, the loopback mode is enabled.
8	11	X1	I	**CRYSTAL OR EXTERNAL OSCILLATOR INPUT**
9	12	X2	O	**CRYSTAL FEEDBACK OUTPUT:** Used in crystal connections only. Connected to ground when using an external oscillator.
10	13	TXD	I	**TRANSMIT DATA INPUT:** NRZ data input from the controller. The data is combined with the transmit clock to produce Manchester data. TXD is sampled on the rising edge of transmit clock.
11	14	TXC	O	**TRANSMIT CLOCK:** The 10 MHz clock derived from the 20 MHz oscillator.
12	15	TXE	I	**TRANSMIT ENABLE:** The encoder begins operation when this input is asserted high.
13 14	16 17	TX− TX+	O	**TRANSMIT OUTPUT:** Differential line driver which sends the encoded data to the transceiver. The outputs are source followers which require 270Ω pull-down resistors.
15	6	NC		**NO CONNECTION:** This may be tied to V_{SS} for the PLCC version to be compatible with the DP8391.
16	18	NC		**NO CONNECTION**
17	19	TEST	I	**FACTORY TEST INPUT:** Used to check the chip's internal functions. May be tied low or have a 0.01 μf bypass capacitor to ground (for compatibility with the bipolar DP8391) during normal operation.
18 19	20 21 22 23	V_{DD} V_{DD} V_{DD} V_{DD}		**POWER CONNECTION**
20	24	NC		**NO CONNECTION**
21 22	25 26	RX− RX+	I	**RECEIVE INPUT:** Differential receive input pair from the transceiver.
23 24	27 28	CD− CD+	I	**COLLISION INPUT:** Differential collision pair input from the transceiver.

7.0 Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7V
DC Input Voltage (V_{IN})	−0.5V to V_{CC} +0.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
Differential Input Voltage	−5.5 to +16V
Differential Output Voltage	0 to 16V
Power Dissipation	500 mW
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C
ESD (R_{ZAP} = 1.5 kΩ, C_{ZAP} = 120 pF)	≥2 kV (Pin 4 = 1.5 kV)

Note: *Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.*

***Note:** An asterisk following a parameter's symbol indicates that the parameter has been characterized but not tested.

Note: All specifications in this datasheet are valid only if the mandatory isolation is employed and all differential signals are taken to exist at the AUI side of the pulse transformer.

8.0 DC Specifications T_A = 0°C to 70°C, V_{CC} = 5V ±5%

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Controller Interface Pins (COL, RXD, CRS, RXC, SEL, LBK, TXD, TXC and TXE)						
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IN}	Input Leakage	V_{IN} = V_{CC} or GND	−1.0		1.0	μA
V_{OH}	Output High Voltage	(TTL) I_{OH} = 2.0 mA (CMOS) I_{OH} = 20 μA	3.5 V_{CC} − 0.1			V V
V_{OL}	Output Low Voltage	(TTL) I_{OL} = 2.0 mA (CMOS) I_{OL} = 20 μA			0.4 0.1	V V
I_{CCO}	Operating V_{CC} Supply Current (Note 1)	10 Mbit/sec			70	mA
I_{CCS}	Stand By V_{CC} Supply Current (Note 2)	10 Mbit/sec			65	mA
Differential Pins (TX±, RX±, and CD±)						
V_{OD}	Diff. Output Voltage (TX±)	78Ω Termination, and 270Ω from each to GND *(Figure 4)*	±550		±1200	mV
V_{OB}*	Diff. Output Voltage Imbalance (TX±)	78Ω Termination, and 270Ω from each to GND *(Figure 4)*		40		mV
V_U*	Undershoot Voltage (TX±)	78Ω Termination, and 270Ω from each to GND *(Figure 4)*		100		mV
V_{DS}	Diff. Squelch Threshold (RX± and CD±)		−175		−300	mV
V_{CM}	Diff. Input Common Mode Voltage (RX± and CD±) (Note 3)		0		5.5	V
Oscillator Pins (X1 and X2)						
V_{IH}	X1 Input High Voltage	X1 is connected to an oscillator, and X2 is grounded	2.0			V
V_{IL}	X1 Input Low Voltage	X1 is connected to an oscillator, and X2 is grounded			0.8	V
I_{OSC}	X1 Input Current	X1 = V_{CC} or GND X2 = GND	−2		+2	mA

Note 1: This measurement was made while the DP83910A was undergoing transmission, reception, and collision detection. Also, this value was not measured instantaneously, but averaged over a span of several milliseconds. (V_{IN} = 2.4V or 0.4V and I_o = 0 mA).

Note 2: This measurement was made while the DP83910A was sitting idle with TXE low. Also, this value was not measured instantaneously, but averaged over a span of several milliseconds. (V_{IN} = 2.4V or 0.4V and I_o = 0 mA).

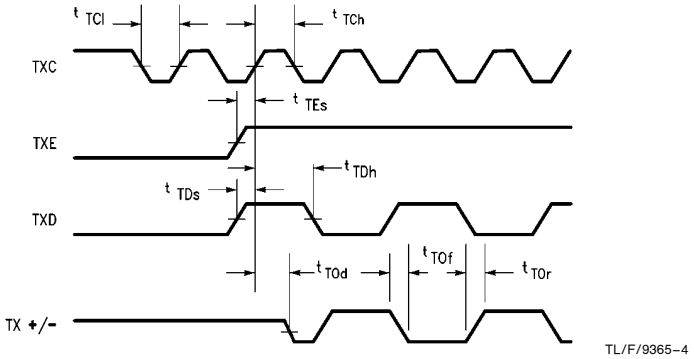
Note 3: This parameter is guaranteed by design and is not tested.

9.0 Switching Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

Oscillator Specification

Symbol	Parameter	Min	Max	Units
t_{XTH}	X1 to Transmit Clock High	5	30	ns
t_{XTL}	X1 to Transmit Clock Low	5	30	ns

Transmit Timing (Start of Packet)



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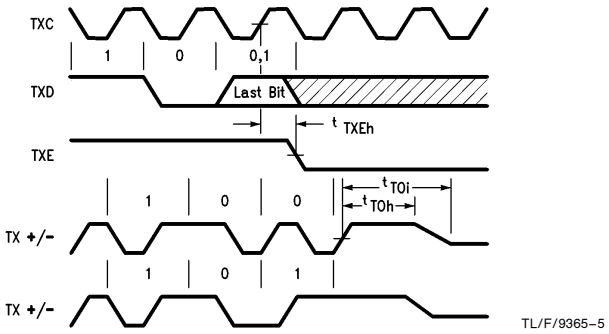
Transmit Specifications (Start of Packet)

Symbol	Parameter	Min	Max	Units
t_{TCh}	Transmit Clock High Time (Note 1)	40	60	ns
t_{TCl}	Transmit Clock Low Time (Note 1)	40	60	ns
t_{TCc}*	Transmit Clock Cycle Time (Note 1)	99.99	100.01	ns
t_{TCr}*	Transmit Clock Rise Time (20% to 80%) ($C_L = 30$ pF)		8	ns
t_{TCf}*	Transmit Clock Fall Time (80% to 20%) ($C_L = 30$ pF)		8	ns
t_{TEs}	Transmit Enable Setup Time to Rising Edge of TXC (Note 1)	20		ns
t_{TDs}	Transmit Data Setup Time from Rising Edge of TXC (Note 1)	20		ns
t_{TDh}	Transmit Data Hold Time from Rising Edge of TXC	0		ns
t_{TOd}	Transmit Output Delay from Rising Edge of TXC (Note 1)		65	ns
t_{TOf}*	Transmit Output Fall Time (80% to 20%)		7	ns
t_{TOr}*	Transmit Output Rise Time (20% to 80%)		7	ns
t_{TOj}*	Transmit Output Jitter	0.5 Typical		ns

Note 1: This parameter is measured using the fifty percent point of each clock edge.

9.0 Switching Characteristics (Continued)

Transmit Timing (End of Packet)



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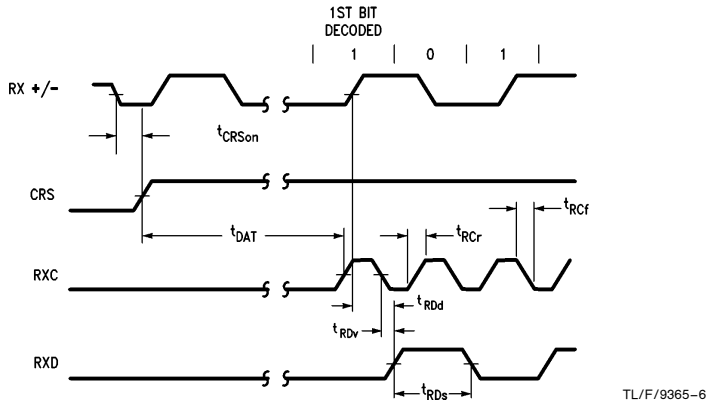
Transmit Specifications (End of Packet)

Symbol	Parameter	Min	Max	Units
t_{TXEh}	Transmit Enable Hold Time from Rising Edge of TXC	0		ns
t_{TOh}	Transmit Output High before Idle (Half Step)	200		ns
t_{TOi}*	Transmit Output Idle Time (Half Step)		8000	ns

Receive Timing (Start of Packet)



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Receiver Specifications (Start of Packet)

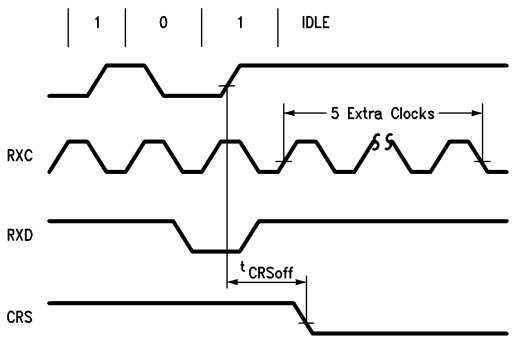
Symbol	Parameter	Min	Max	Units
t_{RCd}	Receive Clock Duty Cycle (Note 1)	40	60	%
t_{RCr}*	Receive Clock Rise Time (20% to 80%, C_{TL} = 30 pF)		7	ns
t_{RCf}*	Receive Clock Fall Time (80% to 20%, C_{TL} = 30 pF)		7	ns
t_{CRSon}	Carrier Sense Turn On Delay		70	ns
t_{DAT}	Decoder Acquisition Time		700	ns
t_{RDd}	Receive Data Output Delay		150	ns
t_{RDs}	Receive Data Output Stable after Going Valid	90		ns
t_{Dtor}	Differential Inputs Turn-On Pulse (Note 2)	30		ns
t_{RDV}	Receive Data Output Valid from Falling Edge of RXC		10	ns

Note 1: This parameter is measured using the fifty percent point of each clock edge.

Note 2: This parameter was characterized with a differential input of −375 mV on the receive pair inputs.

9.0 Switching Characteristics (Continued)

Receive Timing (End of Packet)



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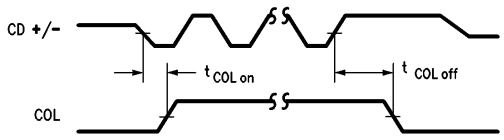
Receiver Specifications (End of Packet)

Symbol	Parameter	Min	Max	Units
t_{CRSoff}	Carrier Sense Turn Off Delay (Note 1)		155	ns
t_{RXCh}	Minimum Number of RXCs after CRS Low (Note 2)	5		Bit Times

Note 1: When CRS goes low, it will go low a minimum of 2 receive clocks.

Note 2: The DP8390 Network Interface Controller (NIC) requires a minimum of 5 receive clocks after CRS goes low to function properly.

Collision Timing



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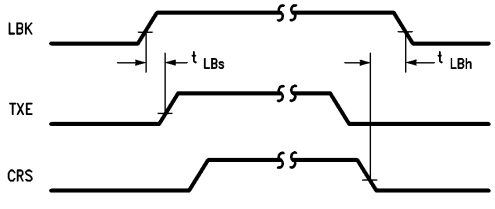
Collision Specifications

Symbol	Parameter	Min	Max	Units
t_{COLon}	Collision Turn On Delay		60	ns
t_{COLoff}	Collision Turn Off Delay		350	ns
t_{Dtoc}	Differential Inputs Turn-On Pulse (Squelch, Note 1)	30		ns

Note 1: This parameter was characterized with a differential input of −375 mV on the collision input pair.

9.0 Switching Characteristics (Continued)

Loopback Timing



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Loopback Specifications

Symbol	Parameter	Min	Max	Units
t_{LBs}	Loopback Setup Time (Note 1)	50		ns
t_{LBh}	Loopback Hold Time (Note 1)	1000		ns

Note 1: This parameter is guaranteed by design and is not tested.

AC Timing Test Conditions

All specifications are valid only if the mandatory isolation is employed and all differential signals are taken to be at the AUI side of the pulse tranformer.

Input Pulse Levels (TTL/CMOS)	GND to 3.0V
Input Rise and Fall Times (TTL/CMOS)	5 ns
Input and Output Reference Levels (TTL/CMOS)	1.3V
Input Pulse Levels (Diff.)	−350 to −1315 mV
Input and Output Reference Levels (Diff.)	50% Point of the Differential

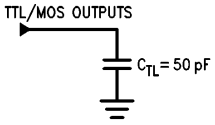

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FIGURE 3

Capacitance $T_A = 25°C, f = 1$ MHz

Symbol	Parameter	Typ	Units
C_{IN}	Input Capacitance	7	pF
C_{OUT}	Output Capacitance	7	pF

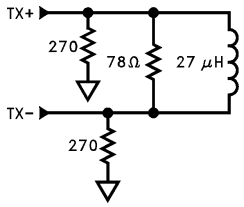

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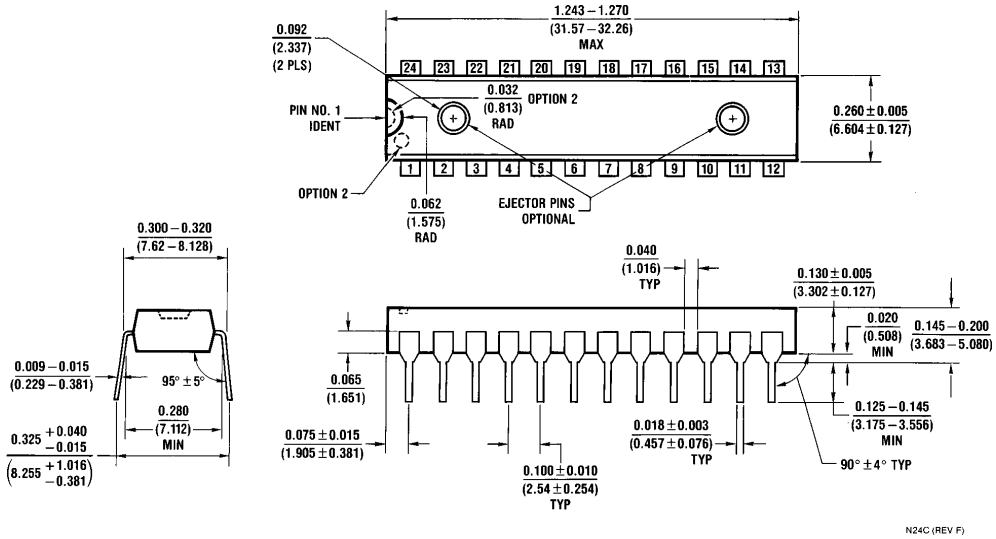
FIGURE 4

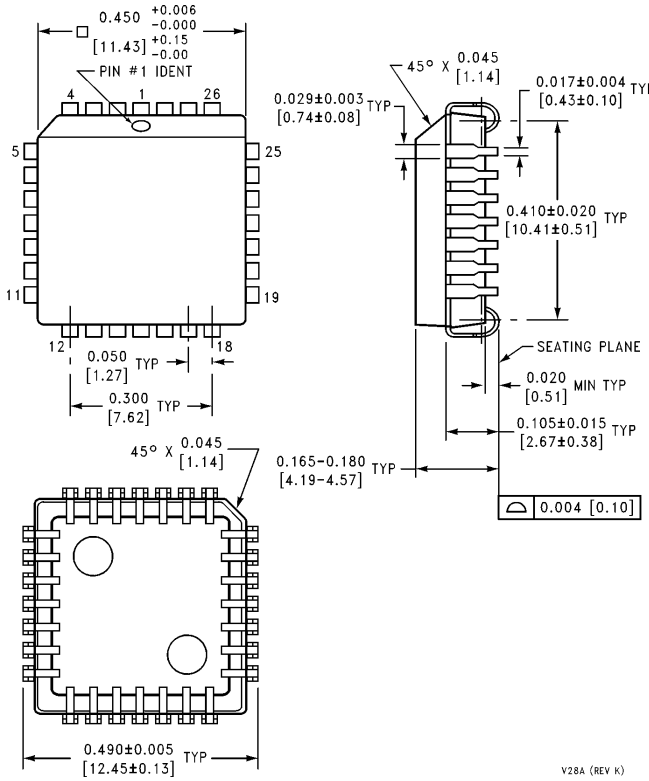
Note: In the above diagram, the TX+ and TX− signals are taken from the AUI side of the isolation (pulse transformer). The pulse transformer used for all testing is the Pulse Engineering PE64103.

Physical Dimensions inches (millimeters)



Molded Dual-In-Line Package (N)
Order Number DP83910AN
NS Package Number N24C

Physical Dimensions inches (millimeters) (Continued)



Plastic Chip Carrier (V)
Order Number DP83910AV
NS Package Number V28A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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