National Semiconductor

May 1999

DS75160A/DS75161A IEEE-488 GPIB Transceivers

General Description

This family of high-speed-Schottky 8-channel bi-directional transceivers is designed to interface TTL/MOS logic to the IEEE Standard 488-1978 General Purpose Interface Bus (GPIB). PNP inputs are used at all driver inputs for minimum loading, and hysteresis is provided at all receiver inputs for added noise margin. The IEEE-488 required bus termination is provided internally with an active turn-off feature which disconnects the termination from the bus when V_{CC} is removed.

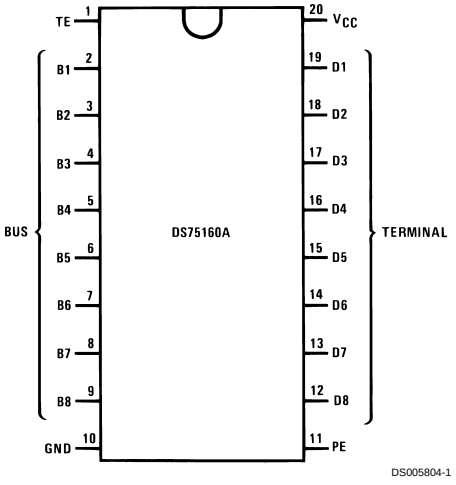
The General Purpose Interface Bus is comprised of 16 signal lines — 8 for data and 8 for interface management. The data lines are always implemented with DS75160A, and the management lines are either implemented with DS75161A in a single-controller system.

Features

- 8-channel bi-directional non-inverting transceivers
- Bi-directional control implemented with TRI-STATE® output design
- Meets IEEE Standard 488-1978
- High-speed Schottky design
- Low power consumption
- High impedance PNP inputs (drivers)
- 500 mV (typ) input hysteresis (receivers)
- On-chip bus terminators
- No bus loading when V_{CC} is removed
- Pin selectable open collector mode on DS75160A driver outputs
- Accommodates multi-controller systems

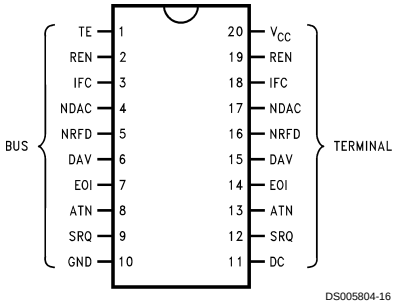
Connection Diagrams

Dual-In-Line Package



Top View
Order Number DS75160AN or DS75160AWM
See NS Package Number M20B or N20A

Dual-In-Line Package



Order Number DS75161AN or DS75161AWM
See NS Package Number M20B or N20B

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Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature (Soldering, 4 sec.)	260˚C
Maximum Power Dissipation (Note 1) at 25˚C	
Molded Package	1897 mW

	Min	Max	Units
V_{CC}, Supply Voltage	4.75	5.25	V
T_A, Ambient Temperature	0	70	˚C
I_{OL}, Output Low Current			
Bus		48	mA
Terminal		16	mA

Note 1: Derate molded package 15.2 mW/˚C above 25˚C.

Electrical Characteristics (Notes 3, 4)

Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage				2			V
V_{IL}	Low-Level Input Voltage						0.8	V
V_{IK}	Input Clamp Voltage		I_I = −18 mA			−0.8	−1.5	V
V_{HYS}	Input Hysteresis	Bus			400	500		mV
V_{OH}	High-Level Output Voltage	Terminal	I_{OH} = −800 µA		2.7	3.5		V
		Bus (Note 4)	I_{OH} = −5.2 mA		2.5	3.4		
V_{OL}	Low-Level Output Voltage	Terminal	I_{OL} = 16 mA			0.3	0.5	V
		Bus	I_{OH} = 48 mA			0.4	0.5	
I_{IH}	High-Level Input Current	Terminal and TE, PE, DC, SC Inputs	V_I = 5.5V			0.2	100	µA
			V_I = 2.7V			0.1	20	
I_{IL}	Low-Level Input Current		V_I = 0.5V			−10	−100	µA
V_{BIAS}	Terminator Bias Voltage at Bus Port	Bus	Driver Disabled	$I_{I(bus)}$ = 0 (No Load)	2.5	3.0	3.7	V
I_{LOAD}	Terminator Bus Loading Current		Driver Disabled	$V_{I(bus)}$ = −1.5V to 0.4V	−1.3			mA
				$V_{I(bus)}$ = 0.4V to 2.5V	0		−3.2	
				$V_{I(bus)}$ = 2.5V to 3.7V			2.5 −3.2	
				$V_{I(bus)}$ = 3.7V to 5V	0		2.5	
				$V_{I(bus)}$ = 5V to 5.5V	0.7		2.5	
			V_{CC} = 0V, $V_{I(bus)}$ = 0V to 2.5V				40	µA
I_{OS}	Short-Circuit Output Current	Terminal	V_I = 2V, V_O = 0V (Note 5)		−15	−35	−75	mA
		Bus (Note 6)			−35	−75	−150	
I_{CC}	Supply Current	DS75160A	Transmit, TE = 2V, PE = 2V, V_I = 0.8V			85	125	mA
			Receive, TE = 0.8V, PE = 2V, V_I = 0.8V			70	100	
		DS75161A	TE = 0.8V, DC = 0.8V, V_I = 0.8V			84	125	
C_{IN}	Bus-Port Capacitance	Bus	V_{CC} = 5V or 0V, V_I = 0V to 2V, f = 1 MHz			20	30	pF

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 3: Unless otherwise specified, min/max limits apply across the 0˚C to +70˚C temperature range and the 4.75V to 5.25V power supply range. All typical values are for T_A = 25˚C and V_{CC} = 5.0V.

Note 4: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 5: Only one output at a time should be shorted.

Note 6: This characteristic does not apply to outputs on DS75161A that are open collector.

Switching Characteristics (Note 7)

V_{CC} = 5.0V ±5%, T_A = 0˚C to 70˚C

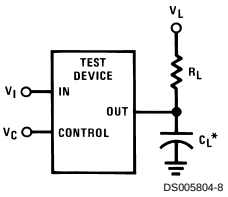
Symbol	Parameter	From	To	Conditions	DS75160A			DS75161A			DS75162A			Units
					Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	Terminal	Bus	V_L = 2.3V, R_L = 38.3Ω, C_L = 30 pF, *Figure 1*		10	20		10	20		10	20	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output					14	20		14	20		14	20	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Bus	Terminal	V_L = 5.0V, R_L = 240Ω, C_L = 30 pF, *Figure 2*		14	20		14	20		14	20	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output					10	20		10	20		10	20	ns
t_{PZH}	Output Enable Time to High Level	TE, DC, or SC (Note 8) (Note 9)	Bus	V_I = 3.0V, V_L = 0V, R_L = 480Ω, C_L = 15 pF, *Figure 1*		19	32		23	40		23	40	ns
t_{PHZ}	Output Disable Time From High Level					15	22		15	25		15	25	ns
t_{PZL}	Output Enable Time to Low Level			V_I = 0V, V_L = 2.3V, R_L = 38.3Ω, C_L = 15 pF, *Figure 1*		24	35		28	48		28	48	ns
t_{PLZ}	Output Disable Time From Low Level					17	25		17	27		17	27	ns
t_{PZH}	Output Enable Time to High Level	TE, DC, or SC (Note 8) (Note 9)	Terminal	V_I = 3.0V, V_L = 0V, R_L = 3 kΩ, C_L = 15 pF, *Figure 1*		17	33		18	40		18	40	ns
t_{PHZ}	Output Disable Time From High Level					15	25		22	33		22	33	ns
t_{PZL}	Output Enable Time to Low Level			V_I = 0V, V_L = 5V, R_L = 280Ω, C_L = 15 pF, *Figure 1*		25	39		28	52		28	52	ns
t_{PLZ}	Output Disable Time From Low Level					15	27		20	35		20	35	ns
t_{PZH}	Output Pull-Up Enable Time (DS75160A Only)	PE (Note 8)	Bus	V_I = 3V, V_L = 0V, R_L = 480Ω, C_L = 15 pF, *Figure 1*		10	17		NA			NA		ns
t_{PHZ}	Output Pull-Up Disable Time (DS75160A Only)					10	15		NA			NA		ns

Note 7: Typical values are for V_{CC} = 5.0V and T_A = 25˚C and are meant for reference only.

Note 8: Refer to Functional Truth Tables for control input definition.

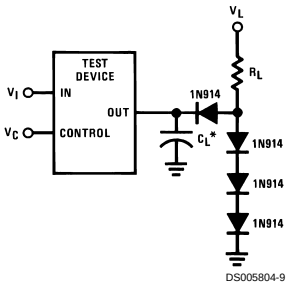
Note 9: Test configuration should be connected to only one transceiver at a time due to the high current stress caused by the V_I voltage source when the output connected to that input becomes active.

Switching Load Configurations



V_C logic high = 3.0V
V_C logic low = 0V
*C_L includes jig and probe capacitance

FIGURE 1.

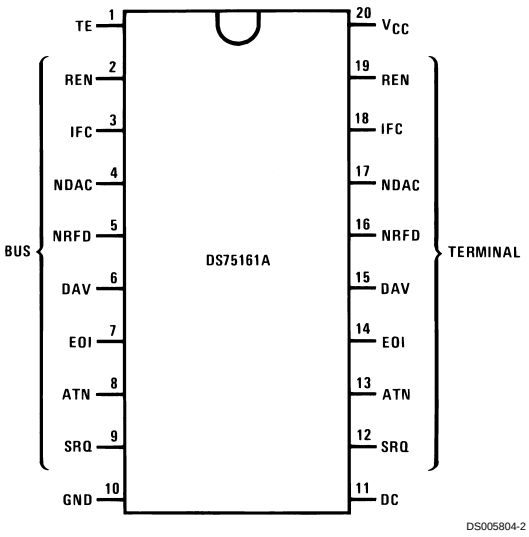


V_C logic high = 3.0V
V_C logic low = 0V
*C_L includes jig and probe capacitance

FIGURE 2.

Connection Diagrams

Dual-In-Line Package



Top View

Functional Description

DS75160A

This device is an 8-channel bi-directional transceiver with one common direction control input, denoted TE. When used to implement the IEEE-488 bus, this device is connected to the eight data bus lines, designated DIO_1–DIO_8. The port connections to the bus lines have internal terminators, in accordance with the IEEE-488 Standard, that are deactivated when the device is powered down. This feature guarantees no bus loading when V_{CC} = 0V. The bus port outputs also have a control mode that either enables or disables the active upper stage of the totem-pole configuration. When this control input, denoted PE, is in the high state, the bus outputs operate in the high-speed totem-pole mode. When PE is in the low state, the bus outputs operate as open collector outputs which are necessary for parallel polling.

DS75161A

This device is also an 8-channel bi-directional transceiver which is specifically configured to implement the eight management signal lines of the IEEE-488 bus. This device, paired with the DS75160A, forms the complete 16-line interface between the IEEE-488 bus and a single controller instrumentation system. In compliance with the system organization of the management signal lines, the SRQ, NDAC, and NRFD bus port outputs are open collector. In contrast to the DS75160A, these open collector outputs are a fixed configuration. The direction control is divided into three groups. The DAV, NDAC, and NRFD transceiver directions are controlled by the TE input. The ATN, SRQ, REN, and IFC transceiver directions are controlled by the DC input. The EOI transceiver direction is a function of both the TE and DC inputs, as well as the logic level present on the ATN channel. The port connections to the bus lines have internal terminators identical to the DS75160A.

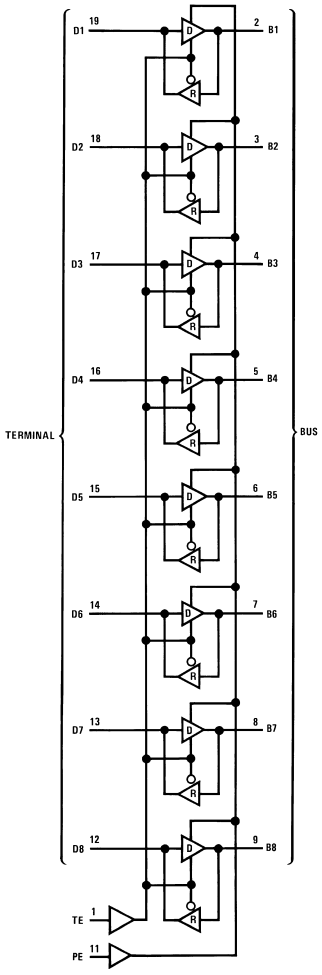
Functional Description (Continued)

Table of Signal Line Abbreviations

Signal Line Classification	Mnemonic	Definition	Device
Control Signals	DC	Direction Control	DS75161A
	PE	Pull-Up Enable	DS75160A
	TE	Talk Enable	All
	SC	System Controller	
Data I/O Ports	B1–B8	Bus Side of Device	DS75160A
	D1–D8	Terminal Side of Device	
Management Signals	ATN	Attention	DS75161A
	DAV	Data Valid	
	EOI	End or Identify	
	IFC	Interface Clear	
	NDAC	Not Data Accepted	
	NRFD	Not Ready for Data	
	REN	Remote Enable	
	SRQ	Service Request	

Logic Diagrams

DS75160A



Note 1: Denotes driver

Note 2: Denotes receiver

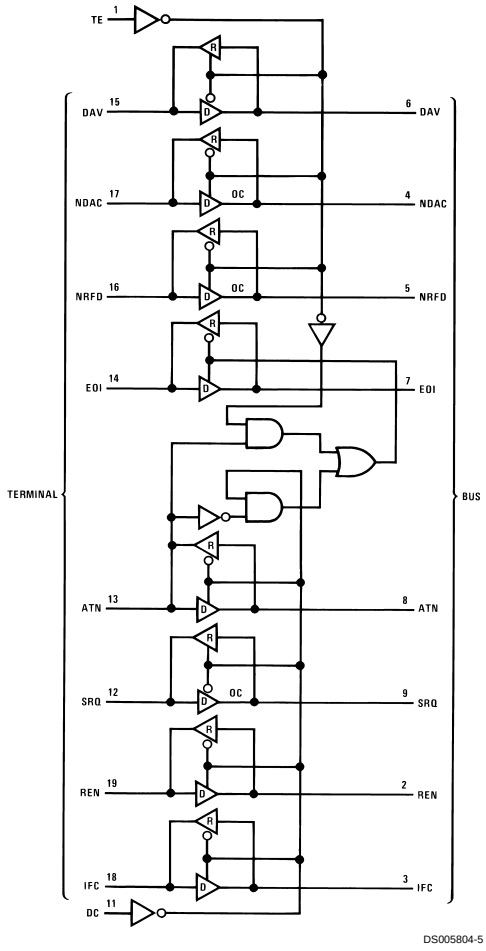
Note 3: Driver and receiver outputs are totem-pole configurations

Note 4: The driver outputs of DS75160A can have their active pull-ups disabled by switching the PE input (pin 11) to the logic low state. This mode configures the outputs as open collector.

DS005804-4

Logic Diagrams (Continued)

DS75161A



DS005804-5

Note 1: D — Denotes driver

Note 2: R — Denotes receiver

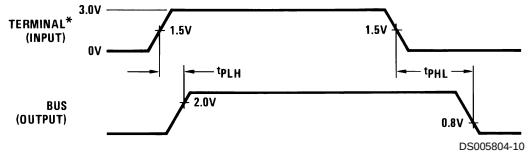
Note 3: Symbol "OC" specifies open collector output

Note 4: Driver and receiver outputs that are not specified "OC" are totem-pole configurations

DS005804-7

Switching Waveforms

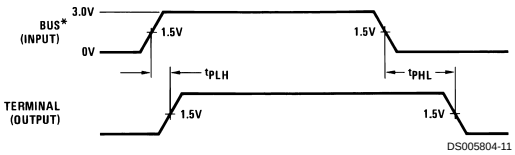
Transmit Propagation Delays



DS005804-10

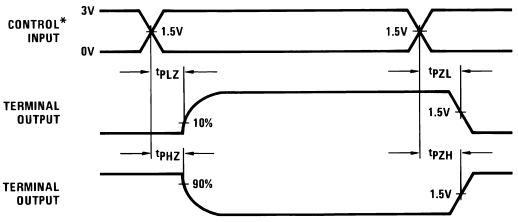
Switching Waveforms (Continued)

Receive Propagation Delays



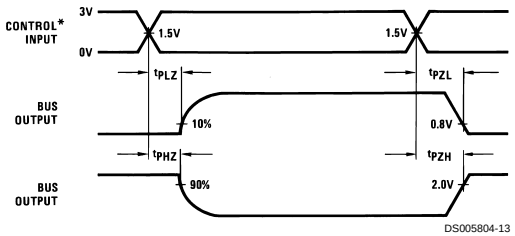
DS005804-11

Terminal Enable/Disable Times



DS005804-12

Bus Enable/Disable Times

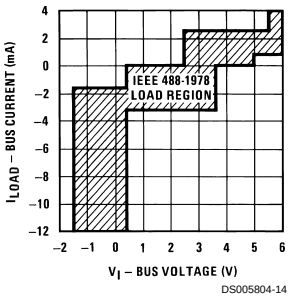


DS005804-13

*Input signal: f = 1.0 MHz, 50% duty cycle, $t_r = t_f \leq 5$ ns

Performance Characteristics

Bus Port Load Characteristics



DS005804-14

Refer to Electrical Characteristics table

Functional Truth Tables

DS75160A

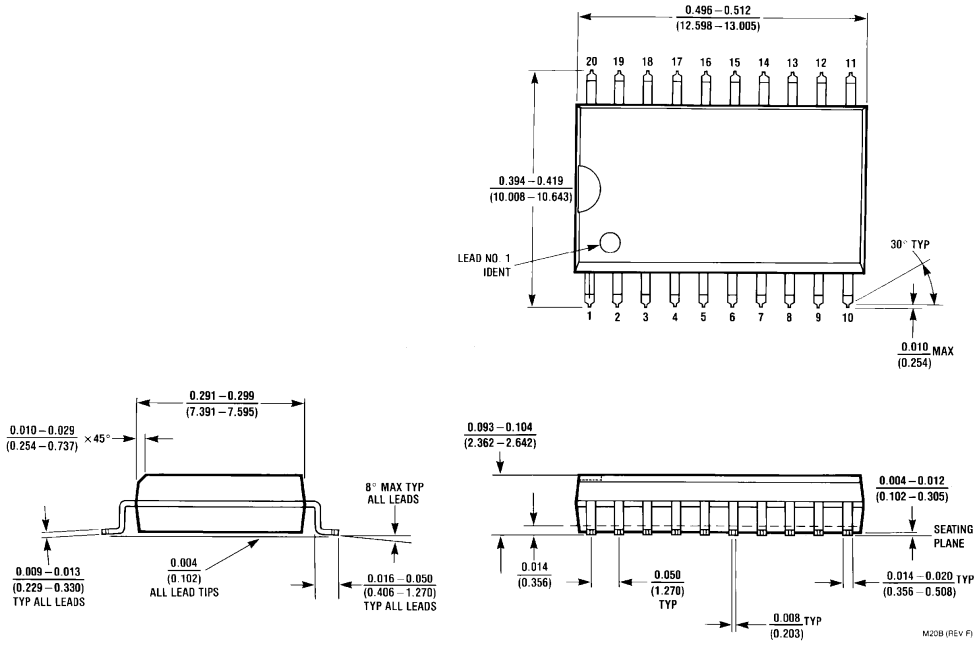
Control Input Level		Data Transceivers	
TE	**PE**	**Direction**	**Bus Port Configuration**
H	H	T	Totem-Pole Output
H	L	T	Open Collector Output
L	X	R	Input

DS75161A

Control Input Level			Transceiver Signal Direction							
TE	**DC**	**ATN***		**EOI**	**REN**	**IFC**	**SRQ**	**NRFD**	**NDAC**	**DAV**
H	H		R		R	R	T	R	R	T
H	L		T		T	T	R	R	R	T
L	H		R		R	R	T	T	T	R
L	L		T		T	T	R	T	T	R
H	X	H		T						
L	X	H		R						
X	H	L		R						
X	L	L		T						

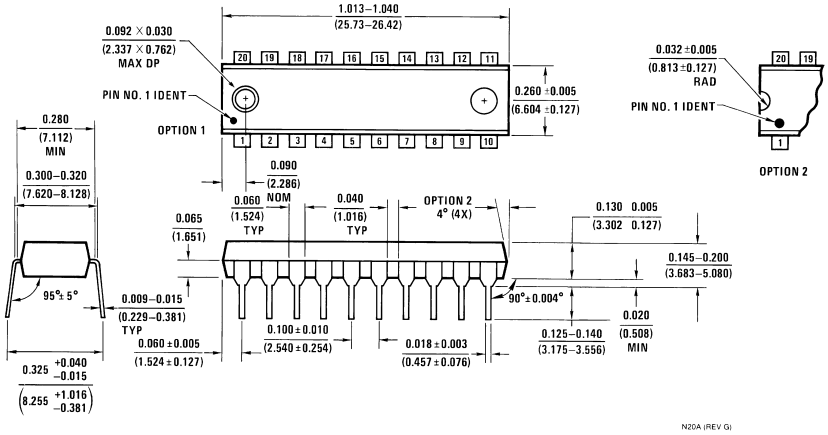
H = High level input
L = Low level input
X = Don't care
T = Transmit, i.e., signal outputted to bus
R = Receive, i.e., signal outputted to terminal
*The ATN signal level is sensed for internal multiplex control of EOI transmission direction logic.

Physical Dimensions inches (millimeters) unless otherwise noted



Order Number DS75160AWM
NS Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N)
Order Number DS75160AN or DS75161AN
NS Package Number N20A

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