May 1999

National Semiconductor

# DS7831/DS8832
# Dual TRI-STATE® Line Driver

## General Description

Through simple logic control, the DS7831/DS8832 can be used as either a quad single-ended line driver or a dual differential line driver. They are specifically designed for party line (bus-organized) systems. The DS8832 does not have the $V_{CC}$ clamp diodes found on the DS7831.

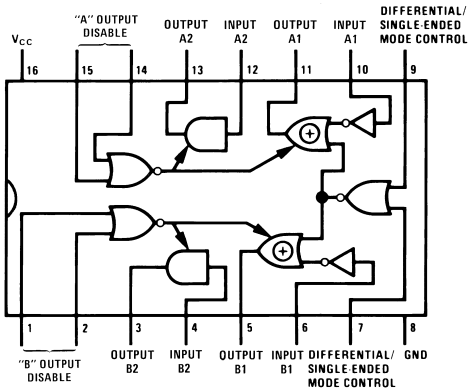
The DS7831 is specified for operation over the −55˚C to +125˚C military temperature range. The DS8832 is specified for operation over the 0˚C to +70˚C temperature range.

## Features

- Series 54/74 compatible
- 17 ns propagation delay
- Very low output impedance — high drive capability
- 40 mA sink and source currents
- Gating control to allow either single-ended or differential operation
- High impedance output state which allows many outputs to be connected to a common bus line

## Connection and Logic Diagram

**Dual-In-Line Package**




**Top View**
**Order Number DS8832J or DS8832N**
**See NS Package Number J16A or N16A**
**For Complete Military 883 Specificatons,**
**See RETS Data Sheet.**
**Order Number DS7831J/883, DS7831W/883,**
**See NS Package Number J16A or W16A**

TRI-STATE® is a registered trademark of National Semiconductor Corp.

© 1999 National Semiconductor Corporation 

## Truth Table

(Shown for A Channels Only)

| "A" Output Disable | | Differential/ Single-Ended Mode Control | | Input A1 | Output A1 | Input A2 | Output A2 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Logical "1" or Logical "0" | Same as Input A1 | Logical "1" or Logical "0" | Same as Input A2 |
| 0 | 0 | X<br>1 | 1<br>X | Logical "1" or Logical "0" | Opposite of Input A1 | Logical "1" or Logical "0" | Same as Input A2 |
| 1<br>X | X<br>1 | X | X | X | High Impedance State | X | High Impedance State |

X = Don't Care

## Absolute Maximum Ratings (Note 2)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | 7V |
| Input Voltage | 5.5V |
| Output Voltage | 5.5V |
| Storage Temperature Range | −65˚C to +150˚C |
| Lead Temperature (Soldering, 4 sec.) | 260˚C |
| Maximum Power Dissipation (Note 1) at 25˚C | |
| Cavity Package | 1433 mW |
| Molded Package | 1362 mW |

## Operating Conditions

| | Min | Max | Units |
|---|---|---|---|
| Supply Voltage ($V_{CC}$) | | | |
| DS7831 | 4.5 | 5.5 | V |
| DS8831/DS8832 | 4.75 | 5.25 | V |
| Temperature ($T_A$) | | | |
| DS7831 | −55 | +125 | ˚C |
| DS8832 | 0 | +70 | ˚C |

**Note 1:** Derate cavity package 9.6 mW/˚C above 25˚C; derate molded package 10.9 mW/˚C above 25˚C.

## Electrical Characteristics (Notes 3, 4)

| Symbol | Parameter | Conditions | | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Logical “1” Input Voltage | $V_{CC}$ = Min | | | 2.0 | | | V |
| $V_{IL}$ | Logical “0” Input Voltage | $V_{CC}$ = Min | | | | | 0.8 | V |
| $V_{OH}$ | Logical “1” Output Voltage | DS7831 | $V_{CC}$ = Min | $I_O$ = −40 mA | 1.8 | 2.3 | | V |
| | | | | $I_O$ = −2 mA | 2.4 | 2.7 | | V |
| | | DS8832 | | $I_O$ = −40 mA | 1.8 | 2.5 | | V |
| | | | | $I_O$ = −5.2 mA | 2.4 | 2.9 | | V |
| $V_{OL}$ | Logical “0” Output Voltage | DS7831 | $V_{CC}$ = Min | $I_O$ = 40 mA | | 0.29 | 0.50 | V |
| | | | | $I_O$ = 32 mA | | | 0.40 | V |
| | | DS8832 | | $I_O$ = 40 mA | | 0.29 | 0.50 | V |
| | | | | $I_O$ = 32 mA | | | 0.40 | V |
| $I_{IH}$ | Logical “1” Input Current | $V_{CC}$ = Max | DS7831, $V_{IN}$ = 5.5V | | | | 1 | mA |
| | | | DS8832, $V_{IN}$ = 2.4V | | | | 40 | µA |
| $I_{IL}$ | Logical “0” Input Current | $V_{CC}$ = Max, $V_{IN}$ = 0.4V | | | | −1.0 | −1.6 | mA |
| $I_{OD}$ | Output Disable Current | $V_{CC}$ = Max, $V_O$ = 2.4V or 0.4V | | | −40 | | 40 | µA |
| $I_{SC}$ | Output Short Circuit Current | $V_{CC}$ = Max, (Note 5) | | | −40 | −100 | −120 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max in TRI-STATE | | | | 65 | 90 | mA |
| $V_{CLI}$ | Input Diode Clamp Voltage | $V_{CC}$ = 5.0V, $T_A$ = 25˚C, $I_{IN}$ = −12 mA | | | | | −1.5 | V |
| $V_{CLO}$ | Output Diode Clamp Voltage | $V_{CC}$ = 5.0V, $T_A$ = 25˚C | $I_{OUT}$ = −12 mA | DS7831 DS8832 | | | −1.5 | V |
| | | | $I_{OUT}$ = 12 mA | DS7831 | | | $V_{CC}$ + 1.5 | V |

## Switching Characteristics

$T_A$ = 25˚C, $V_{CC}$ = 5V, unless otherwise noted

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{pd0}$ | Propagation Delay to a Logical “0” from Inputs A1, A2, B1, B2 Differential Single-ended Mode Control to Outputs | (See *Figure 4* and *Figure 5* ) | | 13 | 25 | ns |
| $t_{pd1}$ | Propagation Delay to a Logical “1” from Inputs A1, A2, B1, B2 Differential Single-ended Mode Control to Outputs | | | 13 | 25 | ns |
| $t_{1H}$ | Delay from Disable Inputs to High Impedance State (from Logical “1” Level) | | | 6 | 12 | ns |
| $t_{0H}$ | Delay from Disable Inputs to High Impedance State (from Logical “0” Level) | | | 14 | 22 | ns |

## Switching Characteristics (Continued)

$T_A$ = 25˚C, $V_{CC}$ = 5V, unless otherwise noted

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{H1}$ | Propagation Delay from Disable Inputs to Logical "1" Level (from High Impedance State) | | | 14 | 22 | ns |
| $t_{H0}$ | Propagation Delay from Disable Inputs to Logical "0" Level (from High Impedance State) | | | 18 | 27 | ns |

**Note 2:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 3:** Unless otherwise specified min/max limits apply across the −55˚C to +125˚C temperature range for the DS7831 and across the 0˚C to +70˚C range for the DS8832. All typical values are for $T_A$ = 25˚C and $V_{CC}$ = 5V.

**Note 4:** All currents into device pins shown as positive, out of device pins as negative, all voltage referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

**Note 5:** Applies for $T_A$ = 125˚C only. Only one output should be shorted at a time.

## Mode of Operation

To operate as a quad single-ended line driver apply logical "0"s to the output disable pins (to keep the outputs in the normal low impedance mode) and apply logical "0"s to both Differential/Single-ended Mode Control inputs. All four channels will then operate independently and no signal inversion will occur between inputs and outputs.

To operate as a dual differential line driver apply logical "0"s to the Output Disable pins and apply at least one logical "1" to the Differential/Single-ended Mode Control inputs.

The inputs to the A channels should be connected together and the inputs to the B channels should be connected together.

In this mode the signals applied to the resulting inputs will pass non-inverted on the $A_2$ and $B_2$ outputs and inverted on the $A_1$ and $B_1$ outputs.

When operating in a bus-organized system with outputs tied directly to outputs of other DS7831, DS8832's (*Figure 1*), all devices except one must be placed in the "high impedance" state. This is accomplished by ensuring that a logical "1" is applied to at least one of the Output Disable pins of each device which is to be in the "high impedance" state. A NOR gate was purposely chosen for this function since it is possible with only two DM5442/DM7442, BCD-to-decimal decoders, to decode as many as 100 DS7831, DS8832's (*Figure 2*).

The unique device whose Disable inputs receive two logical "0" levels assumes the normal low impedance output state, providing good capacitive drive capability and waveform integrity especially during the transition from the logical "0" to logical "1" state. The other outputs — in the high impedance state — take only a small amount of leakage current from the low impedance outputs. Since the logical "1" output current from the selected device is 100 times that of a conventional Series 54/74 device (40 mA vs. 400 µA), the output is easily able to supply that leakage current for several hundred other DS7831/DS8831's, DS7832/DS8832's and still have available drive for the bus line (*Figure 3*).

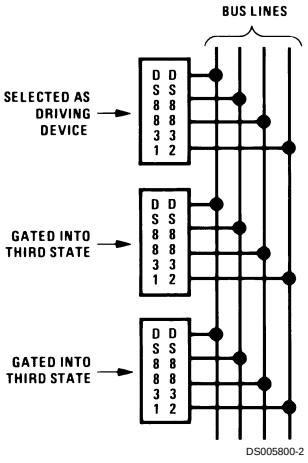



**FIGURE 1.**

## Mode of Operation (Continued)

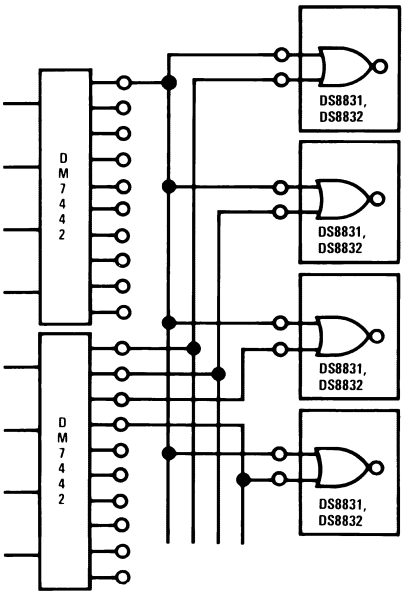



**FIGURE 2.**

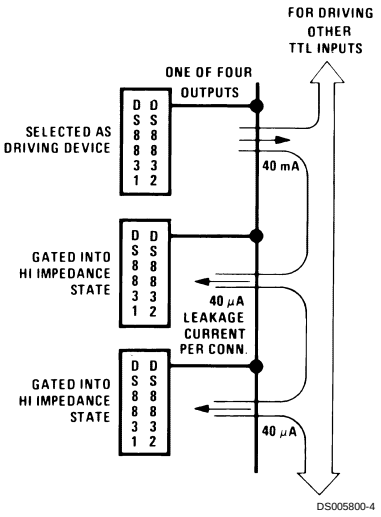
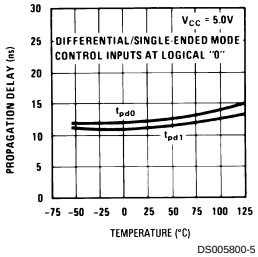



**FIGURE 3.**

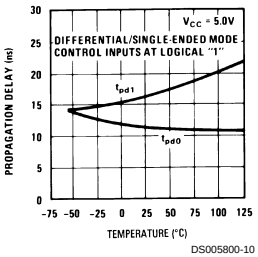
## Typical Performance Characteristics

**Propagation Delay from Input to Output (Channel 1)**



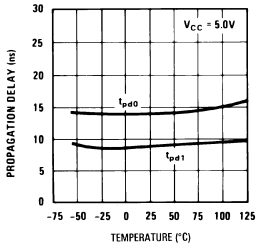

DS005800-5

**Propagation Delay from Input to Output (Channel 1)**



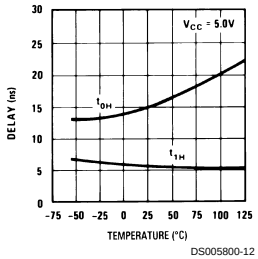

DS005800-10

**Propagation Delay from Input to Output (Channel 2)**



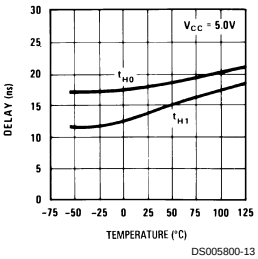

DS005800-11

**Delay from Disable to High Impedance State**



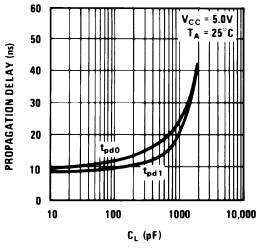

DS005800-12

**Delay from Disable to Low Impedance State**



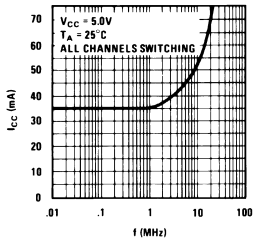

DS005800-13

**Propagation Delay vs Load Capacitance**



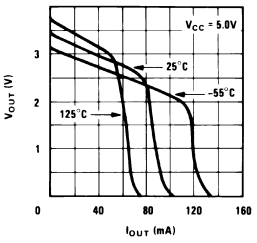

DS005800-14

**Total Supply Current vs Frequency**



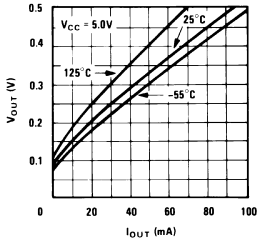

DS005800-15

**Logical "1" Output Voltage vs Source Current**



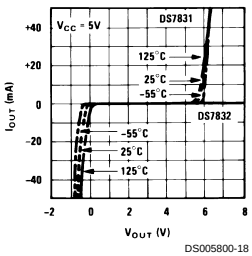

DS005800-16

**Logical "0" Output Voltage vs Sink Current**



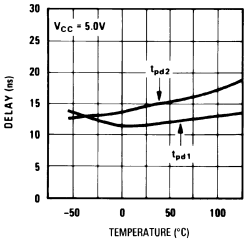

DS005800-17

**$I_{OUT}$ vs $V_{OUT}$ High Impedance Output State**



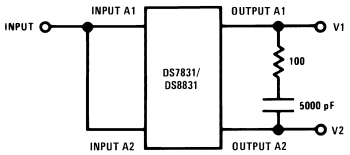

DS005800-18

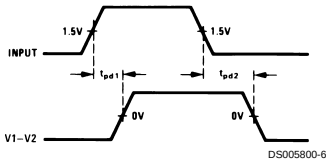
**Propagation Delay in Differential Mode**




DS005800-19

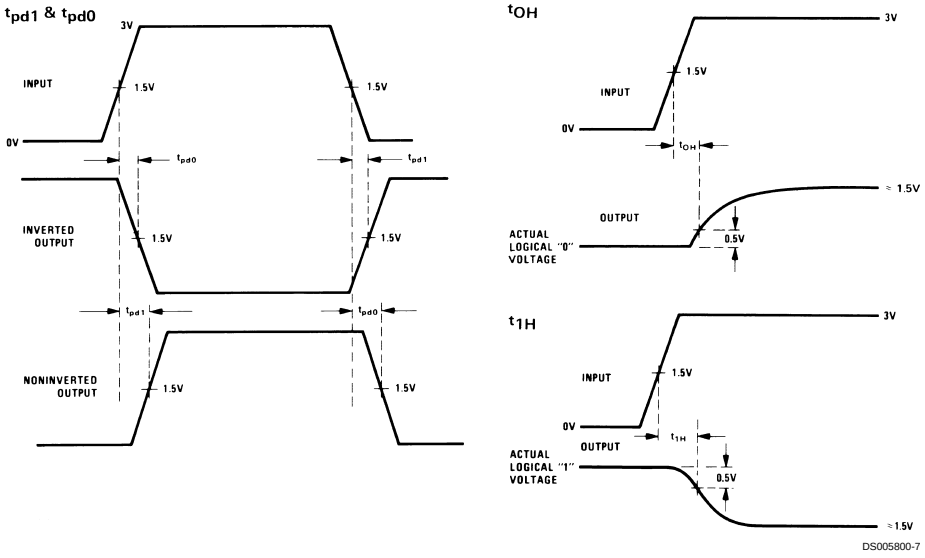
## Typical Performance Characteristics (Continued)




DS005800-6

## Switching Time Waveforms




DS005800-7

Input characteristic:
Amplitude = 3.0V
Frequency = 1.0 MHz, 50% duty cycle
$t_r = t_f \leq$ ns (10% to 90%)

## Switching Time Waveforms (Continued)

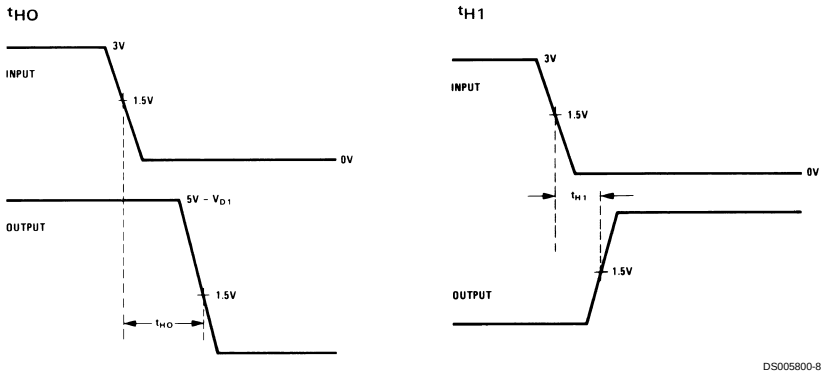
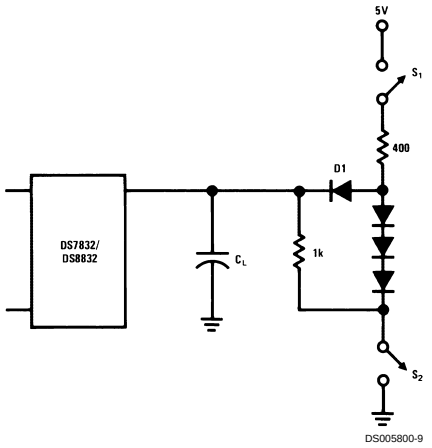



**FIGURE 4.**

## AC Load Circuit

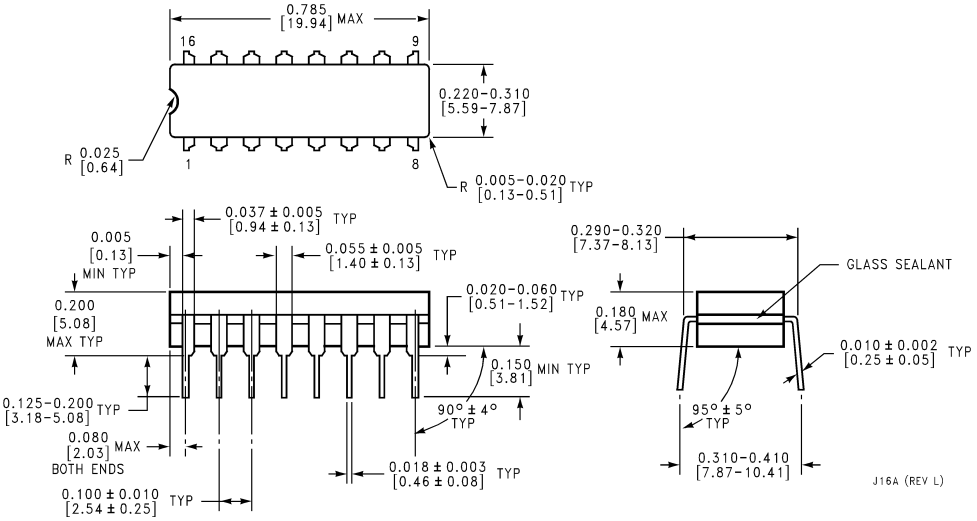



| Symbol | Switch S1 | Switch S2 | $C_L$ |
|---|---|---|---|
| $t_{pd1}$ | closed | closed | 50 pF |
| $t_{pd0}$ | closed | closed | 50 pF |
| $t_{0H}$ | closed | closed | *5 pF |
| $t_{1H}$ | closed | closed | *5 pF |
| $t_{H0}$ | closed | open | 50 pF |
| $t_{H1}$ | open | closed | 50 pF |

*Jig capacitance

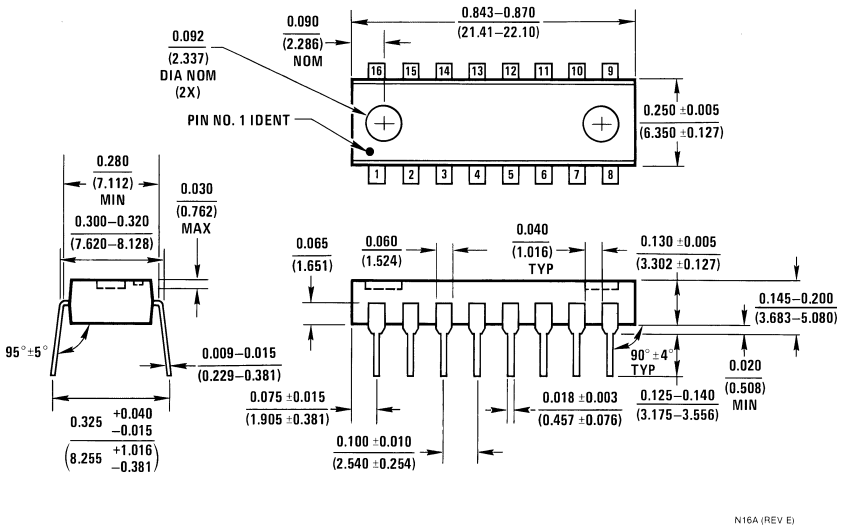
**FIGURE 5.**

## Physical Dimensions inches (millimeters) unless otherwise noted




**Ceramic Dual-In-Line Package (J)**
**Order Number DS7831J or DS8832J**
**NS Package Number J16A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**Molded Dual-In-Line Package (N)**
**Order Number DS8832N**
**NS Package Number N16A**

**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**National Semiconductor Corporation**
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

**National Semiconductor Europe**
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

**National Semiconductor Asia Pacific Customer Response Group**
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

**National Semiconductor Japan Ltd.**
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.