National Semiconductor

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DS90C383/DS90CF384
+3.3V Programmable LVDS Transmitter 24-Bit Flat Panel Display (FPD) Link—65 MHz, +3.3V LVDS Receiver 24-Bit Flat Panel Display (FPD) Link—65 MHz

General Description

The DS90C383 transmitter converts 28 bits of CMOS/TTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. The DS90CF384 receiver converts the LVDS data streams back into 28 bits of CMOS/TTL data. At a transmit clock frequency of 65 MHz, 24 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 455 Mbps per LVDS data channel. Using a 65 MHz clock, the data throughputs is 227 Mbytes/sec. The transmitter is offered with programmable edge data strobes for convenient interface with a variety of graphics controllers. The transmitter can be programmed for Rising edge strobe or Falling edge strobe through a dedicated pin. A Rising edge transmitter will inter-operate with a Falling edge receiver (DS90CF384) without any translation logic. The DS90CF384 is also offered in 64 ball, 0.8mm fine pitch ball grid array(FBGA) package which provides a 44 % reduction in PCB footprint (available Q3, 1999).

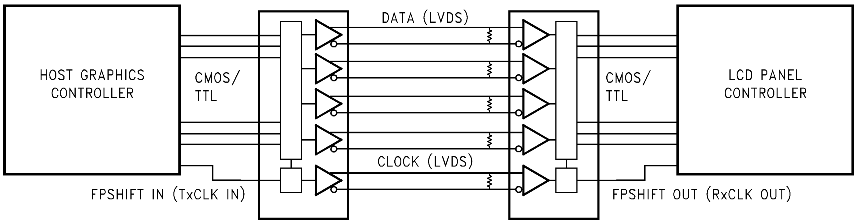
This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Features

- 20 to 65 MHz shift clock support
- Programmable transmitter (DS90C383) strobe select (Rising or Falling edge strobe)
- Single 3.3V supply
- Chipset (Tx + Rx) power consumption < 250 mW (typ)
- Power-down mode (< 0.5 mW total)
- Single pixel per clock XGA (1024x768) ready
- Supports VGA, SVGA, XGA and higher addressability.
- Up to 227 Megabytes/sec bandwidth
- Up to 1.8 Gbps throughput
- Narrow bus reduces cable size and cost
- 290 mV swing LVDS devices for low EMI
- PLL requires no external components
- Low profile 56-lead TSSOP package.
- DS90CF384 also available in 64 ball, 0.8mm fine pitch ball grid array(FBGA) package
- Falling edge data strobe Receiver
- Compatible with TIA/EIA-644 LVDS standard
- ESD rating >7 kV
- Operating Temperature: −40˚C to +85˚C

Block Diagrams

Application



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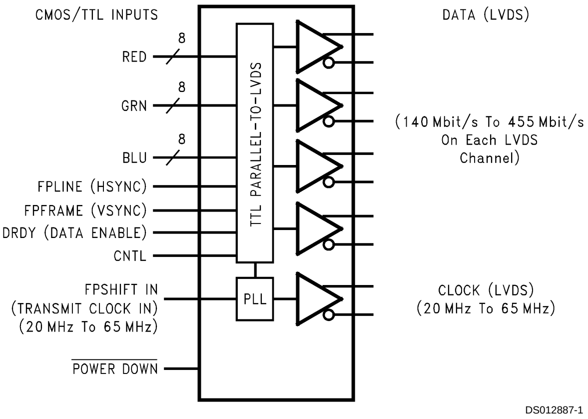
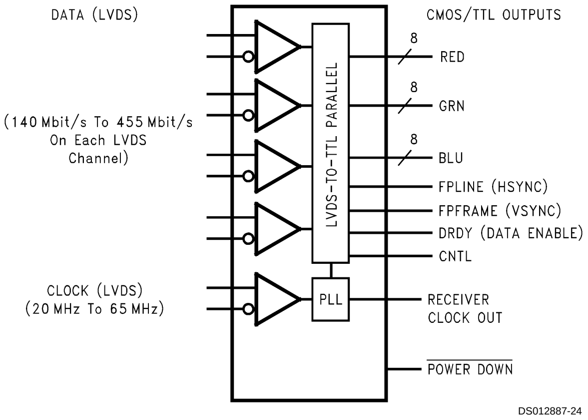
Block Diagrams (Continued)

DS90C383



Order Number DS90C383MTD
See NS Package Number MTD56

DS90CF384



Order Number DS90CF384MTD or DS90CF384SLC
See NS Package Number MTD56 or SLC64A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +4V
CMOS/TTL Input Voltage	−0.3V to (V_{CC} + 0.3V)
CMOS/TTL Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Driver Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Output Short Circuit Duration	Continuous
Junction Temperature	+150˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature (Soldering, 4 sec for TSSOP)	+260˚C
Solder Reflow Temperature (20 sec for FBGA)	+220˚C
Maximum Package Power Dissipation Capacity 25˚C	
MTD56 (TSSOP) Package:	
DS90C383MTD	1.63 W
DS90CF384MTD	1.61 W
Package Derating:	
DS90C383MTD	12.5 mW/˚C above +25˚C
DS90CF384MTD	12.4 mW/˚C above +25˚C
Maximum Package Power Dissipation Capacity 25˚C	
SLC64A Package:	
DS90CF384SLC	2.0 W
Package Derating:	
DS90CF384SLC	10.2 mW/˚C above +25˚C
ESD Rating (HBM, 1.5 kΩ, 100 pF)	> 7 kV

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−40	+25	+85	˚C
Receiver Input Range	0		2.4	V
Supply Noise Voltage (V_{CC})			100	mV_{PP}

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS/TTL DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA	2.7	3.3		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA		0.06	0.3	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = V_{CC}, GND, 2.5V or 0.4V		±5.1	±10	µA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V		−60	−120	mA
LVDS DC SPECIFICATIONS						
V_{OD}	Differential Output Voltage	R_L = 100Ω	250	345	450	mV
ΔV_{OD}	Change in V_{OD} between complimentary output states				35	mV
V_{OS}	Offset Voltage (Note 4)		1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between complimentary output states				35	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω		−3.5	−5	mA
I_{OZ}	Output TRI-STATE® Current	$\overline{\text{Power Down}}$ = 0V, V_{OUT} = 0V or V_{CC}		±1	±10	µA
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V			+100	mV
V_{TL}	Differential Input Low Threshold		−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V, V_{CC} = 3.6V			±10	µA
		V_{IN} = 0V, V_{CC} = 3.6V			±10	µA
TRANSMITTER SUPPLY CURRENT						
ICCTW	Transmitter Supply Current	R_L = 100Ω, C_L = 5 pF, f = 32.5 MHz		31	45	mA
	Worst Case	Worst Case Pattern f = 37.5 MHz		32	50	mA
		(Figures 1, 3), T_A = −40˚C to +85˚C f = 65 MHz		42	55	mA

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TRANSMITTER SUPPLY CURRENT							
ICCTG	Transmitter Supply Current	R_L = 100Ω, C_L = 5 pF,	f = 32.5 MHz		23	35	mA
	16 Grayscale	16 Grayscale Pattern	f = 37.5 MHz		28	40	mA
		(Figures 2, 3), T_A = −40˚C to +85˚C	f = 65 MHz		31	45	mA
ICCTZ	Transmitter Supply Current Power Down	$\overline{\text{Power Down}}$ = Low Driver Outputs in TRI-STATE® under Power Down Mode			10	55	µA
RECEIVER SUPPLY CURRENT							
ICCRW	Receiver Supply Current	C_L = 8 pF,	f = 32.5 MHz		49	65	mA
	Worst Case	Worst Case Pattern	f = 37.5 MHz		53	70	mA
		(Figures 1, 4), T_A = −40˚C to +85˚C	f = 65 MHz		78	105	mA
ICCRG	Receiver Supply Current,	C_L = 8 pF,	f = 32.5 MHz		28	45	mA
	16 Grayscale	16 Grayscale Pattern	f = 37.5 MHz		30	47	mA
		(Figures 2, 4), T_A = −40˚C to +85˚C	f = 65 MHz		43	60	mA
ICCRZ	Receiver Supply Current Power Down	$\overline{\text{Power Down}}$ = Low Receiver Outputs Stay Low during Power Down Mode			10	55	µA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{CC} = 3.3V and T_A = +25C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Note 4: V_{OS} previously referred as V_{CM}.

Transmitter Switching Characteristics

Over recommended operating supply and −40˚C to +85˚C ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time *(Figure 3)*			0.75	1.5	ns
LHLT	LVDS High-to-Low Transition Time *(Figure 3)*			0.75	1.5	ns
TCIT	TxCLK IN Transition Time *(Figure 5)*				5	ns
TCCS	TxOUT Channel-to-Channel Skew *(Figure 6)*			250		ps
TPPos0	Transmitter Output Pulse Position for Bit 0 *(Figure 17)*	f = 65 MHz	−0.4	0	0.3	ns
TPPos1	Transmitter Output Pulse Position for Bit 1		1.8	2.2	2.5	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		4.0	4.4	4.7	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		6.2	6.6	6.9	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		8.4	8.8	9.1	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		10.6	11	11.3	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		12.8	13.2	13.5	ns
TCIP	TxCLK IN Period *(Figure 7)*		15	T	50	ns
TCIH	TxCLK IN High Time *(Figure 7)*		0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time *(Figure 7)*		0.35T	0.5T	0.65T	ns
TSTC	TxIN Setup to TxCLK IN *(Figure 7)*	f = 65 MHz	2.5			ns
THTC	TxIN Hold to TxCLK IN *(Figure 7)*		0			ns
TCCD	TxCLK IN to TxCLK OUT Delay 25˚C, V_{CC} = 3.3V *(Figure 9)*		3.0	3.7	5.5	ns
TPLLS	Transmitter Phase Lock Loop Set *(Figure 11)*				10	ms
TPDD	Transmitter Power Down Delay *(Figure 15)*				100	ns

Receiver Switching Characteristics

Over recommended operating supply and −40˚C to +85˚C ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
CLHT	CMOS/TTL Low-to-High Transition Time *(Figure 4)*			2.2	5.0	ns
CHLT	CMOS/TTL High-to-Low Transition Time *(Figure 4)*			2.2	5.0	ns
RSPos0	Receiver Input Strobe Position for Bit 0 *(Figure 18)*	f = 65 MHz	0.7	1.1	1.4	ns
RSPos1	Receiver Input Strobe Position for Bit 1		2.9	3.3	3.6	ns
RSPos2	Receiver Input Strobe Position for Bit 2		5.1	5.5	5.8	ns
RSPos3	Receiver Input Strobe Position for Bit 3		7.3	7.7	8.0	ns
RSPos4	Receiver Input Strobe Position for Bit 4		9.5	9.9	10.2	ns
RSPos5	Receiver Input Strobe Position for Bit 5		11.7	12.1	12.4	ns
RSPos6	Receiver Input Strobe Position for Bit 6		13.9	14.3	14.6	ns
RSKM	RxIN Skew Margin (Note 5) *(Figure 19)*	f = 65 MHz	400			ps
RCOP	RxCLK OUT Period *(Figure 8)*		15	T	50	ns
RCOH	RxCLK OUT High Time *(Figure 8)*	f = 65 MHz	7.3	8.6		ns
RCOL	RxCLK OUT Low Time *(Figure 8)*		3.45	4.9		ns
RSRC	RxOUT Setup to RxCLK OUT *(Figure 8)*		2.5	6.9		ns
RHRC	RxOUT Hold to RxCLK OUT *(Figure 8)*		2.5	5.7		ns
RCCD	RxCLK IN to RxCLK OUT Delay 25˚C, V_{CC} = 3.3V *(Figure 10)*		5.0	7.1	9.0	ns
RPLLS	Receiver Phase Lock Loop Set *(Figure 12)*				10	ms
RPDD	Receiver Power Down Delay *(Figure 16)*				1	µs

Note 5: Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account the transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window-RSPOS). This margin allows for LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable), and clock jitter (less than 250 ps).

AC Timing Diagrams

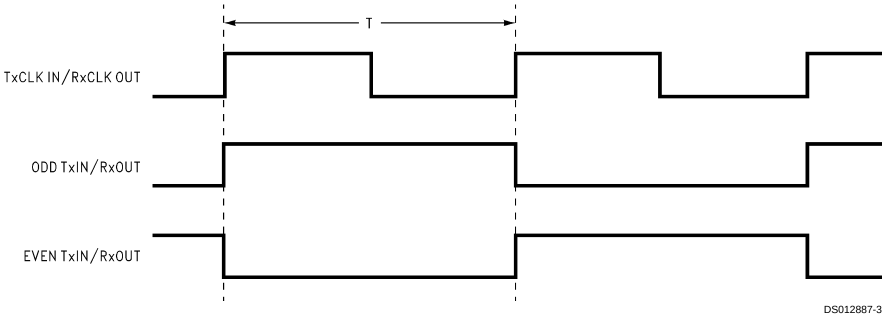


FIGURE 1. "Worst Case" Test Pattern

AC Timing Diagrams (Continued)

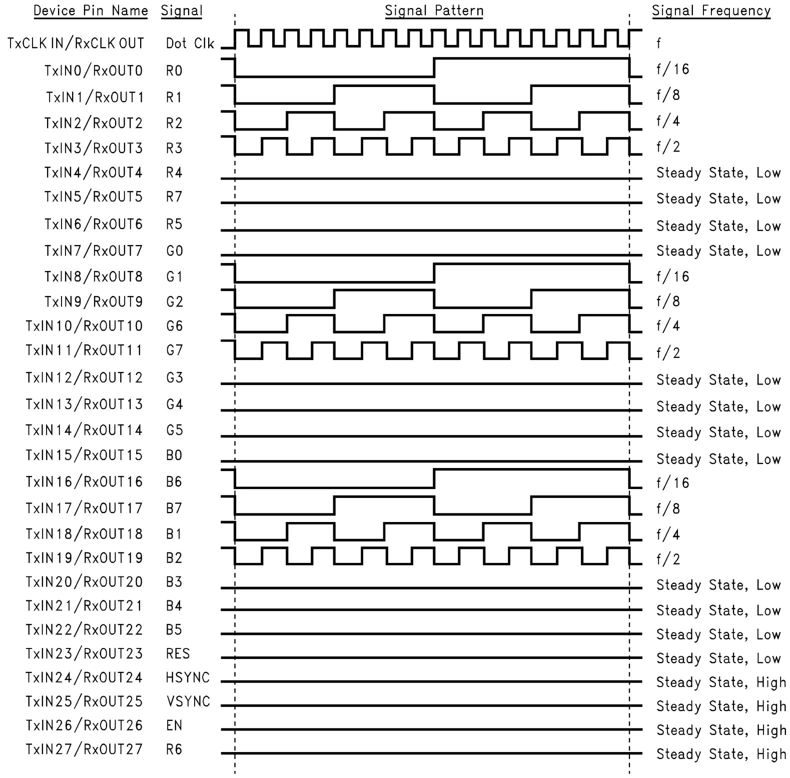


FIGURE 2. "16 Grayscale" Test Pattern (Notes 6, 7, 8, 9)

Note 6: The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

Note 7: The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

Note 8: *Figures 1, 2* show a falling edge data strobe (TxCLK IN/RxCLK OUT).

Note 9: Recommended pin to signal mapping. Customer may choose to define differently.

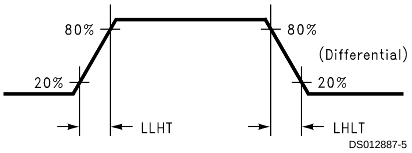


FIGURE 3. DS90C383 (Transmitter) LVDS Output Load and Transition Times

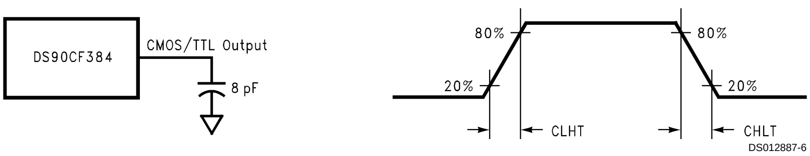


FIGURE 4. DS90CF384 (Receiver) CMOS/TTL Output Load and Transition Times

AC Timing Diagrams (Continued)

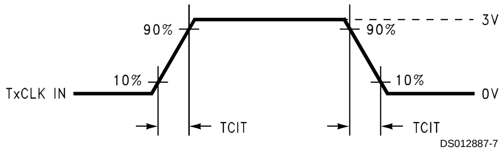
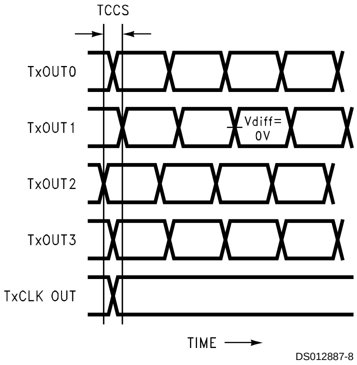


FIGURE 5. DS90C383 (Transmitter) Input Clock Transition Time



Measurements at V_{diff} = 0V
TCCS measured between earliest and latest LVDS edges.
TxCLK Differential Low High Edge

FIGURE 6. DS90C383 (Transmitter) Channel-to-Channel Skew

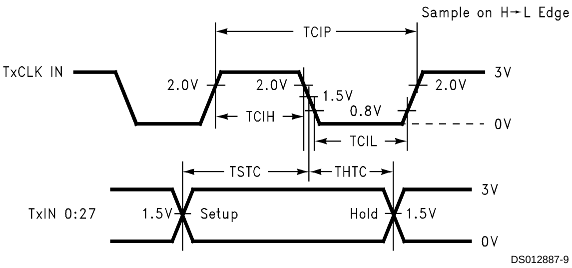


FIGURE 7. DS90C383 (Transmitter) Setup/Hold and High/Low Times (Falling Edge Strobe)

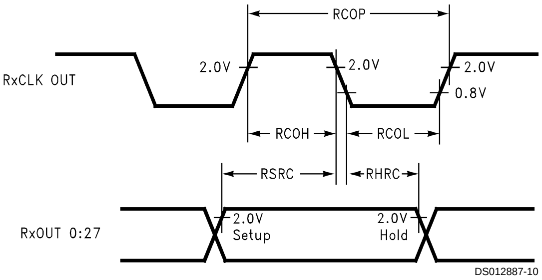


FIGURE 8. DS90CF384 (Receiver) Setup/Hold and High/Low Times

AC Timing Diagrams (Continued)

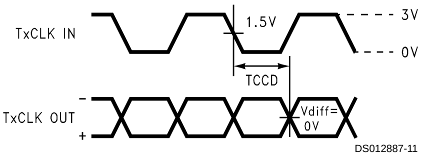


FIGURE 9. DS90C383 (Transmitter) Clock In to Clock Out Delay (Falling Edge Strobe)

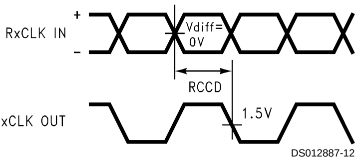


FIGURE 10. DS90CF384 (Receiver) Clock In to Clock Out Delay

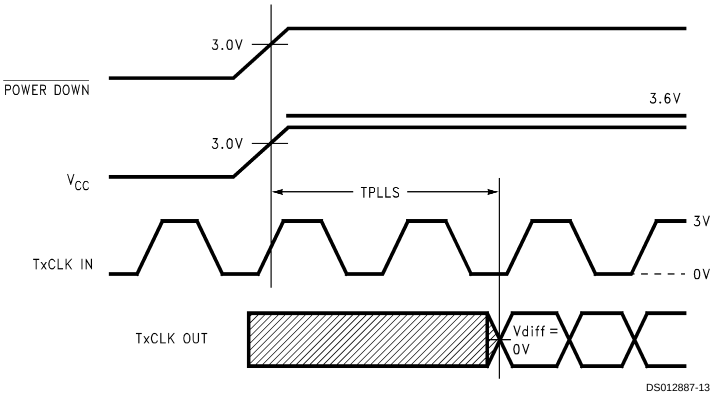


FIGURE 11. DS90C383 (Transmitter) Phase Lock Loop Set Time

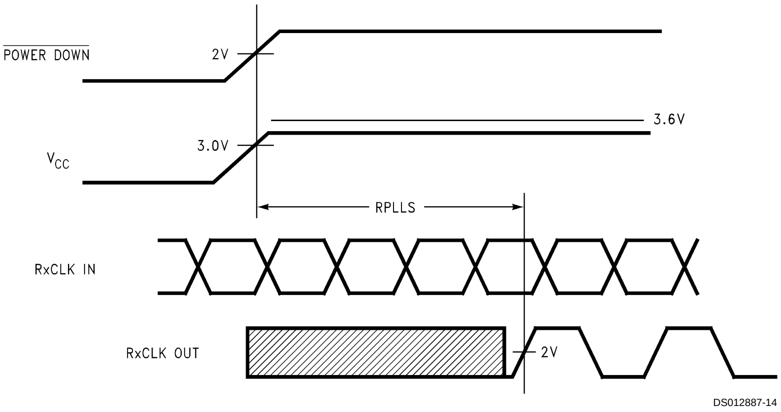


FIGURE 12. DS90CF384 (Receiver) Phase Lock Loop Set Time

AC Timing Diagrams (Continued)

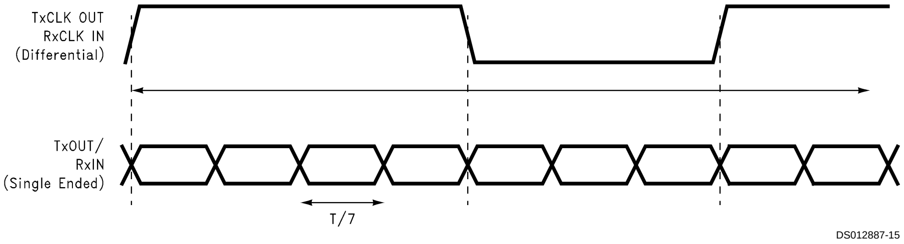


FIGURE 13. Seven Bits of LVDS in Once Clock Cycle

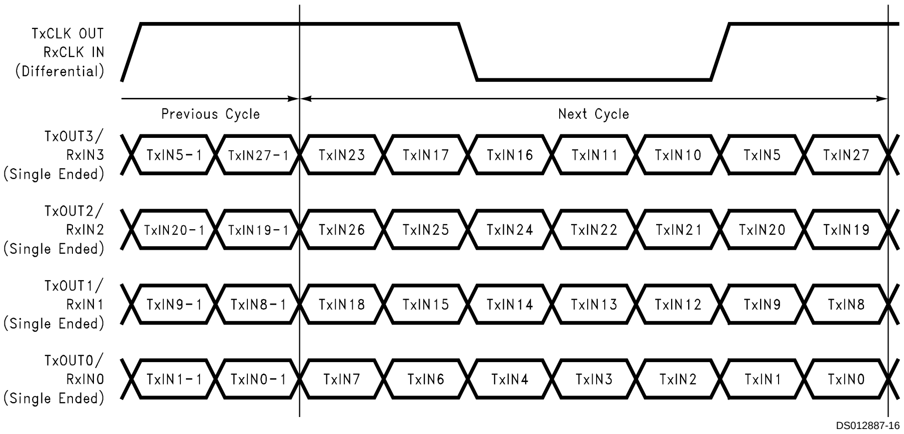


FIGURE 14. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs

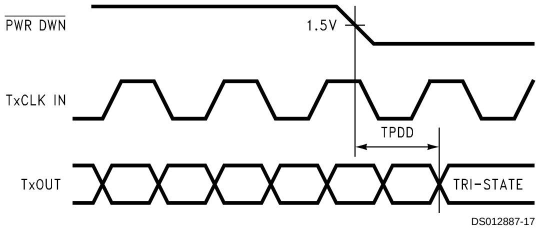


FIGURE 15. Transmitter Power Down Delay

AC Timing Diagrams (Continued)

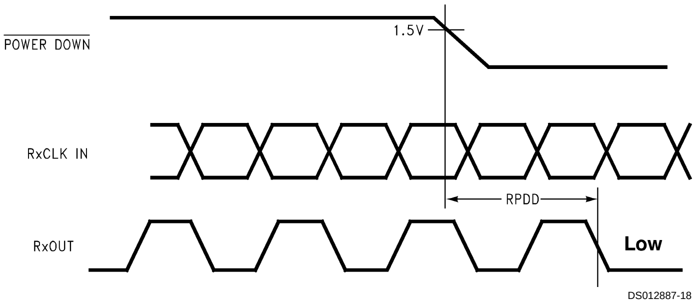


FIGURE 16. Receiver Power Down Delay

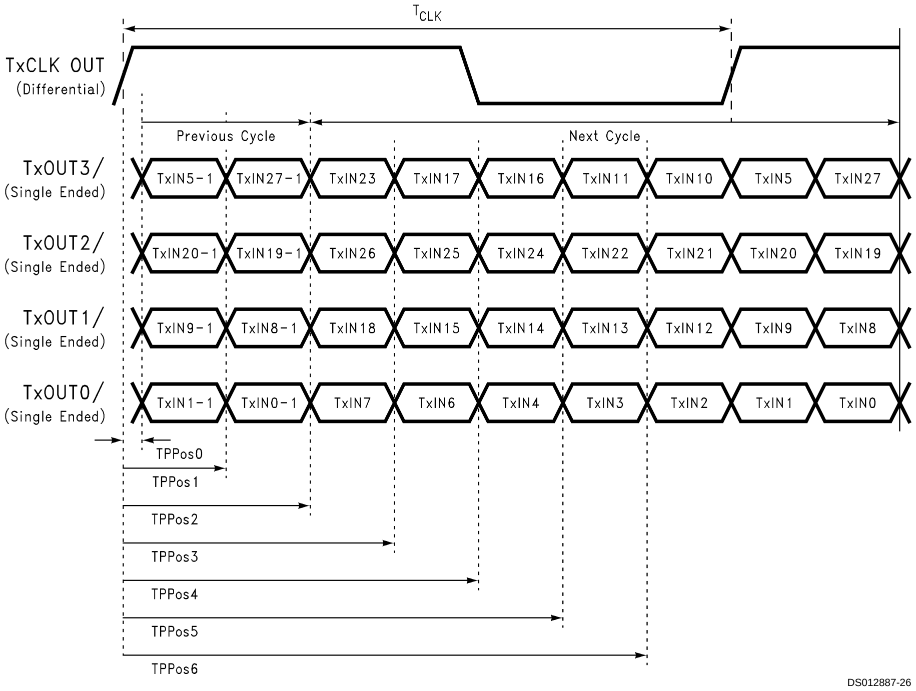


FIGURE 17. Transmitter LVDS Output Pulse Position Measurement

AC Timing Diagrams (Continued)

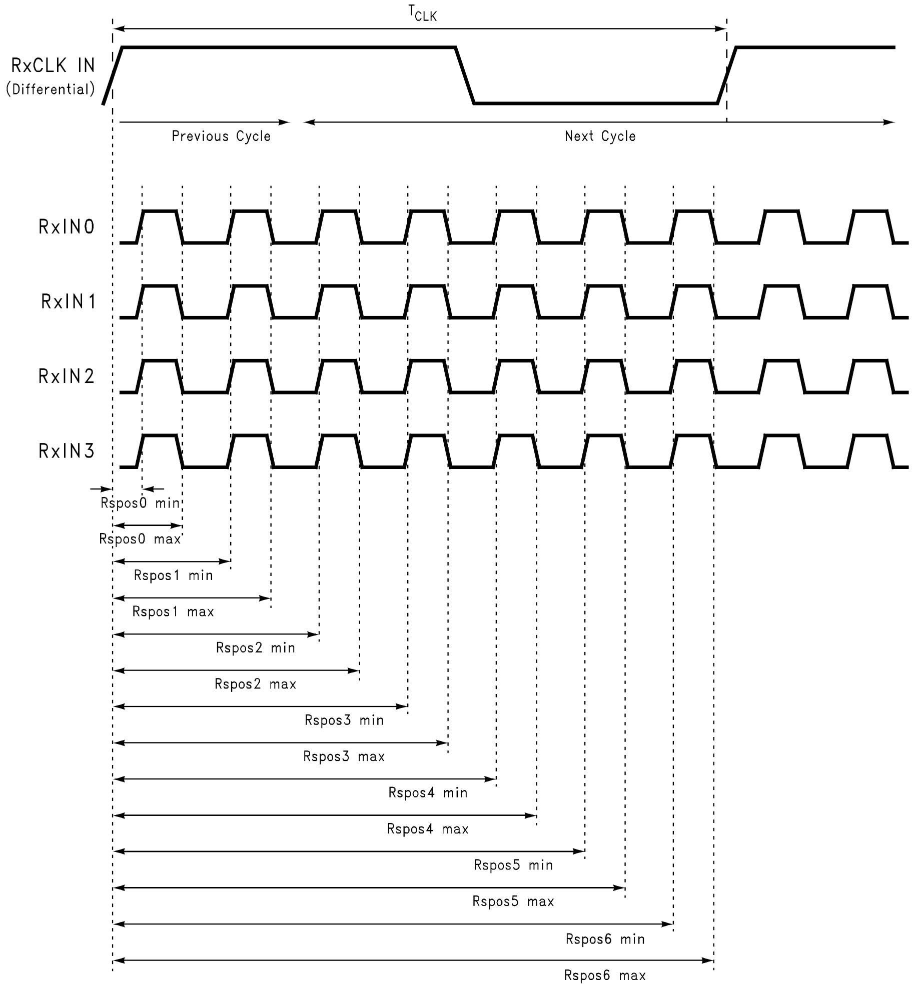


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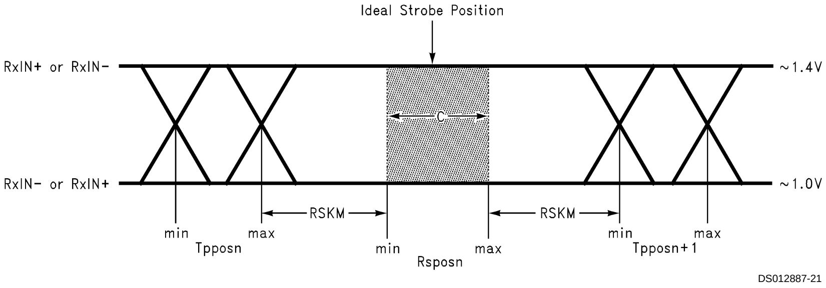
FIGURE 18. Receiver LVDS Input Strobe Position

AC Timing Diagrams (Continued)



C — Setup and Hold Time (Internal data sampling window) defined by Rspos (receiver input strobe position) min and max
Tppos — Transmitter output pulse position (min and max)
RSKM = Cable Skew (type, length) + Source Clock Jitter (cycle to cycle) (Note 10) + ISI (Inter-symbol interference) (Note 11)
Cable Skew — typically 10 ps–40 ps per foot, media dependent

Note 10: Cycle-to-cycle jitter is less than 250 ps at 65 MHZ

Note 11: ISI is dependent on interconnect length; may be zero

FIGURE 19. Receiver LVDS Input Skew Margin

DS90C383 Pin Description — FPD Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	28	TTL level input. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines — FPLINE, FPFRAME and DRDY (also referred to as HSYNC, VSYNC, Data Enable).
TxOUT+	O	4	Positive LVDS differential data output.
TxOUT−	O	4	Negative LVDS differential data output.
FPSHIFT IN	I	1	TTL level clock input. The falling edge acts as data strobe. Pin name TxCLK IN.
R_FB	I	1	Programmable strobe select.
RTxCLK OUT+	O	1	Positive LVDS differential clock output.
TxCLK OUT−	O	1	Negative LVDS differential clock output.
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. When asserted (low input) TRI-STATES the outputs, ensuring low current at power down.
V_{CC}	I	3	Power supply pins for TTL inputs.
GND	I	4	Ground pins for TTL inputs.
PLL V_{CC}	I	1	Power supply pin for PLL.
PLL GND	I	2	Ground pins for PLL.
LVDS V_{CC}	I	1	Power supply pin for LVDS outputs.
LVDS GND	I	3	Ground pins for LVDS outputs.

DS90CF384 MTD56 package Pin Description — FPD Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	4	Positive LVDS differential data inputs.
RxIN−	I	4	Negative LVDS differential data inputs.
RxOUT	O	28	TTL level data outputs. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines — FPLINE, FPFRAME, DRDY (also referred to as HSYNC, VSYNC, Data Enable).
RxCLK IN+	I	1	Positive LVDS differential clock input.
RxCLK IN−	I	1	Negative LVDS differential clock input.
FPSHIFT OUT	O	1	TTL level clock output. The falling edge acts as data strobe. Pin name RxCLK OUT.
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. When asserted (low input) the receiver outputs are low.
V_{CC}	I	4	Power supply pins for TTL outputs.
GND	I	5	Ground pins for TTL outputs.
PLL V_{CC}	I	1	Power supply for PLL.
PLL GND	I	2	Ground pin for PLL.
LVDS V_{CC}	I	1	Power supply pin for LVDS inputs.
LVDS GND	I	3	Ground pins for LVDS inputs.

DS90CF384 64 ball FBGA package Pin Description—FPD Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	4	Positive LVDS differential data inputs.
RxIN−	I	4	Negative LVDS differential data inputs.
RxOUT	O	28	TTL level data outputs. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines—FPLINE, FPFRAME, DRDY (also referred to as HSYNC, VSYNC, Data Enable).
RxCLK IN+	I	1	Positive LVDS differential clock input.
RxCLK IN−	I	1	Negative LVDS differential clock input.
FPSHIFT OUT	O	1	TTL level clock output. The falling edge acts as data strobe. Pin name RxCLK OUT.
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. When asserted (low input) the receiver outputs are low.
V_{CC}	I	4	Power supply pins for TTL outputs.
GND	I	5	Ground pins for TTL outputs.
PLL V_{CC}	I	1	Power supply for PLL.
PLL GND	I	2	Ground pin for PLL.
LVDS V_{CC}	I	1	Power supply pin for LVDS inputs.
LVDS GND	I	3	Ground pins for LVDS inputs.
NC		6	Pins not connected.

Applications Information

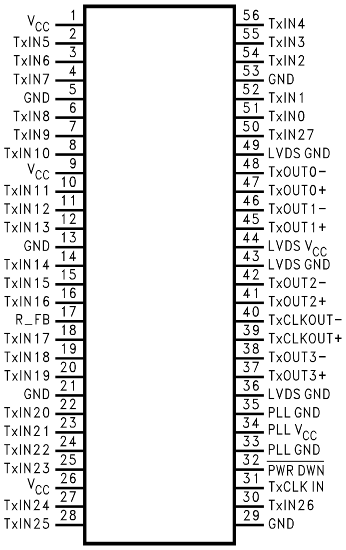
The DS90C383 and DS90CF384 are backward compatible with the existing 5V FPD Link transmitter/receiver pair (DS90CR583, DS90CR584, DS90CF583 and DS90CF584). To upgrade from a 5V to a 3.3V system the following must be addressed:

1. Change 5V power supply to 3.3V. Provide this supply to the V_{CC}, LVDS V_{CC} and PLL V_{CC} of both the transmitter and receiver devices. This change may enable the removal of a 5V supply from the system, and power may be supplied from an existing 3V power source.
2. The DS90C383 (transmitter) incorporates a rise/fall strobe select pin. This select function is on pin 17, formerly a V_{CC} connection on the 5V products. When the rise/fall strobe select pin is connected to V_{CC}, the part is configured with a rising edge strobe. In a system currently using a 5V rising edge strobe transmitter (DS90CR583), no layout changes are required to accommodate the new rise/fall select pin on the 3.3V transmitter. The V_{CC} signal may remain at pin 17, and the device will be configured with a rising edge strobe.

   When converting from a 5V falling edge transmitter (DS90CF583) to the 3V transmitter a minimal board layout change is necessary. The 3.3V transmitter will not be configured with a falling edge strobe if V_{CC} remains connected to the select pin. To guarantee the 3.3V transmitter functions with a falling edge strobe pin 17 should be connected to ground OR left unconnected. When not connected (left open) and internal pull-down resistor ties pin 17 to ground, thus configuring the transmitter with a falling edge strobe.
3. The DS90C383 transmitter input and control inputs accept 3.3V TTL/CMOS levels. They are not 5V tolerant.

Pin Diagrams

DS90C383MTD



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DS90CF384MTD

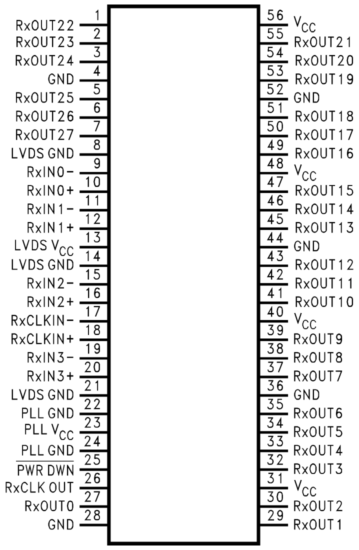

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TABLE 1. Programmable Transmitter

Pin	Condition	Strobe Status
R_FB	R_FB = V_{CC}	Rising edge strobe
R_FB	R_FB = GND	Falling edge strobe

DS90CF384 64 ball, FBGA package pin definition—FPD Link Receiver

By Pin			By Pin Type		
Pin	Pin Name	Type	Pin	Pin Name	Type
A1	RxOUT17	O	A4	GND	G
A2	VCC	P	B1	GND	G
A3	RxOUT15	O	B6	GND	G
A4	GND	G	D8	GND	G
A5	RxOUT12	O	E3	GND	G
A6	RxOUT8	O	E5	LVDS GND	G
A7	RxOUT7	O	G3	LVDS GND	G
A8	RxOUT6	O	G7	LVDS GND	G
B1	GND	G	H5	LVDS GND	G
B2	NC		F6	PLL GND	G
B3	RxOUT16	O	G8	PLL GND	G
B4	RxOUT11	O	E6	PWR DWN	I
B5	VCC	P	H6	RxCLKIN-	I
B6	GND	G	H7	RxCLKIN+	I
B7	RxOUT5	O	H2	RxIN0-	I
B8	RxOUT3	O	H3	RxIN0+	I
C1	RxOUT21	O	F4	RxIN1-	I
C2	NC		G4	RxIN1+	I
C3	RxOUT18	O	G5	RxIN2-	I
C4	RxOUT14	O	F5	RxIN2+	I
C5	RxOUT9	O	G6	RxIN3-	I
C6	RxOUT4	O	H8	RxIN3+	I
C7	NC		E7	RxCLKOUT	O
C8	RxOUT1	O	E8	RxOUT0	O
D1	VCC	P	C8	RxOUT1	O
D2	RxOUT20	O	D5	RxOUT10	O
D3	RxOUT19	O	B4	RxOUT11	O
D4	RxOUT13	O	A5	RxOUT12	O
D5	RxOUT10	O	D4	RxOUT13	O
D6	VCC	P	C4	RxOUT14	O
D7	RxOUT2	O	A3	RxOUT15	O
D8	GND	G	B3	RxOUT16	O
E1	RxOUT22	O	A1	RxOUT17	O
E2	RxOUT24	O	C3	RxOUT18	O
E3	GND	G	D3	RxOUT19	O
E4	LVDS VCC	P	D7	RxOUT2	O
E5	LVDS GND	G	D2	RxOUT20	O
E6	PWR DWN	I	C1	RxOUT21	O
E7	RxCLKOUT	O	E1	RxOUT22	O
E8	RxOUT0	O	F1	RxOUT23	O
F1	RxOUT23	O	E2	RxOUT24	O
F2	RxOUT26	O	G1	RxOUT25	O
F3	NC		F2	RxOUT26	O
F4	RxIN1-	I	H1	RxOUT27	O
F5	RxIN2+	I	B8	RxOUT3	O
F6	PLL GND	G	C6	RxOUT4	O
F7	PLL VCC	P	B7	RxOUT5	O
F8	NC		A8	RxOUT6	O

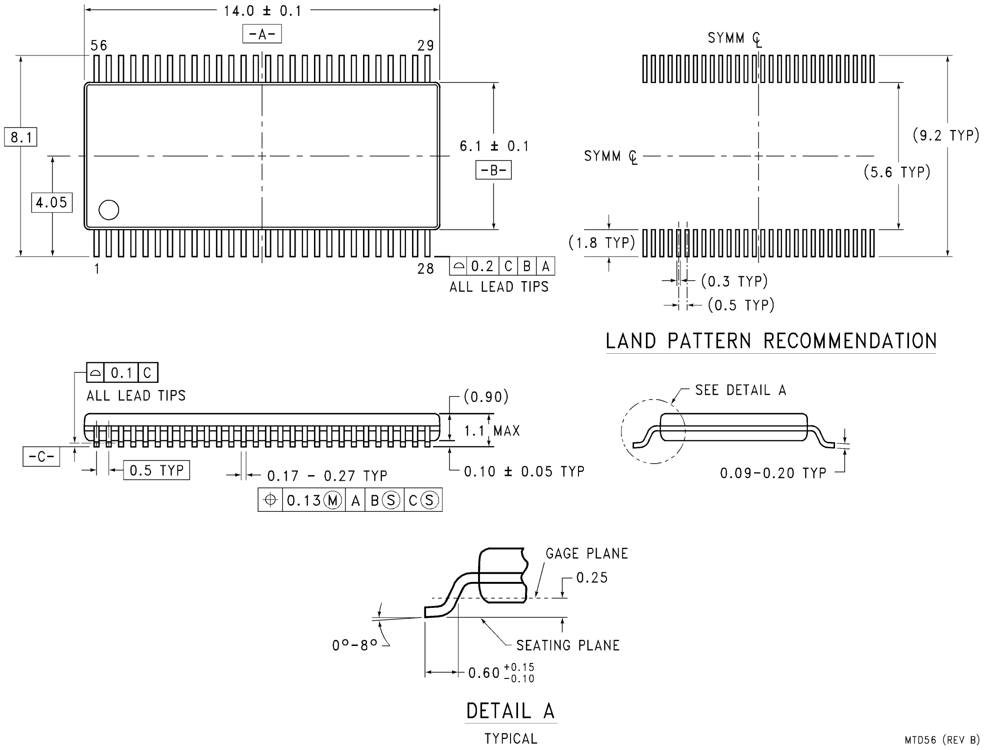
DS90CF384 64 ball, FBGA package pin definition — FPD Link Receiver

(Continued)

By Pin			By Pin Type		
G1	RxOUT25	O	A7	RxOUT7	O
G2	NC		A6	RxOUT8	O
G3	LVDS GND	G	C5	RxOUT9	O
G4	RxIN1+	I	E4	LVDS VCC	P
G5	RxIN2-	I	H4	LVDS VCC	P
G6	RxIN3-	I	F7	PLL VCC	P
G7	LVDS GND	G	A2	VCC	P
G8	PLL GND	G	B5	VCC	P
H1	RxOUT27	O	D1	VCC	P
H2	RxIN0-	I	D6	VCC	P
H3	RxIN0+	I	B2	NC	
H4	LVDS VCC	P	C2	NC	
H5	LVDS GND	G	C7	NC	
H6	RxCLKIN-	I	F3	NC	
H7	RxCLKIN+	I	F8	NC	
H8	RxIN3+	I	G2	NC	

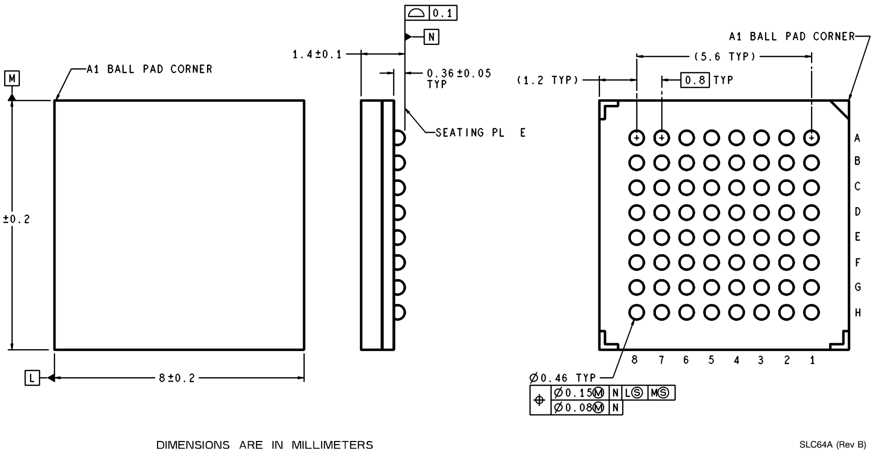
G:Ground
I : Input
O:Output
P:Power
NC:Not connectted

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Molded Thin Shrink Small Outline Package, JEDEC
Dimensions show in millimeters
Order Number DS90C383MTD, DS90CF384MTD
NS Package Number MTD56

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



64 ball, 0.8mm fine pitch ball grid array(FBGA) Package
Dimensions show in millimeters
Order Number DS90CF384SLC
NS Package Number SLC64A

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