

## LM6118/LM6218 Fast Settling Dual Operational Amplifiers

### General Description

The LM6118/LM6218 are monolithic fast-settling unity-gain-compensated dual operational amplifiers with  $\pm 20$  mA output drive capability. The PNP input stage has a typical bias current of 200 nA, and the operating supply voltage is  $\pm 5$ V to  $\pm 20$ V.

These dual op amps use slew enhancement with special mirror circuitry to achieve fast response and high gain with low total supply current.

The amplifiers are built on a junction-isolated VIP™ (Vertically Integrated PNP) process which produces fast PNP's that complement the standard NPN's.

### Features

- Low offset voltage:
- 0.01% settling time:
- Slew rate  $A_v = -1$ :
- Slew rate  $A_v = +1$ :
- Gain bandwidth:
- Total supply current:
- Output drives 50 $\Omega$  load ( $\pm 1$ V)

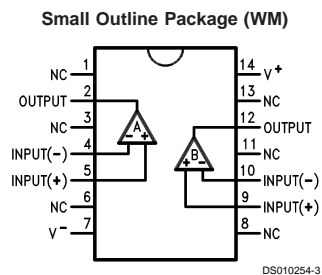
### Typical

0.2 mV
400 ns
140 V/ $\mu$ s
75 V/ $\mu$ s
17 MHz
5.5 mA

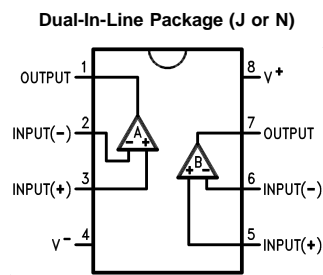
### Applications

- D/A converters
- Fast integrators
- Active filters

### Connection Diagrams and Order Information



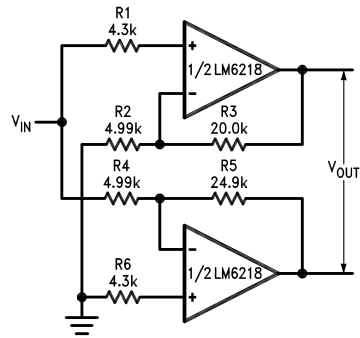
**Top View**  
Order Number LM6218WM  
See NS Package Number M14B



**Top View**  
Order Number LM6118N,  
LM6218AN or LM6218N  
See NS Package Number N08E

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## Typical Applications



Single ended input to differential output  
 $A_V = 10$ , BW = 3.2 MHz  
40  $V_{PP}$  Response = 1.4 MHz  
 $V_S = \pm 15V$

**Wide-Band, Fast-Settling  
40  $V_{PP}$  Amplifier**

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage	42V
Input Voltage	(Note 2)
Differential Input Current (Note 3)	±10 mA
Output Current (Note 4)	Internally Limited
Power Dissipation (Note 5)	500 mW
ESD Tolerance	
(C = 100 pF, R = 1.5 kΩ)	±2 kV

Junction Temperature	150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature	
(Soldering, 10 sec.)	300°C

## Operating Temp. Range

LM6118	-55°C to +125°C
LM6218A	-40°C to +85°C
LM6218	-40°C to +85°C

## Electrical Characteristics

±5V ≤ V<sub>S</sub> ≤ ±20V, V<sub>CM</sub> = 0V, V<sub>OUT</sub> = 0V, I<sub>OUT</sub> = 0A, unless otherwise specified. Limits with standard type face are for T<sub>J</sub> = 25°C, and **Bold Face Type** are for **Temperature Extremes**.

Parameter	Conditions	Typ 25°C	LM6118 Limits (Note 6)	LM6218A Limits (Note 6)	LM6218 Limits (Note 6)	Units
Input Offset Voltage	V <sub>S</sub> = ±15V	0.2	1 <b>2</b>	1 <b>2</b>	3 <b>4</b>	mV (max)
Input Offset Voltage	V <sub>-</sub> + 3V ≤ V <sub>CM</sub> ≤ V <sub>+</sub> - 3.5V	0.3	1.5 <b>2.5</b>	1.5 <b>2.5</b>	3.5 <b>4.5</b>	mV (max)
Input Offset Current	V <sub>-</sub> + 3V ≤ V <sub>CM</sub> ≤ V <sub>+</sub> - 3.5V	20	50 <b>250</b>	50 <b>100</b>	100 <b>200</b>	nA (max)
Input Bias Current	V <sub>-</sub> + 3V ≤ V <sub>CM</sub> ≤ V <sub>+</sub> - 3.5V	200	350 <b>950</b>	350 <b>950</b>	500 <b>1250</b>	nA (max)
Input Common Mode Rejection Ratio	V <sub>-</sub> + 3V ≤ V <sub>CM</sub> ≤ V <sub>+</sub> - 3.5V V <sub>S</sub> = ±20V	100	90 <b>85</b>	90 <b>85</b>	80 <b>75</b>	dB (min)
Positive Power Supply Rejection Ratio	V <sub>-</sub> = -15V 5V ≤ V <sub>+</sub> ≤ 20V	100	90 <b>85</b>	90 <b>85</b>	80 <b>75</b>	dB (min)
Negative Power Supply Rejection Ratio	V <sub>+</sub> = 15V -20V ≤ V <sub>-</sub> ≤ -5V	100	90 <b>85</b>	90 <b>85</b>	80 <b>75</b>	dB (min)
Large Signal Voltage Gain	V <sub>out</sub> = ±15V R <sub>L</sub> = 10k V <sub>S</sub> = ±20V	500	150 <b>100</b>	150 <b>100</b>	100 <b>70</b>	V/mV (min)
	V <sub>out</sub> = ±10V R <sub>L</sub> = 500 V <sub>S</sub> = ±15V (±20 mA)	200	50 <b>30</b>	50 <b>30</b>	40 <b>25</b>	V/mV (min)
V <sub>O</sub> Output Voltage Swing	Supply = ±20V R <sub>L</sub> = 10k	17.3	±17	±17	±17	V (min)
Total Supply Current	V <sub>S</sub> = ±15V	5.5	7 <b>7.5</b>	7 <b>7.5</b>	7 <b>7.5</b>	mA (max)
Output Current Limit	V <sub>S</sub> = ±15V, Pulsed	65	100	100	100	mA (max)
Slew Rate, A <sub>v</sub> = -1	V <sub>S</sub> = ±15V, V <sub>out</sub> = ±10V R <sub>S</sub> = R <sub>f</sub> = 2k, C <sub>f</sub> = 10 pF	140	100 <b>50</b>	100 <b>50</b>	100 <b>50</b>	V/μs (min)
Slew Rate, A <sub>v</sub> = +1	V <sub>S</sub> = ±15V, V <sub>out</sub> = ±10V R <sub>S</sub> = R <sub>f</sub> = 2k, C <sub>f</sub> = 10 pF	75	50 <b>30</b>	50 <b>30</b>	50 <b>30</b>	V/μs (min)
Gain-Bandwidth Product	V <sub>S</sub> = ±15V, f <sub>o</sub> = 200 kHz	17	14	14	13	MHz (min)
0.01% Settling Time A <sub>v</sub> = -1	ΔV <sub>out</sub> = 10V, V <sub>S</sub> = ±15V, R <sub>S</sub> = R <sub>f</sub> = 2k, C <sub>f</sub> = 10 pF	400				ns
Input Capacitance	Inverter	5				pF
	Follower	3				pF

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

**Note 2:** Input voltage range is (V<sup>+</sup> - 1V) to (V<sup>-</sup>).

## Electrical Characteristics (Continued)

**Note 3:** The inputs are shunted with three series-connected diodes back-to-back for input differential clamping. Therefore differential input voltages greater than about 1.8V will cause excessive current to flow unless limited to less than 10 mA.

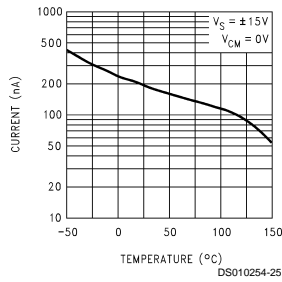
**Note 4:** Current limiting protects the output from a short to ground or any voltage less than the supplies. With a continuous overload, the package dissipation must be taken into account and heat sinking provided when necessary.

**Note 5:** Devices must be derated using a thermal resistance of 90°C/W for the N and WM packages.

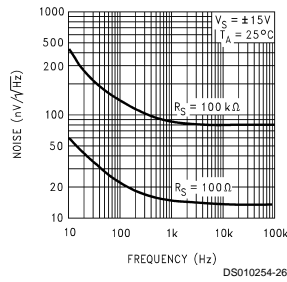
**Note 6:** Limits are guaranteed by testing or correlation.

## Typical Performance Characteristics

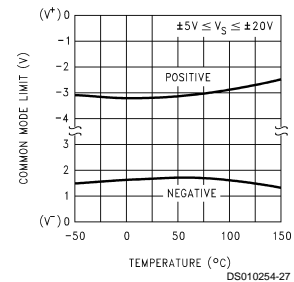
### Input Bias Current



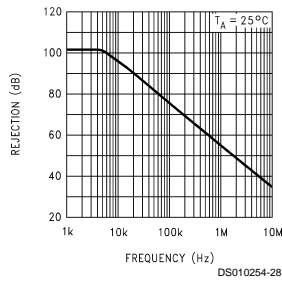
### Input Noise Voltage



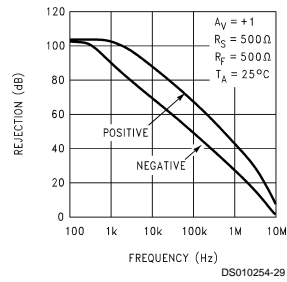
### Common Mode Limits



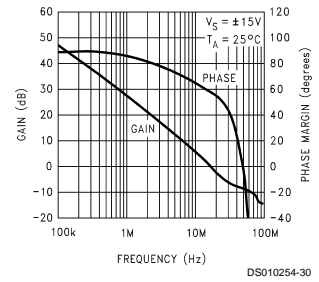
### Common Mode Rejection



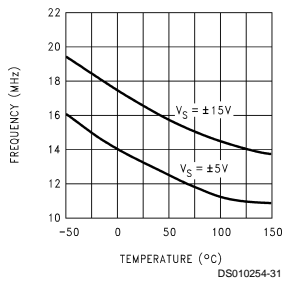
### Power Supply Rejection



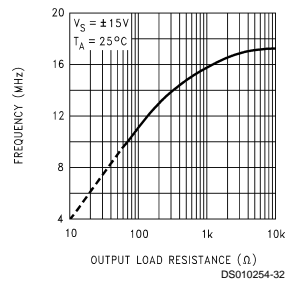
### Frequency Response High Frequency



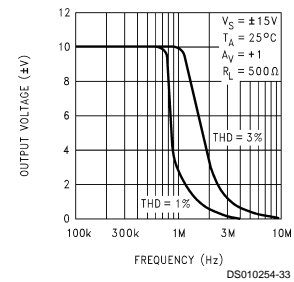
### Unity Gain Bandwidth



### Unity Gain Bandwidth vs Output Load

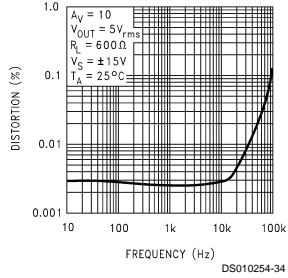


### Large Signal Response (Sine Wave)

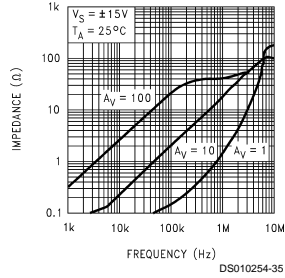


## Typical Performance Characteristics (Continued)

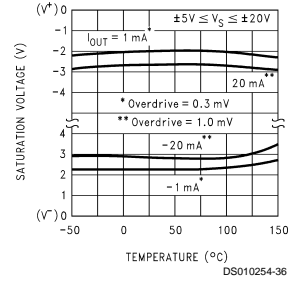
**Total Harmonic Distortion**



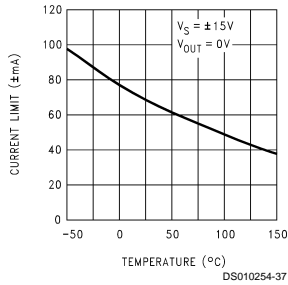
**Output Impedance**



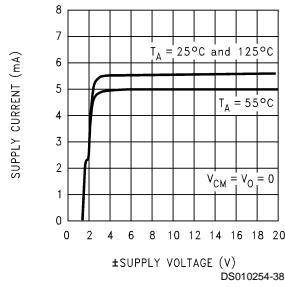
**Output Saturation**



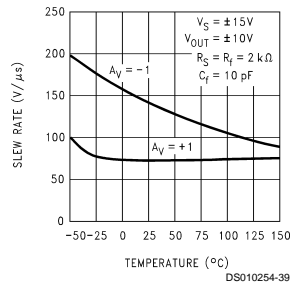
**Output Current Limit**



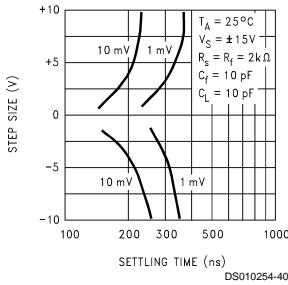
**Supply Current (Both Amplifiers)**



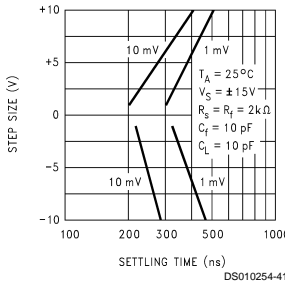
**Slew Rate**



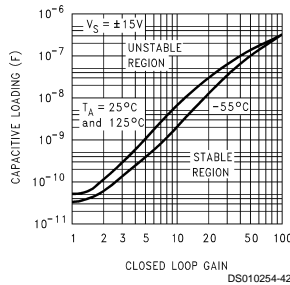
**Inverter Settling Time**



**Follower Settling Time**

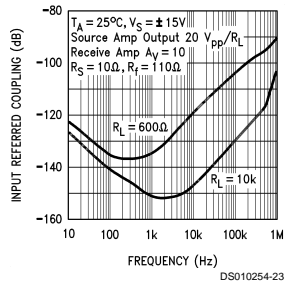


**Typical Stability Range**

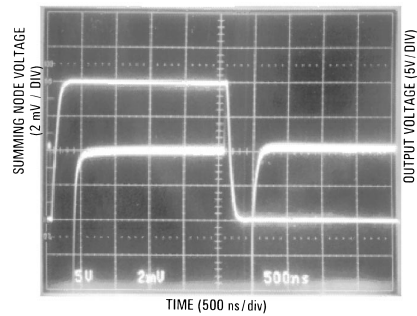


## Typical Performance Characteristics (Continued)

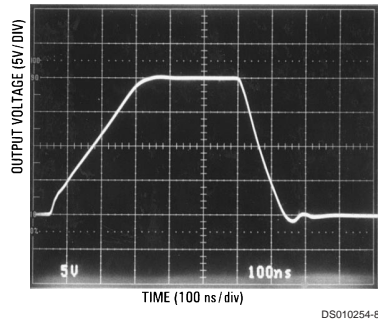
### Amplifier to Amplifier Coupling



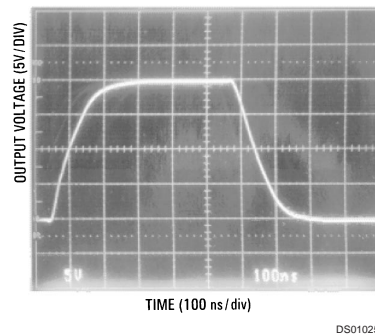
### Settling Time, $V_S = \pm 15\text{V}$



### Step Response, $A_V = +1$ , $V_S = \pm 15\text{V}$



### Step Response, $A_V = -1$ , $V_S = \pm 15\text{V}$



## Application Information

### General

The LM6118/LM6218 are high-speed, fast-settling dual op-amps. To insure maximum performance, circuit board layout is very important. Minimizing stray capacitance at the inputs and reducing coupling between the amplifier's input and output will minimize problems.

### Supply Bypassing

To assure stability, it is recommended that each power supply pin be bypassed with a  $0.1 \mu\text{F}$  low inductance capacitor near the device. If high frequency spikes from digital circuits or switching supplies are present, additional filtering is recommended. To prevent these spikes from appearing at the output, R-C filtering of the supplies near the device may be necessary.

### Power Dissipation

These amplifiers are specified to 20 mA output current. If accompanied with high supply voltages, relatively high power dissipation in the device will occur, resulting in high junction temperatures. In these cases the package thermal resistance must be taken into consideration. (See Note 5 under Electrical Characteristics.) For high dissipation, an N package with large areas of copper on the pc board is recommended.

### Amplifier Shut Down

If one of the amplifiers is not used, it can be shut down by connecting both the inverting and non-inverting inputs to the  $V^-$  pin. This will reduce the power supply current by approximately 25%.

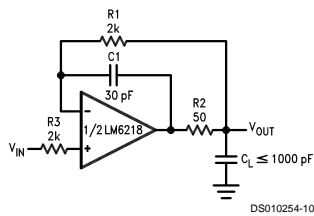
### Capacitive Loading

Maximum capacitive loading is about  $50 \text{ pF}$  for a closed-loop gain of  $+1$ , before the amplifier exhibits excessive ringing and becomes unstable. A curve showing maximum capacitive loads, with different closed-loop gains, is shown in the Typical Performance Characteristics section.

To drive larger capacitive loads at low closed-loop gains, isolate the amplifier output from the capacitive load with  $50\Omega$ . Connect a small capacitor directly from the amplifier output to the inverting input. The feedback loop is closed from the isolated output with a series resistor to the inverting input.

## Application Information (Continued)

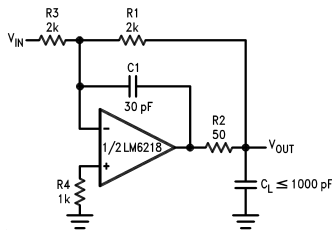
### Voltage Follower



DS010254-10

For  $C_L = 1000$  pF, Small signal BW = 5 MHz  
20 V<sub>p-p</sub> BW = 500 kHz

### Inverter

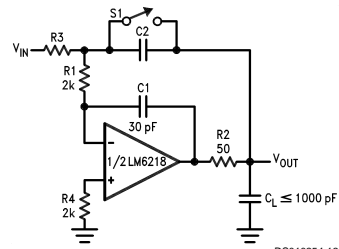


DS010254-11

Settling time to 0.01%, 10V Step

For  $C_L = 1000$  pF, settling time = 1500 ns  
For  $C_L = 300$  pF, settling time = 500 ns

### Integrator



DS010254-12

Examples of unity gain connections for a voltage follower, Inverter, and integrator driving capacitive loads up to 1000 pF are shown here. Different R1–C1 time constants and capacitive loads will have an effect on settling times.

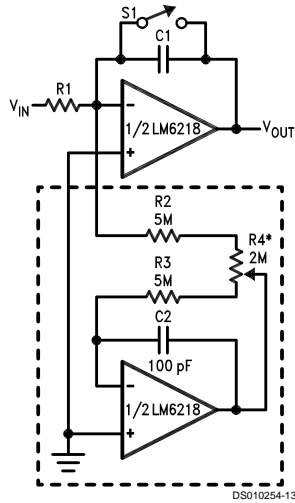
### Input Bias Current Compensation

Input bias current of the first op amp can be reduced or balanced out by the second op amp. Both amplifiers are laid out in mirror image fashion and in close proximity to each other, thus both input bias currents will be nearly identical and will track with temperature. With both op amp inputs at the same potential, a second op amp can be used to convert bias current to voltage, and then back to current feeding the first op amp using large value resistors to reduce the bias current to the level of the offset current.

Examples are shown here for an inverting application, (a) where the inputs are at ground potential, and a second circuit (b) for compensating bias currents for both inputs.

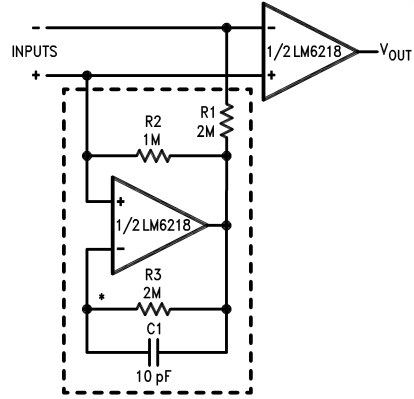
## Application Information (Continued)

### Bias Current Compensation



\*adjust for zero integrator drift

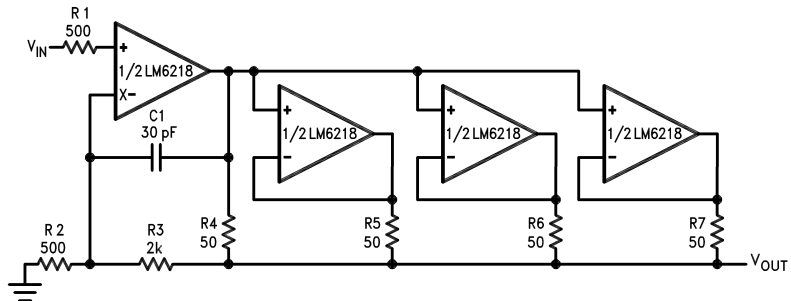
**(a) Inverting Input Bias Compensation for Integrator Application**



\*mount resistor close to input pin to minimize stray capacitance

**(b) Compensation to Both Inputs**

### Amplifier/Parallel Buffer

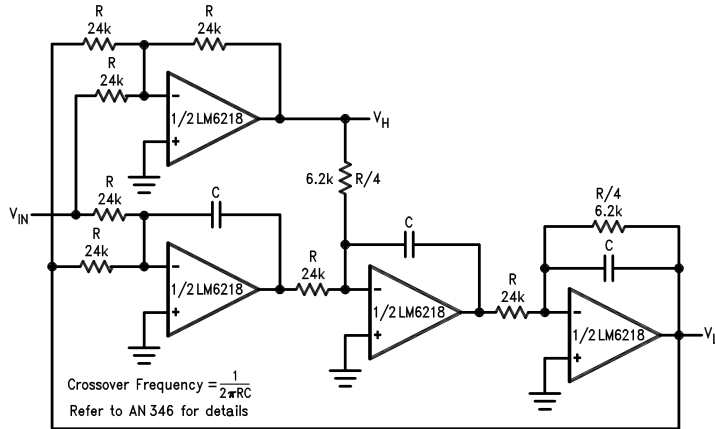


$A_V = +5$ ,  $I_{OUT} \leq 80$  mA  
 $V_S = \pm 15$ V,  $C_L \leq 0.01$   $\mu$ F  
 Large and small signal B.W. = 1.3 MHz (THD = 3%)



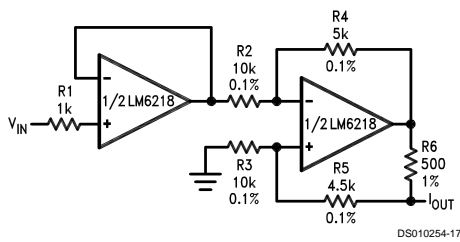
## Application Information (Continued)

### Constant-Voltage Crossover Network With 12 dB/Octave Slope



DS010254-16

### Bilateral Current Source



DS010254-17

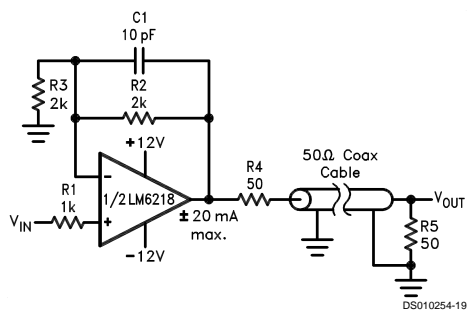
$$V_S = \pm 15V, -10 \leq V_{IN} \leq 10V$$

$$\frac{I_{OUT}}{V_{IN}} = \frac{R_4}{R_2 R_6} = \frac{1 \text{ mA}}{1V}$$

Output dynamic range =  $10V - R_6 |I_{OUT}|$   
 $R_L = 500\Omega$ , small signal BW = 6 MHz  
 Large signal response = 800 kHz

$$C_{out \text{ equiv.}} = \frac{R_2 + R_4}{2\pi f_O R_2 R_6} = 32 \text{ pF} (f_O = 15 \text{ MHz})$$

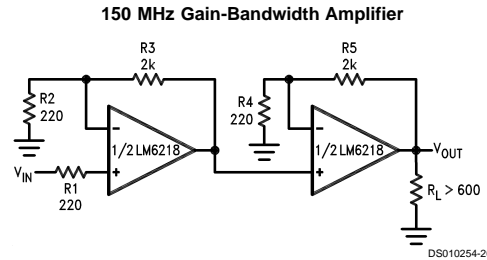
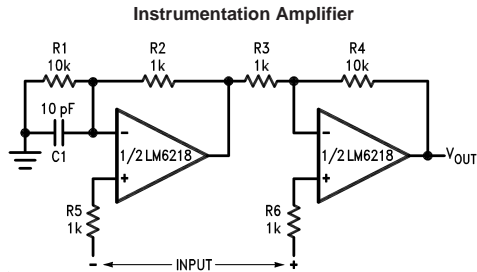
### Coaxial Cable Driver



DS010254-19

Small signal (200 mV<sub>p-p</sub>) BW = 5 MHz

## Application Information (Continued)



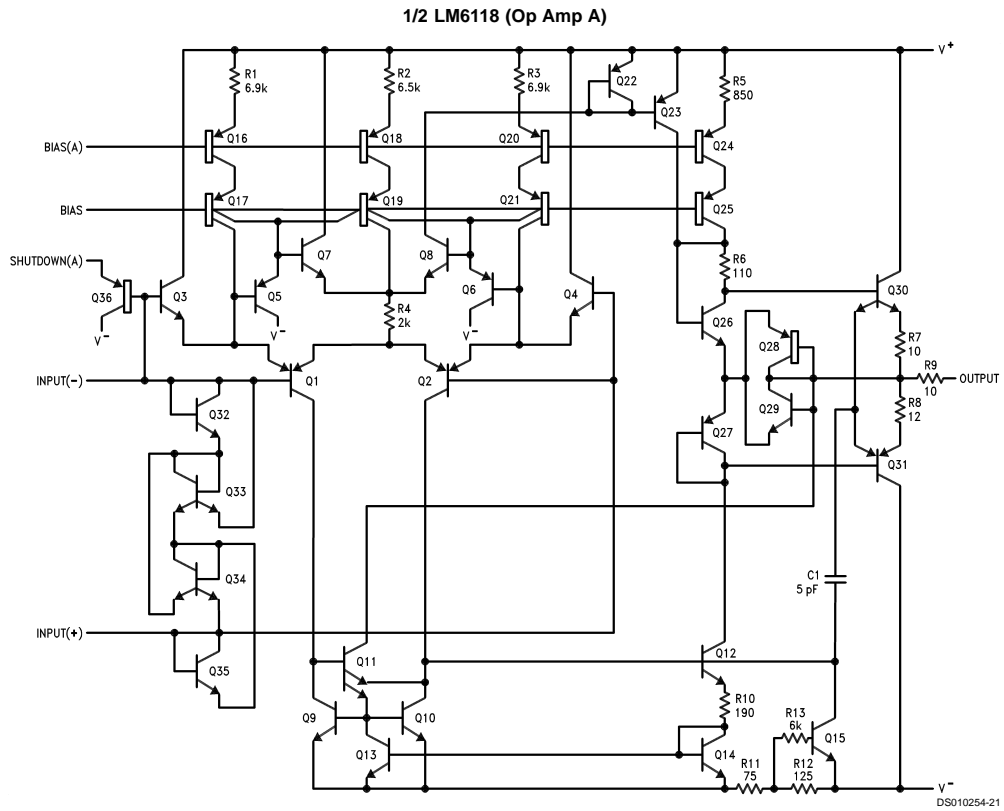
DS010254-18

$A_V = 100$ ,  $V_S = \pm 15V$ ,  
Small signal BW  $\approx 1.5$  MHz  
Large signal BW ( $20 V_{P-P}$ )  $\approx 800$  kHz

$A_V = 10$ ,  $V_S = \pm 15V$ , All resistors 0.01%  
Small signal and large signal ( $20 V_{P-P}$ ) B.W. = 800 kHz

DS010254-20

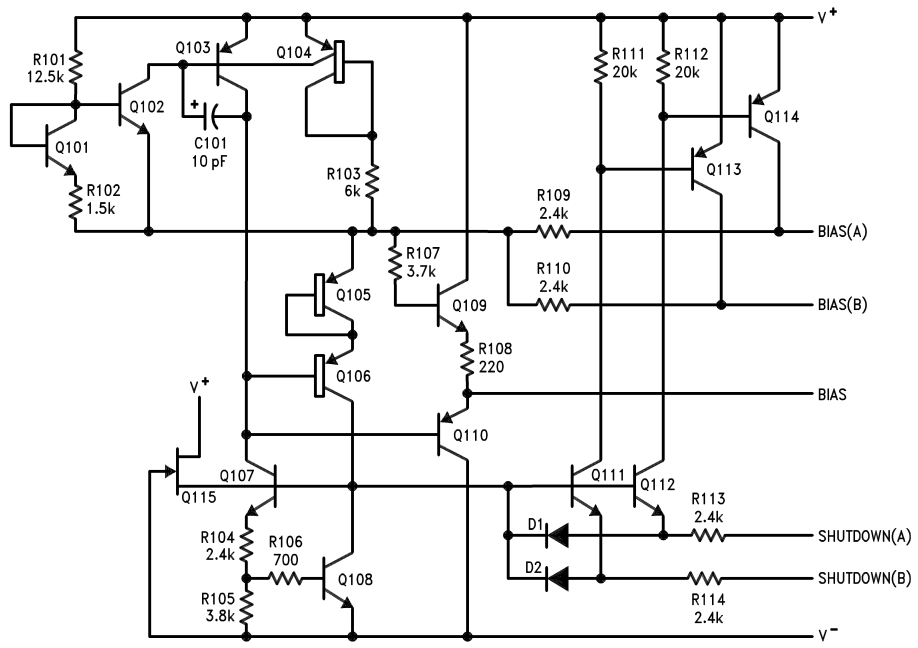
## Schematic Diagram



DS010254-21

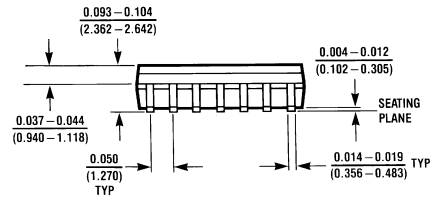
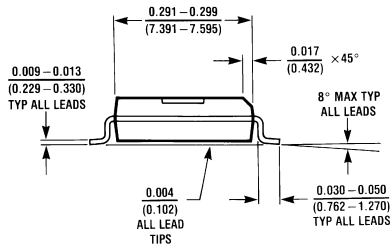
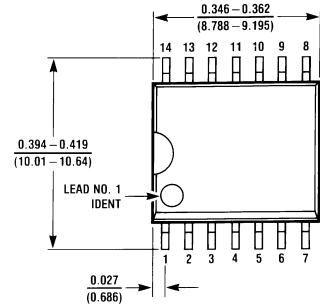
**Schematic Diagram** (Continued)

**Bias Circuit**



DS010254-22

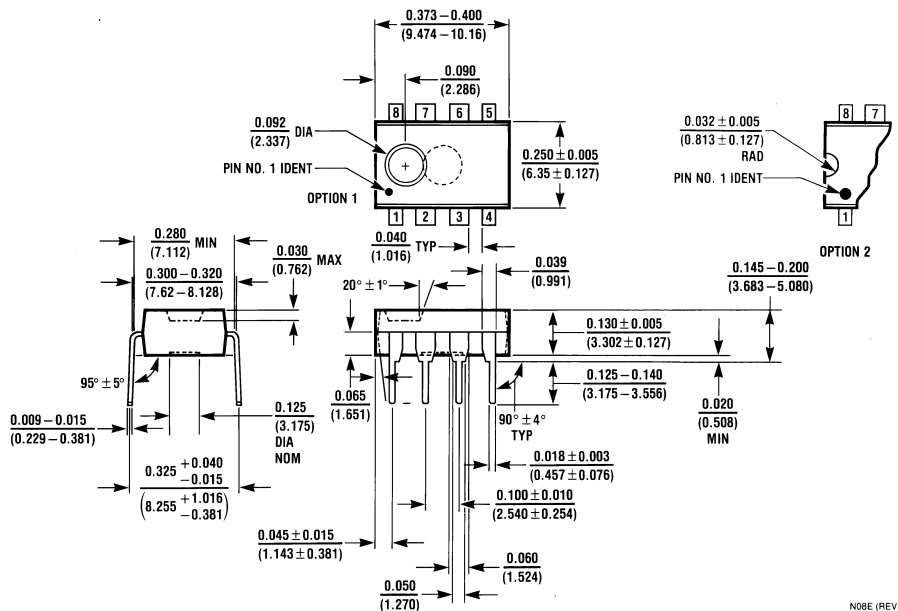
**Physical Dimensions** inches (millimeters) unless otherwise noted



M14B (REV D)

**8-Lead Molded Small Outline Package (M)**  
**Order Number LM6218AWM or LM6218WM**  
**NS Package Number M14B**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**8-Lead Molded Dual-In-Line Package (N)**  
**Order Number LM6118N, LM6218AN or LM6218N**  
**NS Package Number N08E**

N08E (REV F)

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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