National Semiconductor

August 1995

LM9040
Dual Lambda Sensor Interface Amplifier

General Description

The LM9040 is a dual sensor interface circuit consisting of two independent sampled input differential amplifiers designed for use with conventional Lambda Oxygen Sensors. The Lambda Sensor is used for monitoring the oxygen concentration in the exhaust of gasoline engines using catalytic after treatment and will deliver a voltage signal which is dependent on the air-fuel mixture. The gain of the amplifiers are internally set and can directly convert the Lambda sensor output voltage to a level suitable for A/D conversion in a system using a 5V reference.

The input common mode voltage range of each amplifier is ±2V with respect to the IC ground pin. This will allow the IC to connect to sensors which are remotely grounded at the engine exhaust manifold or exhaust pipe.

Each amplifier is capable of independent default operation should either, or both, of the leads to a sensor become open circuited.

Noise filtering is provided by an internal switched capacitor low pass filter as part of each amplifier, and by external components.

The LM9040 is fully specified over the automotive temperature range of −40°C to +125°C and is provided in a 14-pin Small Outline surface mount package.

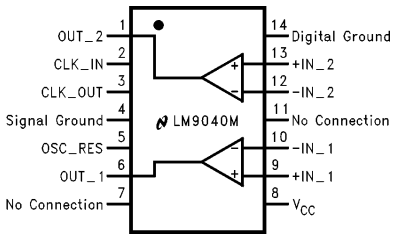
Features

- Single 5V supply operation
- Common mode input voltage range of ±2V
- Differential input voltage range of 50 mV to 950 mV
- Sampled differential input
- Switched capacitor low pass filter
- Internal oscillator and V_{BB} generator
- Open input default operation
- Cold sensor default operation
- Low power consumption (42 mW max)
- Gain set by design and guaranteed over the operating temperature range

Applications

- Closed loop emissions control
- Catalytic converter monitoring

Connection Diagram



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Top View

Ordering Information
LM9040M
See NS Package Number M14B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	−0.3V to +6.0V
Input Voltage Continuous (Note 1)	±14V
Input Voltage Transient t ≤ 1 ms (Note 1)	±60V
ESD Susceptibility (Note 2)	±2000V
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
Lead Soldering Information	
Vapor Phase (60 Seconds)	215°C
Infrared (15 Seconds)	220°C

Operating Ratings

Supply Voltage	4.75V to 5.25V
Differential Input Voltage	0V to +1V
Common Mode Voltage	±2V
Power Dissipation	42 mW

DC Electrical Characteristics

The following specifications apply for V_{CC} = 5.0V, V_{DIFF} = 500 mV, V_{CM} = 0V, R_{OSC} = 178 kΩ, −40°C ≤ T_A ≤ +125°C, DC Test Circuit *Figure 1*, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC}	Supply Current	4.75V ≤ V_{CC} ≤ 5.25V		8.0	mA
Z_{DIFF}	Differential Input Impedance	4.75V ≤ V_{CC} ≤ 5.25V	1.05	1.60	Meg Ω
Z_{IO}	Inverting Input to Ground Impedance	Non-Inverting Inputs Open	10.00		Meg Ω
V_{OL}	Output Low Voltage	V_{DIFF} = 0V, I_{LOAD} = 2.0 μA		100	mV
V_{OC}	V_{OUT} Center	One, or Both, Input(s) Open 4.75V ≤ V_{CC} ≤ 5.25V	V_{CC} • 0.380	V_{CC} • 0.425	V
$V_{OUT(ERROR)}$	(V_{OUT})−(V_{DIFF} • 4.53)	50 mV ≤ V_{DIFF} ≤ 950 mV, V_{CM} = 0V		±65	mV
V_{OH}	Output High Voltage	V_{DIFF} = 5V, I_{LOAD} = −2 μA	V_{CC} − 0.1V		V
R_{OUT}	Output Resistance		1500	3500	Ω
$CMRR_{(DC)}$	DC Common Mode Error	−2V ≤ V_{CM} ≤ +2V		±4.5	mV/V
T_{RISE}	Output Rise Time	C_{OUT} = 0.01 μF		1.2	ms
T_{FALL}	Output Fall Time	C_{OUT} = 0.01 μF		1.2	ms
F_C	Low Pass Filter −3 dB	C_{OUT} = 0.01 μF	400	700	Hz

Note 1: The input voltage must be applied through external 4 kΩ input resistors. See *Figure 2*, AC Test Circuit. Amplifier operation will be disrupted, but will not be destructive.

Note 2: ESD rating is with Human Body Model: 100 pF discharged through a 1500Ω resistor.

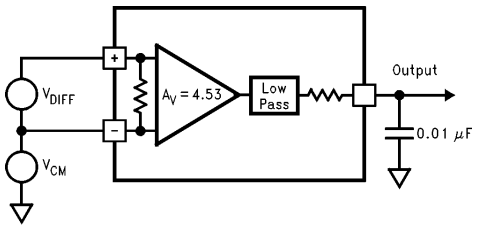

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FIGURE 1. DC Test Circuit

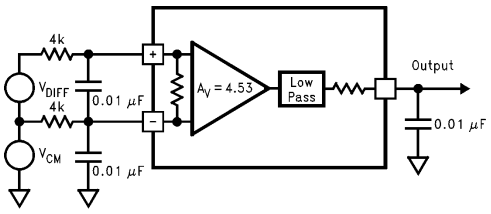

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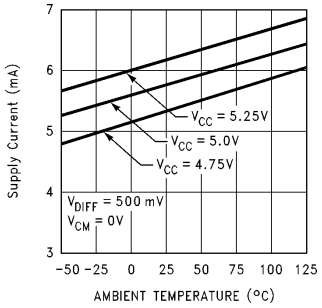
FIGURE 2. AC Test Circuit

Typical Performance Characteristics

Supply Current vs Temperature



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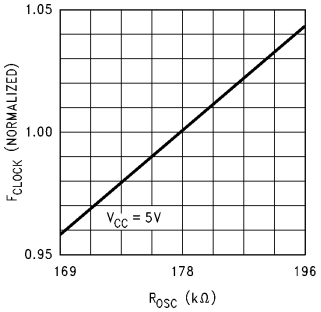
F_{CLOCK} (Normalized) vs R_{OSC}



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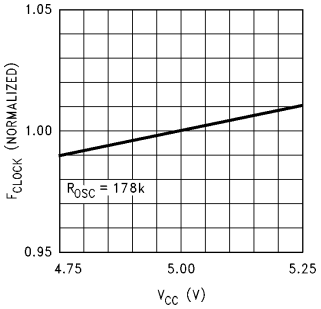
F_{CLOCK} (Normalized) vs V_{CC}



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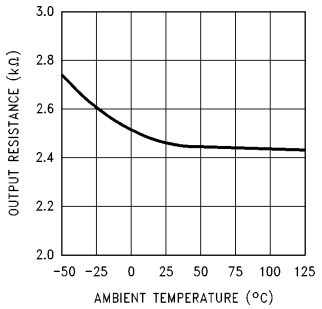
Output R vs Temperature



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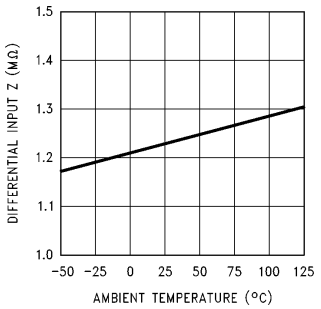
Z_{DIFF} vs Temperature



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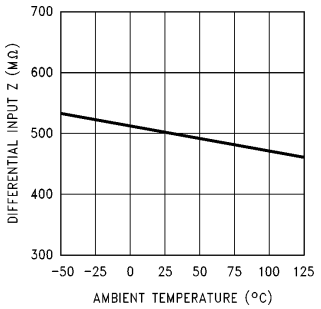
F_C vs Temperature



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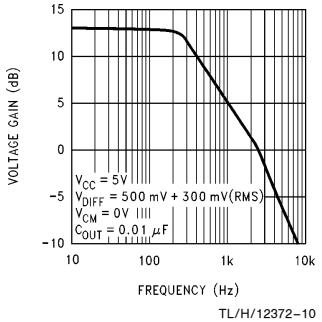
Voltage Gain vs Frequency



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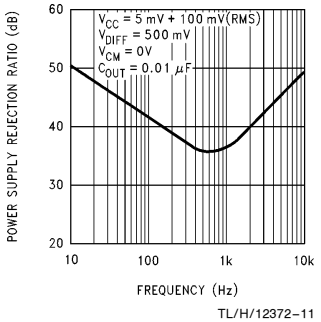
PSRR vs Frequency



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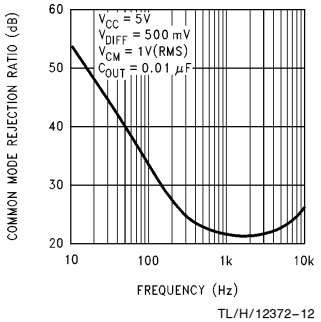
CMRR vs Frequency



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Circuit Description

The LM9040 is fabricated in CMOS technology and is designed to operate from a single, well regulated, 5V supply. The IC consists of two independent differential amplifiers which are designed using two-phased switched capacitor networks (SCN). The differential inputs have a common mode operating range of 2V above and below ground. The SCN includes the input sampling, the lowpass filter, cold sensor bias voltage, and the gain circuitry. Each amplifier has an independent voltage comparator to detect an open inverting input pin. Additional support circuitry includes the oscillator, clock generator, and V_{BB} bias generator.

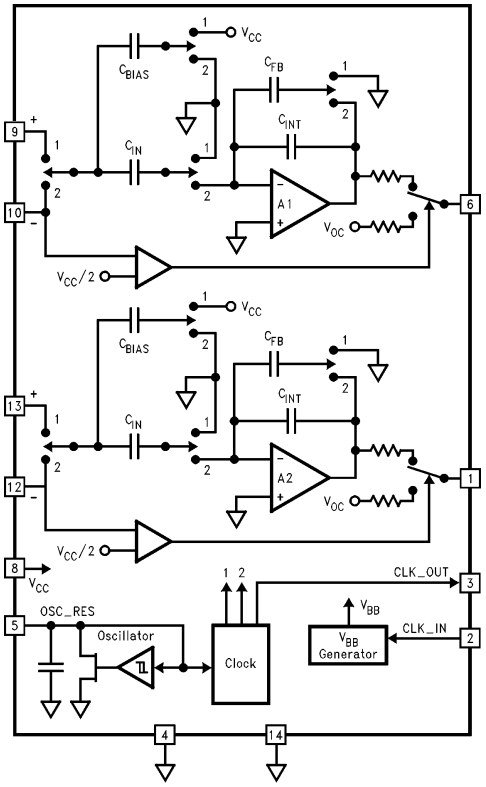

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FIGURE 3. Simplified Circuit

Oscillator

The device contains an internal oscillator which is used to drive the internal two-phase clock generator. The oscillator requires an external resistor value of 178 kΩ from the "OSC_RES" pin to device V_{CC}. This resistor value determines the charge rate of the internal capacitor, and thus sets the oscillator frequency. The internal oscillator capacitor is matched to the switched capacitor networks, so that the absolute capacitance values are not as important as is the absolute ratios of the capacitors. The oscillator frequency is approximately 200 kHz.

The oscillator resistor should be located as close to the OSC_RES pin as possible. Any variation of the oscillator resistor value, any stray capacitance on the OSC_RES pin, or any changes in the supply voltage, will result in a change in the oscillator frequency. This will directly affect the device Differential Input Impedance, and Low Pass filter response.

Additional circuitry takes the oscillator signal and generates two non-overlapping clock signals, and a CLK_OUT signal. The clock signals operate at one half the oscillator frequency, or typically 100 kHz. This results in a Nyquist frequency of typically 50 kHz.

Clock Out/Clock In

For the input stage to work with common mode voltages below Ground potential, a negative bias voltage (V_{BB}) is needed. The CLK_OUT pin is used to provide the AC signal needed to drive the internal V_{BB} bias generator through an external coupling capacitor. A minimum coupling capacitor value of 100 pF to a maximum value of 0.1 μF is recommended. The CLK_IN pin is the input to the V_{BB} bias generator circuitry.

Differential Input Circuit

The input stage can be best described as a switched Sample and Difference circuit (see *Figure 4*). When the input capacitor C_{IN} is switched to the non-inverting input, the input voltage plus the common mode voltage is stored on C_{IN}. When C_{IN} is switched to the inverting input, C_{IN} will be discharged by an amount equal to the common mode voltage. The remaining charge across C_{IN} will be equal to the differential input voltage, and a proportional charge will be transferred through the virtual ground via the gain stage.

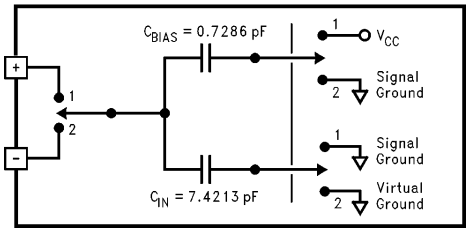

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FIGURE 4. Simplified Switched Capacitor Input Circuit

Differential Input Circuit (Continued)

The differential input impedance is a function of the value of the input capacitor array and the sampling frequency. The capacitor C_{BIAS} is used to generate a bias voltage across the Differential Input impedance (Z_{DIFF}). This bias voltage is similar to the Lambda Sensor output voltage at the stoichiometric air-fuel mixture ($\lambda = 1$). The bias voltage is set by the ratio of C_{IN} and C_{BIAS}, and the value of V_{CC}.

The resulting bias voltage across the Differential Input is defined as:

$$V_{BIAS} = \frac{V_{CC} \bullet C_{BIAS}}{(C_{IN} + C_{BIAS})}$$

With $C_{BIAS} = 0.7286$ pF, $C_{IN} = 7.421$ pF, $F_{CLOCK} =$ 100 kHz, and $V_{CC} = 5$V:

$$V_{BIAS} = \frac{5 \bullet 7.286E\text{-}13}{(7.4213E\text{-}12 + 7.286E\text{-}13)}$$

$$V_{BIAS} = 447 \text{ mV}$$

In effect, the result is the same as forcing a bias current through the Differential Input impedance.

The bias current is defined as:

$$I_{BIAS} = V_{CC} \bullet C_{BIAS} \bullet F_{CLOCK}$$

$$I_{BIAS} = 364.3 \text{ nA}$$

The Differential Input impedance is defined as:

$$Z_{DIFF} = \frac{1}{(C_{IN} + C_{BIAS}) \bullet F_{CLOCK}}$$

$$Z_{DIFF} = 1.227 \text{ M}\Omega$$

This bias voltage will be developed across the Differential Input impedance (Z_{DIFF}) if there is no other path available from the non-inverting input pin for I_{BIAS}, and the inverting input has a current path to ground. See *Figure 5*. During normal operating conditions I_{BIAS} will have a negligible effect on accuracy

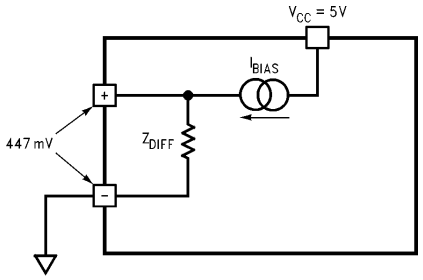

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FIGURE 5. Equivalent Input Bias Circuit

Differential Input Filtering

Since each input is sampled independently, an anti-aliasing filter is required at the amplifier inputs to ensure that the input signal does not exceed the Nyquist frequency.

This external low-pass filter is implemented by adding a capacitor (C_{DIFF}) across the differential input. See *Figure 6*. This forms an RC network across the differential inputs in conjunction with the required external 4 kΩ resistors and the differential input impedance (Z_{DIFF}). The capacitor selected should be small enough to have minimal effect on gain accuracy in the application, yet large enough to filter out unwanted noise. Given that the F_C of the LM9040 is typically 500 Hz, the use of a 0.01 μF capacitor will generally provide adequate filtering, with less than -0.4 dB of input attenuation at 500 Hz and approximately -28 dB at 50 kHz. A larger value capacitor can be used if needed, but a value larger than typically 0.02 μF will begin to dominate the cutoff frequency of the application. This capacitor must be a low leakage and low ESR type so that circuit performance is not degraded.

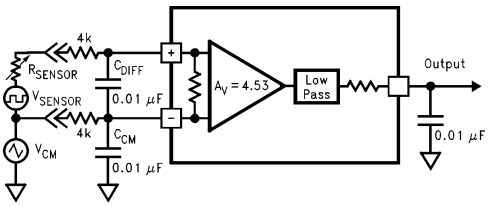

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FIGURE 6. Differential and Common Mode Filtering

Common Mode Filtering

The differential input sampling of the LM9040 actually reduces the effects of common mode input noise at low frequencies. The time interval between the sampling of the inverting input and the non-inverting input is one half of a clock period. A change in the common mode voltage during this short time interval can cause an error in the charge stored on C_{IN}. This will result in an error seen on the output voltage. For a sine-wave common mode voltage the minimum common mode rejection is:

$$CMRR = 2 \bullet \pi \bullet F_{CMR} \bullet (0.5/F_{CLOCK}) \bullet 4.53$$

Where F_{CMR} is the frequency of the common mode signal, and F_{CLOCK} is the clock frequency.

Common Mode Filtering (Continued)

For a common mode sine wave signal having a frequency 100 Hz, and with a F_{CLOCK} of 100 kHz, the minimum common mode rejection would be:

$$CMRR = 2 \bullet 3.14159 \bullet 100 \bullet 5E\text{-}6 \bullet 4.53$$

$$CMRR = 0.014 = -37\ dB$$

If the common mode sine wave has a peak to peak value of 2V, the maximum voltage error at the output would be:

$$V_{OUT(CM)} = 2V \bullet 0.014 = 28\ mV$$

As this formula shows, the value of $V_{OUT(CM)}$ is proportional to the frequency of the CMR signal. If the frequency is doubled, the value of $V_{OUT(CM)}$ is also doubled. The addition of a small bypass capacitor (C_{CM}) from the non-inverting input to ground will help counter this problem. See *Figure 6*. However, the use of this bypass capacitor creates a new problem in that the differential input is no longer balanced. While the Lambda sensor is cold (i.e. $R_{SENSOR} > 10$ MegΩ) there is little difference in CMR performance. As the Lambda sensor heats to the operating temperature and the sensor resistance decreases, the common mode signal is no longer applied to both inputs equally. This imbalance causes $V_{OUT(CM)}$ to increase as R_{SENSOR} decreases, as the non-inverting input will see the full common mode signal, while the non-inverting input will see an attenuated common mode signal.

The selection of the value of the CMR bypass capacitor needs to be balanced with the need for reasonable reduction, or elimination, of common mode signals with both cold and hot sensors. Since normal operation will need to include consideration of the entire impedance range of the sensor, a trade off in overall application performance may be needed.

Generally, the value of the CMR bypass capacitor should be kept as low as possible, and should not be larger than the differential input filter capacitor. Values in the range of 0.001 μF to 0.01 μF will usually provide reasonable CMR results, but optimum results will need to be determined empirically, as the source of common mode signals will be unique to each application.

Gain and Filter Stage

The signal gain and filter stage is designed to have a DC gain of 4.53 V/V, with a cut-off frequency of typically 500 Hz. The external 4 kΩ resistors on each input pin are in series with the differential input impedance. Together they form a voltage divider circuit across the input such that the net DC gain of the application circuit is 4.50 V/V.

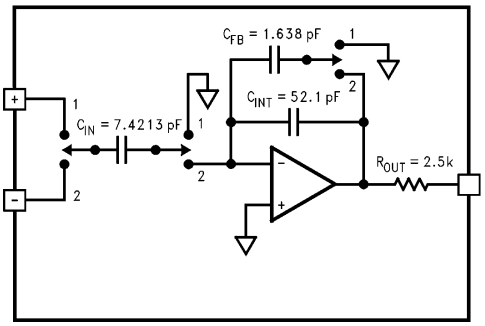

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FIGURE 7. Simplified Gain and Filter Circuit

The internal gain is set by the ratio of C_{IN} and C_{FB}:

$$GAIN_{DC} = \frac{C_{IN}}{C_{FB}}$$

$$GAIN_{DC} = \frac{7.4213\ pF}{1.6383\ pF} = 4.53\ V/V$$

The corner frequency (−3 dB) is set by the ratio of C_{FB} and C_{INT}, and by F_{CLOCK}:

$$F_C = \frac{F_{CLOCK} \bullet C_{FB}}{2 \bullet \pi \bullet C_{INT}}$$

$$F_C = \frac{1E5 \bullet 1.6383E\text{-}12}{2 \bullet 3.14159 \bullet 52.1E\text{-}12} = 500\ Hz$$

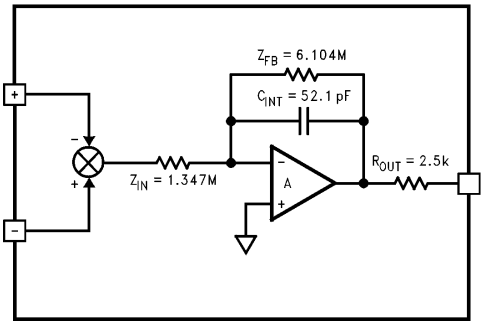

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FIGURE 8. Equivalent Gain and Filter Circuit

Cold Sensor

Typically, a Lambda sensor will have an impedance of less than 10 kΩ when operating at temperatures between 300°C, and 500°C. When a Lambda sensor is not at operating temperature, its impedance can be more than 10 MegΩ. Any voltage signal that may be developed is seriously attenuated. During this high impedance condition the LM9040 will provide a default output voltage.

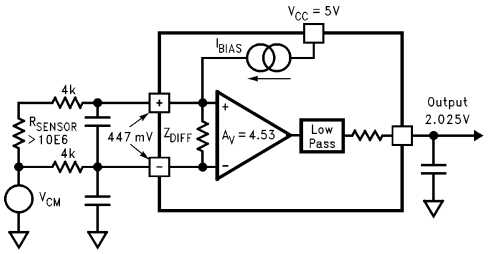

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FIGURE 9. V_{OUT} with Cold Lambda Sensor

Each amplifier input has a bias charge applied across the Differential Input impedance (Z_{DIFF}) by means of charge redistribution through the switched capacitor network. This bias charge is a ratio of V_{CC}, and is typically 447 mV for a V_{CC} value of 5.00V. This will provide an output voltage of typically 2.025V.

While the Lambda sensor is high impedance, the 447 mV across Z_{DIFF} will be the dominant input signal. As the Lambda sensor is heated, and the sensor impedance begins to drop, the voltage signal from the sensor will become the dominate signal.

Output Resistance

With normal operation, each output has typically 2.5 kΩ of resistance. This resistance, along with an external capacitor, form a RC low pass filter to remove any clock noise from the output signal. An external output filter capacitor value of 0.01 μF is recommended. Additionally, the output resistance will provide current limiting for the output stage should it become shorted to Ground or V_{CC}.

Any DC loading of the output will cause an error in the measured output voltage. This error will be equal to the I•R drop across the output resistance:

$$V_{ERROR} = I_{LOAD} \bullet 2.5\ k\Omega$$

Open Input Pins Defaults

In any remote sensor application it is desirable to be able to deal with the possibility of open connections between the sensor and the control module. The LM9040 is capable of providing an output voltage scaled to V_{CC} should either, or both, of the wires to the Lambda sensor open. The two inputs handle the open circuit condition differently. The LM9040 will provide a default V_{OUT} that is typically 2.025V when V_{CC} is at 5V.

For the case of an open connection of the non-inverting input, the device would react the same as for the Cold Sensor condition. The internal bias voltage across Z_{IN} would cause the output voltage to be at a value defined by V_{CC} and the LM9040 DC gain. The inverting input would still be connected to the Lambda sensor ground, so any common mode signals would still need to be allowed for in this condition. See *Figure 9*.

For the case of an open connection of the inverting input, the device output stage switches from the amplifier output to a resistive voltage divider. In this case, the default V_{OUT} is not dependent on the gain stage, and any signal on the non-inverting input will have no effect on the output. Each amplifier has a comparator to monitor the voltage on the inverting input pin. When the voltage on an inverting pin goes above typically 2.5V, the comparator will switch the output from the amplifier output to the voltage divider stage. To fully implement this function requires external pull-up resistors for each of the inverting inputs. To minimize signal errors due to DC currents through the 4 kΩ resistors, the pull-up resistors need to be added in the application circuit between the 4 kΩ input resistor and the connection to the Lambda sensor ground point. A typical pull-up value of 51 kΩ to V_{CC} is recommended. During this condition, the effective resistance of the output stage will be 3.5 kΩ typically. See *Figure 10*.

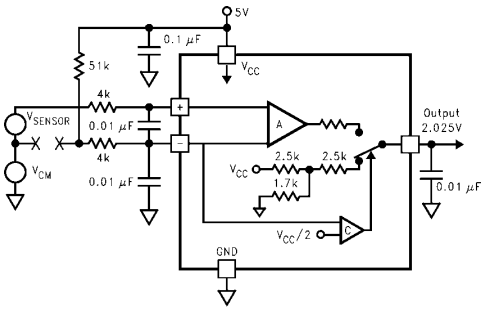

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FIGURE 10. V_{OUT} with Open Inverting Input

Open Input Pins Defaults (Continued)

In the cases where both the inverting and non-inverting pins are open, the non-inverting condition (i.e.: voltage divider across the output) will be the dominant condition.

Any common mode signal seen by inverting input pin should not be allowed to exceed the Common Mode voltage range. Exceeding the positive Common Mode voltage limit could cause the inverting input pin voltage comparator to act as if the inverting input pin is open. Since the comparator circuit is not part of the switched capacitor network there is no frequency limitation on the signal to the comparator. Any transient on the inverting input pin which goes above the comparator threshold will immediately cause the output to switch to the open sensor mode. The output will return to normal operation when the voltage on the inverting input falls below the comparator threshold.

Supply Bypassing

For best performance the LM9040 requires a V_{CC} supply which is stable and noise free. The same 5V V_{REF} supply used for the A/D converter is the recommended V_{CC} supply. During operation the device will generate current spikes coincident with the clock edges. Inadequate bypassing will cause excessive clock noise on the outputs, as well as noise on the V_{CC} line. The LM9040 V_{CC} pin should be bypassed with a minimum 0.1 μF capacitor to the Signal Ground pin, and should be located as close to the device as possible. Some applications may require an additional 4.7 μF tantalum capacitor, especially if there are several other switched capacitor devices running off the same 5V supply line. The Signal and Digital Ground pins should be tied together as close to the device as possible.

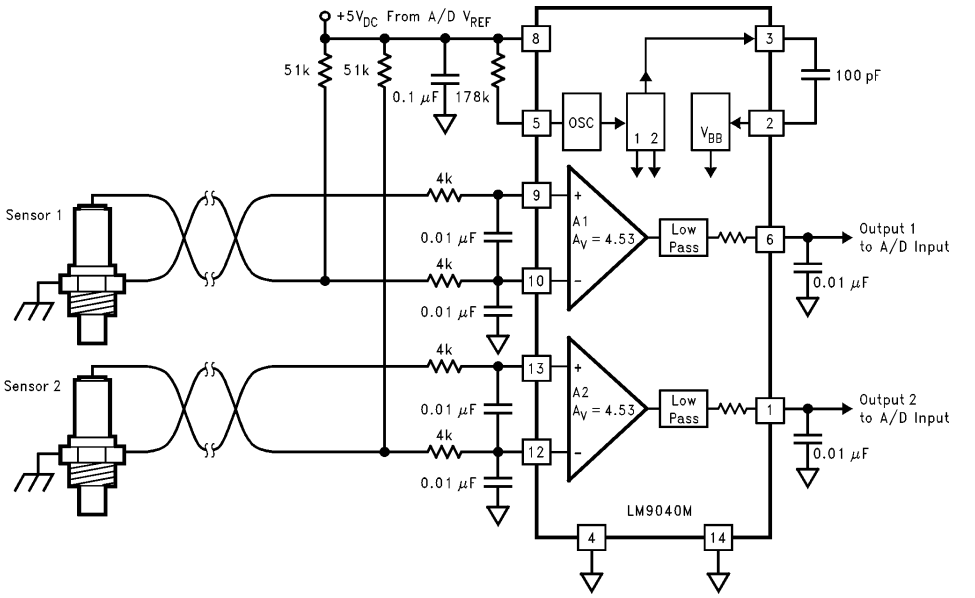

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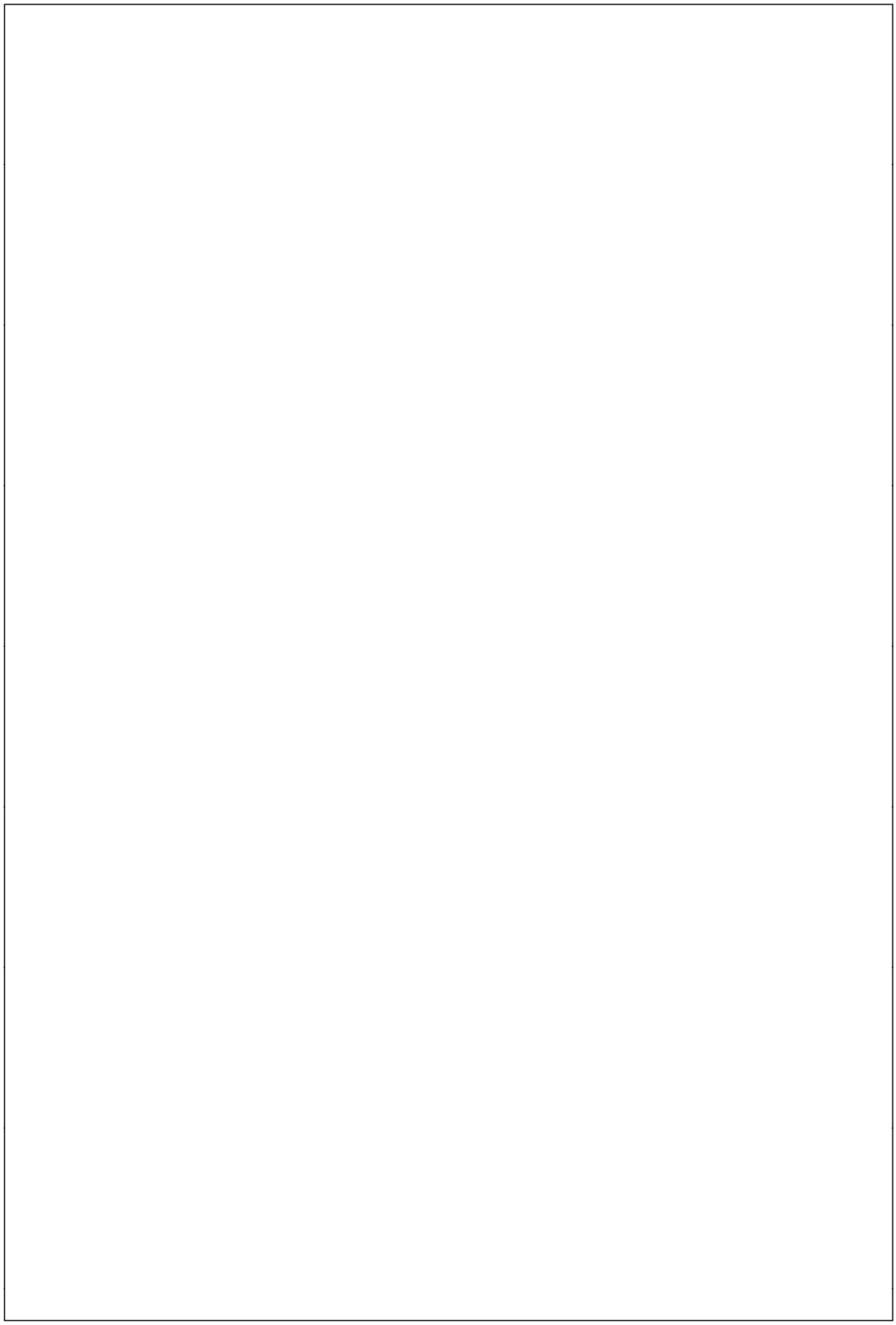
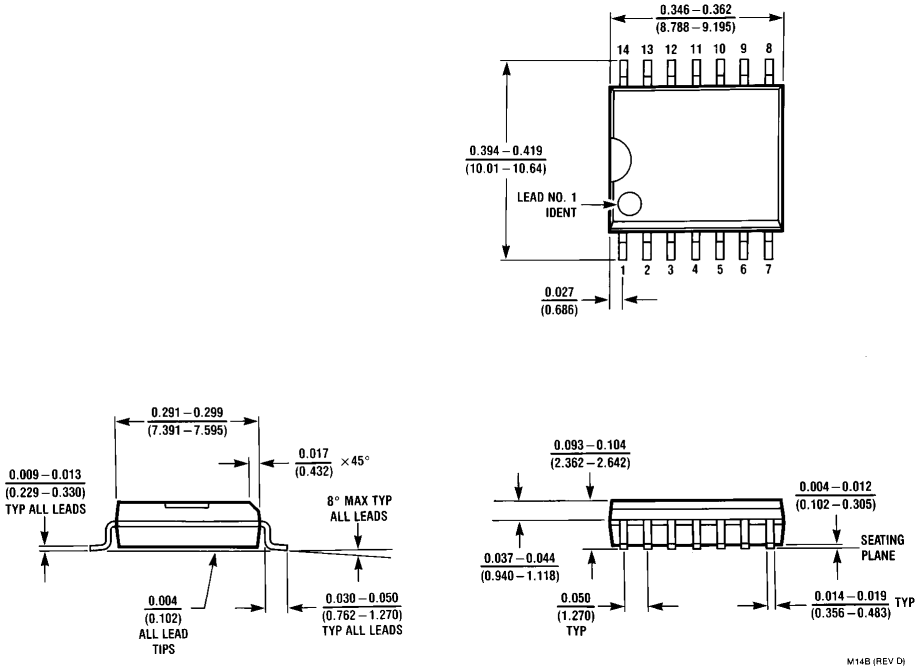
FIGURE 11. Typical Application



Physical Dimensions inches (millimeters)



14-Lead (0.300″ Wide) Molded Small Outline Package, JEDEC
Order Number LM9040M
NS Package Number M14B

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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